

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J43 MLB SCHEMATIC DVT

REV 6.5.0

4/09/13

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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21	24	LPDDR3 DRAM Channel A (32-63)	J41_MLB	02/06/2013	66	110	PCB Rule Definitions	CONSTRAINTS	10/24/2012
22	25	LPDDR3 DRAM Channel B (0-31)	J41_MLB	02/06/2013	67	111	CPU Constraints	CONSTRAINTS	09/25/2012
23	26	LPDDR3 DRAM Channel B (32-63)	J41_MLB	02/06/2013	68	112	PCH Constraints 1	CLEAN_J43	11/13/2012
24	27	LPDDR3 DRAM Termination	J41_MLB	02/06/2013	69	113	PCH Constraints 2	J41_MLB	12/14/2012
25	28	Thunderbolt Host (1 of 2)	J41_MLB	02/06/2013	70	114	Memory Constraints	CONSTRAINTS	09/25/2012
26	29	Thunderbolt Host (2 of 2)	J41_MLB	02/06/2013	71	115	Thunderbolt Constraints	CONSTRAINTS	09/25/2012
27	30	TBT Power Support	J41_MLB	02/06/2013	72	116	Camera Constraints	J41_MLB	01/30/2013
28	32	Thunderbolt Connector A	J41_MLB	02/07/2013	73	117	SMC Constraints	CONSTRAINTS	09/25/2012
29	35	Wireless Connector	J41_MLB	02/06/2013	74	118	Project Specific Constraints	J41_MLB	12/07/2012
30	37	SSD Connector	J41_MLB	04/09/2013	75	119	Project Specific Constraints	CONSTRAINTS	09/25/2012
31	39	Camera 1 of 2	J41_MLB	04/02/2013	76	121	Reference	J41_MLB	07/03/2012
32	40	Camera 2 of 2	J41_MLB	03/20/2013					
33	44	SD READER CONNECTOR	MASTER	07/01/2011					
34	45	SD CONTROLLER (GL3219)	MASTER	10/11/2010					
35	46	External A USB3 Connector	J41_MLB	02/07/2013					
36	48	IPD Connector	J41_MLB	02/12/2013					
37	50	SMC	J41_MLB	02/06/2013					
38	51	SMC Shared Support	J41_MLB	02/06/2013					
39	52	SMC Project Support	J41_MLB	02/06/2013					
40	53	SMBus Connections	J41_MLB	02/06/2013					
41	54	High Side Current Sensing	J41_MLB	03/28/2013					
42	55	Voltage & Load Side Current Sensing	J41_MLB	03/28/2013					
43	56	Debug Sensors 1	J41_MLB	03/28/2013					
44	58	Thermal Sensors	J41_MLB	02/06/2013					
45	60	Fan	J41_MLB	02/06/2013					

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9800	1	SCHEM_MLB,J43	SCH	CRITICAL	
820-3437	1	PCBF_MLB,J43	PCB	CRITICAL	

PRODUCT SAFETY REQUIREMENTS:
 PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
 PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
 NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE <PART_DESCRIPTION>	
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DRAWING
 TITLE=MLB
 ABBREV=DRAWING
 DATE_MODIFIED=Thu Apr 9 20:06:04 2013

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE, COMMON, MLB_MISC, MLB_DEBUG: ENG, MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO, TBTHV:P15V, EDP, CAM_XTAL:NO, CAM_WAKE:NO, APCLKRQ:ISOL, TPAD_INTWAKE:SHARED, USB_PWR:S3, SD_ON_MLB, VCORE_FETS
MLB_DEVEL: ENG	ALTERNATE, BKLT: ENG, XDP_CONN, DDRVREF_DAC, S0PGOOD_ISL, DBGLED, ISNS: ENG
MLB_DEVEL: PVT	XDP_CONN
MLB_DEBUG: ENG	DEVEL_BOM, XDP, LPCPLUS
MLB_DEBUG: PVT	DEVEL_BOM, BKLT: PROD, XDP, LPCPLUS, ISNS: PROD
MLB_DEBUG: PROD	BKLT: PROD, LPCPLUS, XDP, ISNS: PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS: ENG	CPU_ML_SNS:YES, CPUV_ML_SNS:YES, DRAM_SNS:YES, P1V05_SNS:NO, AIRPORT_SNS:YES, SSD_SNS:YES, LCOBELT_SNS:YES, P3V15_SNS:YES, P3V30_SNS:NO, OTHER_ML_SNS:NO, CAM_SNS:YES, CPUVDR_SNS:YES, PANEL_SNS:YES
ISNS: PROD	CPU_ML_SNS:YES, CPUV_ML_SNS:YES, DRAM_SNS:YES, P1V05_SNS:NO, AIRPORT_SNS:NO, SSD_SNS:YES, LCOBELT_SNS:NO, P3V15_SNS:NO, P3V30_SNS:NO, OTHER_ML_SNS:NO, CAM_SNS:NO, CPUVDR_SNS:NO, PANEL_SNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:MICRON_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM, 256KBIT, SPI, 5MHZ, 1.8V, 2X3QFN	U2890	CRITICAL	TBTROM:BLANK
341S3802	1	IC, EEPROM, C/S (V23.4) EVT, J41/J41	U2890	CRITICAL	TBTROM:PROG
338S1159	1	IC, BMC12-A3, 40MHZ/50MHZ MCU, 9X9, 157BGA	U5000	CRITICAL	SMC:BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH, 8X6X0.8	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH, 8X6X0.8	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S3809	1	IC, EFI ROM (V0071) DVT, J41/J43	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW, SR16M, PRQ, CO, 1.3, 15W, 2+3, 1.0, 3M, BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW, SR16L, PRQ, CO, 1.4, 15W, 2+3, 1.1, 3M, BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW, SR16H, PRQ, CO, 1.7, 15W, 2+3, 1.1, 4M, BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC, TWT, CR-4C, B1, PRQ, C10, 288, 12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC, BCM15700A2, S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY, SUBASSY, PCBA, HALL EFFECT, K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 MLB DYNAMX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7670	1	LABEL, TEXT, MLB, K21/K78	LABEL		
376S0964	2	MOSFET, N-CH, 25V, 30A, 9.6M, 8P 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET, N-CH, 25V, 30A, 6.1M, 8P 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET, N-CH, 30V, 15.3A, 12M, 8P 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET, N-CH, 30V, 22A, 6.0M, 8P 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC, SDRAM, 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0676	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0680	4	IC, SDRAM, 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0678	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0666	4	IC, SDRAM, 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0679	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE:MICRON_4GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1


Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NEC alt for Diodes dual
376S1089	376S1128		ALL	NEC alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cytac
372S0186	372S0185		ALL	NEC alt to Diodes
197S0479	197S0478		ALL	200W Epcos alt to NEC
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cytac alt to NEC
197S0480	197S0343		ALL	NEC crystal alt to TSC
197S0481	197S0343		ALL	Epson crystal alt to TSC
107S0254	107S0241		ALL	Cytac sense R alt to TFF
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	Onsemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NEC alt to TSC
197S0545	197S0544		ALL	Epson alt to TSC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Beneas alt to Vishay
152S1876	152S1804		ALL	TK alt to Toko
107S0255	107S0240		ALL	Cytac alt to TFF
107S0250	107S0248		ALL	Cytac alt to TFF

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BOM Configuration

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BOM Variants NOTE: All the "GOOD" BOM Configs have been de-activated

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4146	PCBA,MLB,GOOD,HY-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4293	PCBA,MLB,GOOD,HY-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4294	PCBA,MLB,GOOD,EL-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4295	PCBA,MLB,GOOD,EL-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4745	PCBA,MLB,GOOD,MI-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
639-4445	PCBA,MLB,BETTER,HY-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4446	PCBA,MLB,BETTER,HY-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4447	PCBA,MLB,BETTER,EL-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4448	PCBA,MLB,BETTER,EL-8GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4746	PCBA,MLB,BETTER,MI-4GB,J43	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
639-4755	PCBA,MLB,BEST,HY-4GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4756	PCBA,MLB,BEST,HY-8GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4757	PCBA,MLB,BEST,EL-4GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4758	PCBA,MLB,BEST,EL-8GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4759	PCBA,MLB,BEST,MI-4GB,J43	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
685-0025	CMN PTS,PCBA,MLB,J43	MLB_COMMON
985-0018	J43 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0064	VCORE FET,REN,J43	VCORE_FET:REN
685-0065	VCORE FET,VSHY,J43	VCORE_FET:VSHY

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
685-0064	685-0065		ALL	Replaces alt for Vishay

333S0704	333S0700		ALL	Elpida CSM DRAM alt to Hynix
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Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3758	1	IC,SMC-A3 SCPL,EXT,V22.12a19,PROTO 1,J43	U5000	CRITICAL	SMC:PROG

BOM Groups


BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S1215	1	IC,GL3219,USB3 SD CARD READER,46P,LQFN	U4500	CRITICAL	

Sub-BOMs

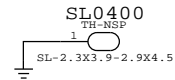
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0018	1	J43 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0025	1	CMN PTS,PCBA,MLB,J43	CMNPTS	CRITICAL	MLB_CMNPTS
685-0065	1	VCORE FET,VSHY,J43	VCOREFETS	CRITICAL	VCORE_FETS

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BOM Variants			
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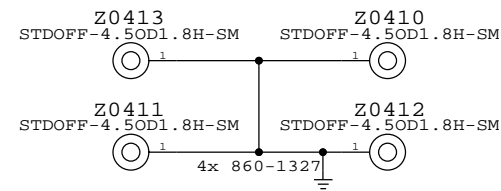
PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN, TOPSIDE, ALT, J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN, TOPSIDE, COVER, ALT, J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN, TBT, J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN, COVER, TBT, J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN, MDP, J11/J13	MDFCAN	CRITICAL	
806-3083	1	SHLD, USB, M/B, J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR, CPU, J41/J43	CPU_INSULATOR	CRITICAL	

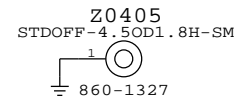
Plated Board Slot



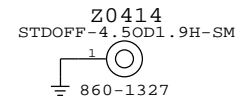
CPU Heat Sink Mounting Bosses



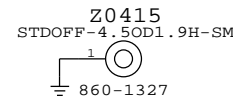
Fan Boss



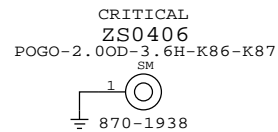
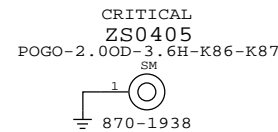
X21 Boss



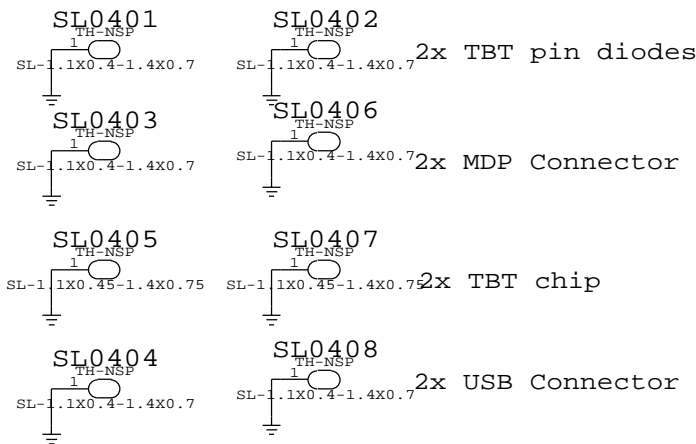
SSD Boss



EMI I/O Pogo Pins
DisplayPort Pogo USB/SD Card Pogo



Can Slots



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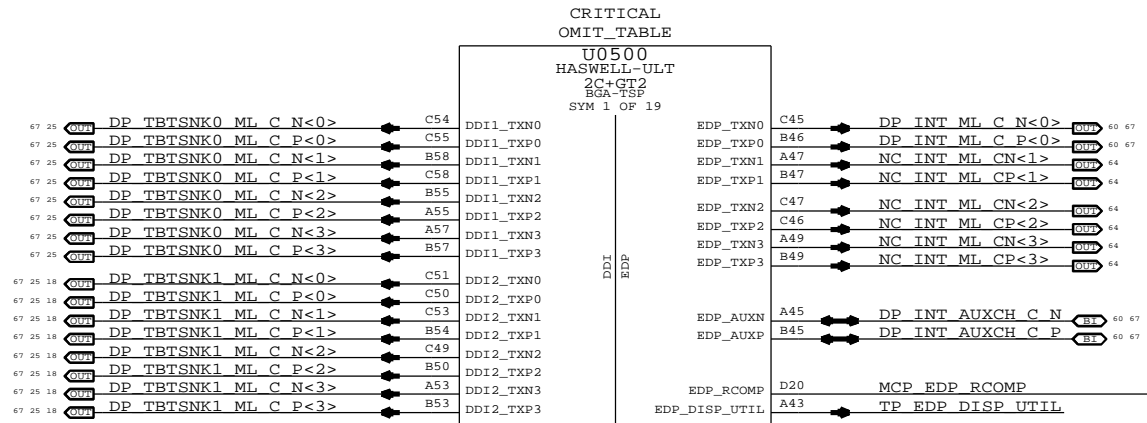
D

D

DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)



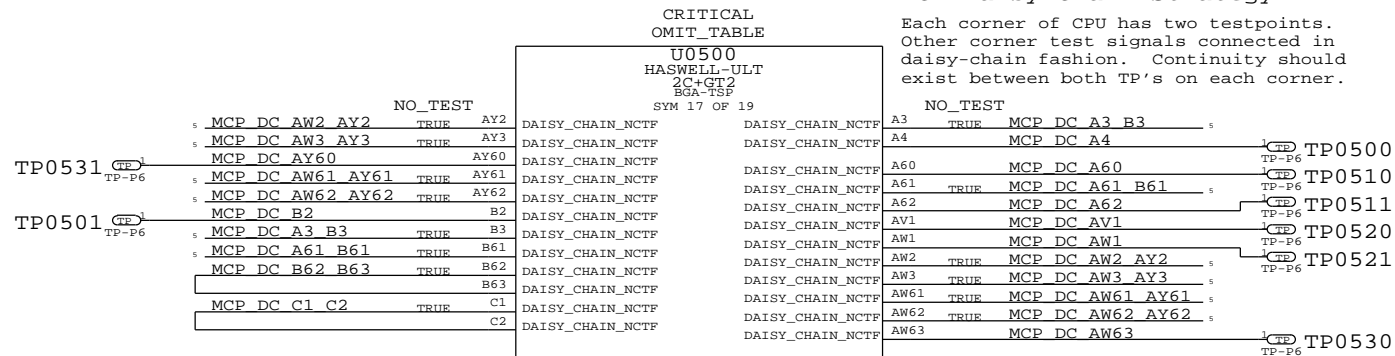
eDP Port Assignment:

C

C

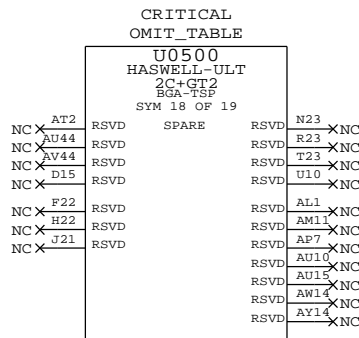
MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.



B

B



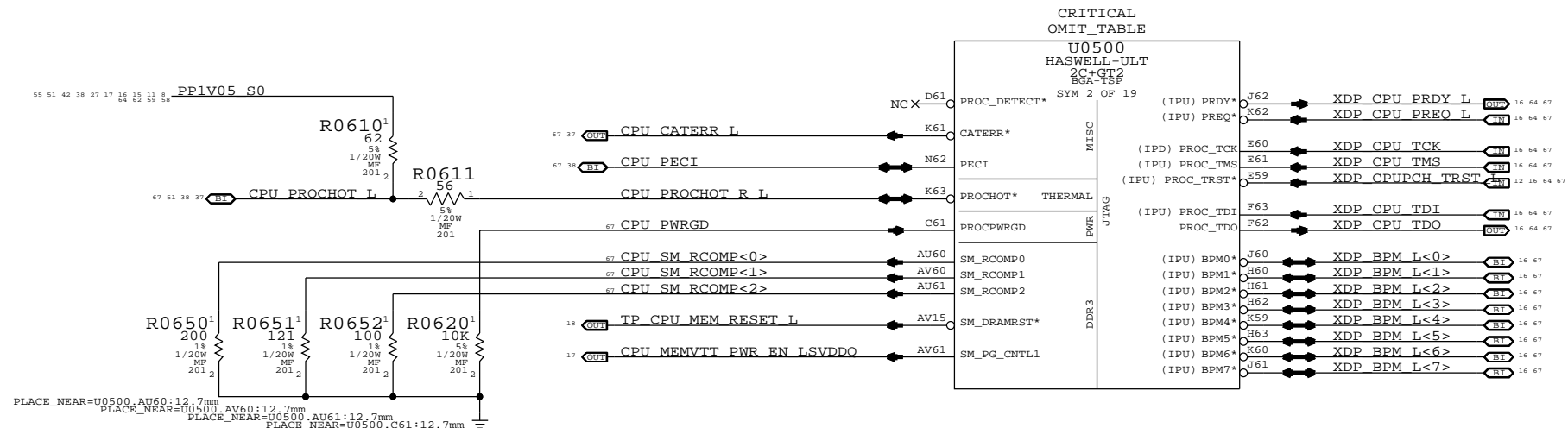
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A

SYNC_MASTER=J41_MLB		SYNC_DATE=02/06/2013	
CPU GFX/NCTF/RSVD			
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D

D



C

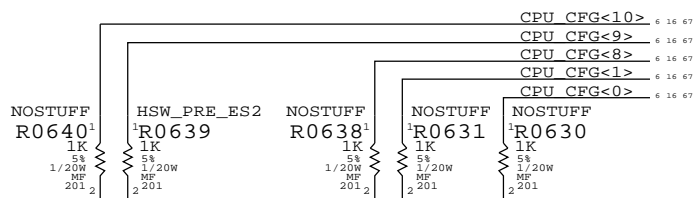
C

B

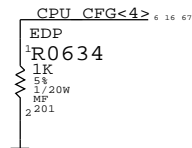
B

CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

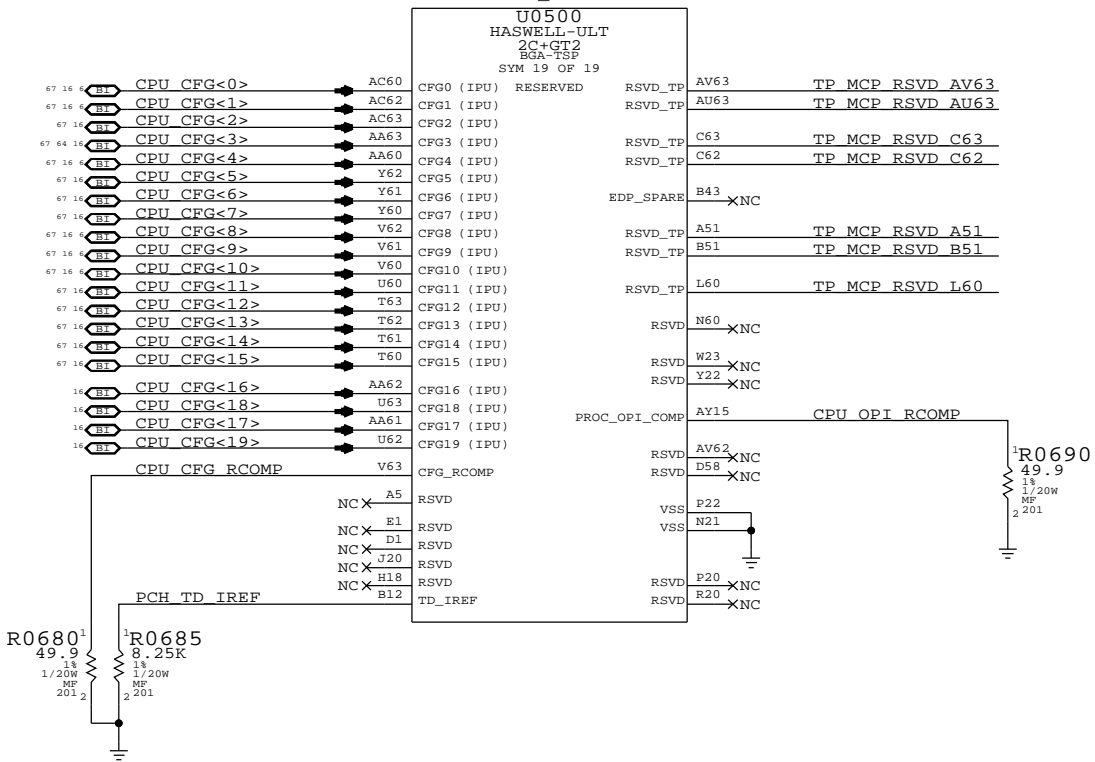
These can be placed close to J1800 and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



CRITICAL OMIT_TABLE



A

A

SYNC MASTER=J41_MLB SYNC DATE=04/02/2013

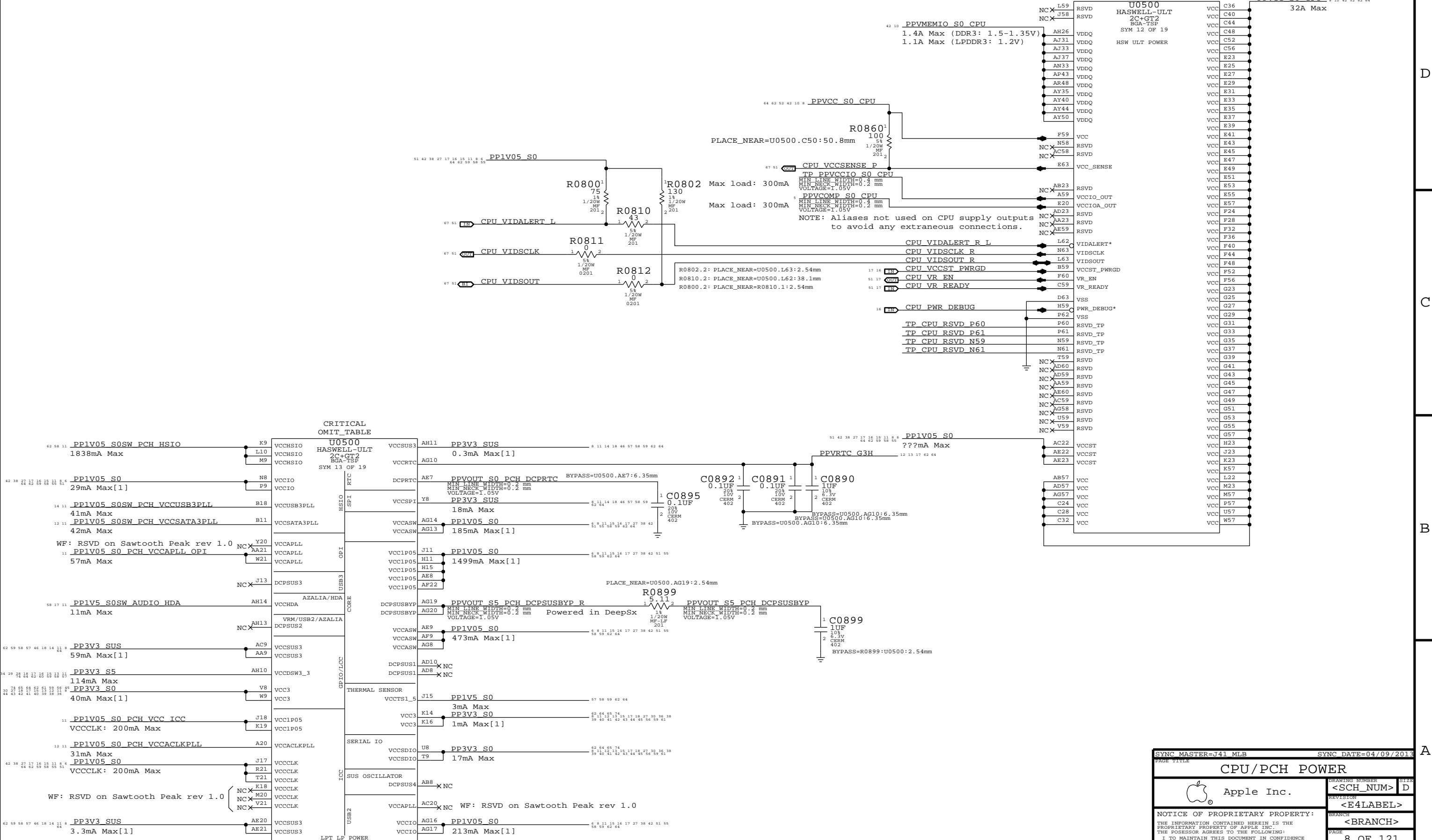
CPU Misc/JTAG/CFG/RSVD

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HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
 LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
 Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



CRITICAL OMIT TABLE

Symbol	Label	Value	Notes
L59	RSVD		
J58	RSVD		
42 10	PPVMEMIO_S0_CPU	1.4A Max (DDR3: 1.5-1.35V) 1.1A Max (LPDDR3: 1.2V)	
AH26	VDDQ		
AJ31	VDDQ		
AJ33	VDDQ		
AJ37	VDDQ		
AN33	VDDQ		
AP43	VDDQ		
AR48	VDDQ		
AY35	VDDQ		
AY40	VDDQ		
AY44	VDDQ		
AY50	VDDQ		
F59	VCC		
N58	RSVD		
AC58	RSVD		
E63	VCC_SENSE		
AB23	RSVD		
A59	VCCIO_OUT		
E20	VCCIO_OUT		
AD23	RSVD		
AA23	RSVD		
AE59	RSVD		
L62	VIDALERT*		
N63	VIDSCLK		
L63	VIDSOUT		
B59	VCCST_PWRGD		
F60	VR_EN		
C59	VR_READY		
D63	VSS		
H59	PWR_DEBUG*		
P62	VSS		
P60	RSVD_TP		
P61	RSVD_TP		
N59	RSVD_TP		
N61	RSVD_TP		
T59	RSVD		
AD60	RSVD		
AD59	RSVD		
AA59	RSVD		
AE60	RSVD		
AC59	RSVD		
AG58	RSVD		
U59	RSVD		
V59	RSVD		
AC22	VCCST		
AE22	VCCST		
AE23	VCCST		
AB57	VCC		
AD57	VCC		
AG57	VCC		
C24	VCC		
C28	VCC		
C32	VCC		

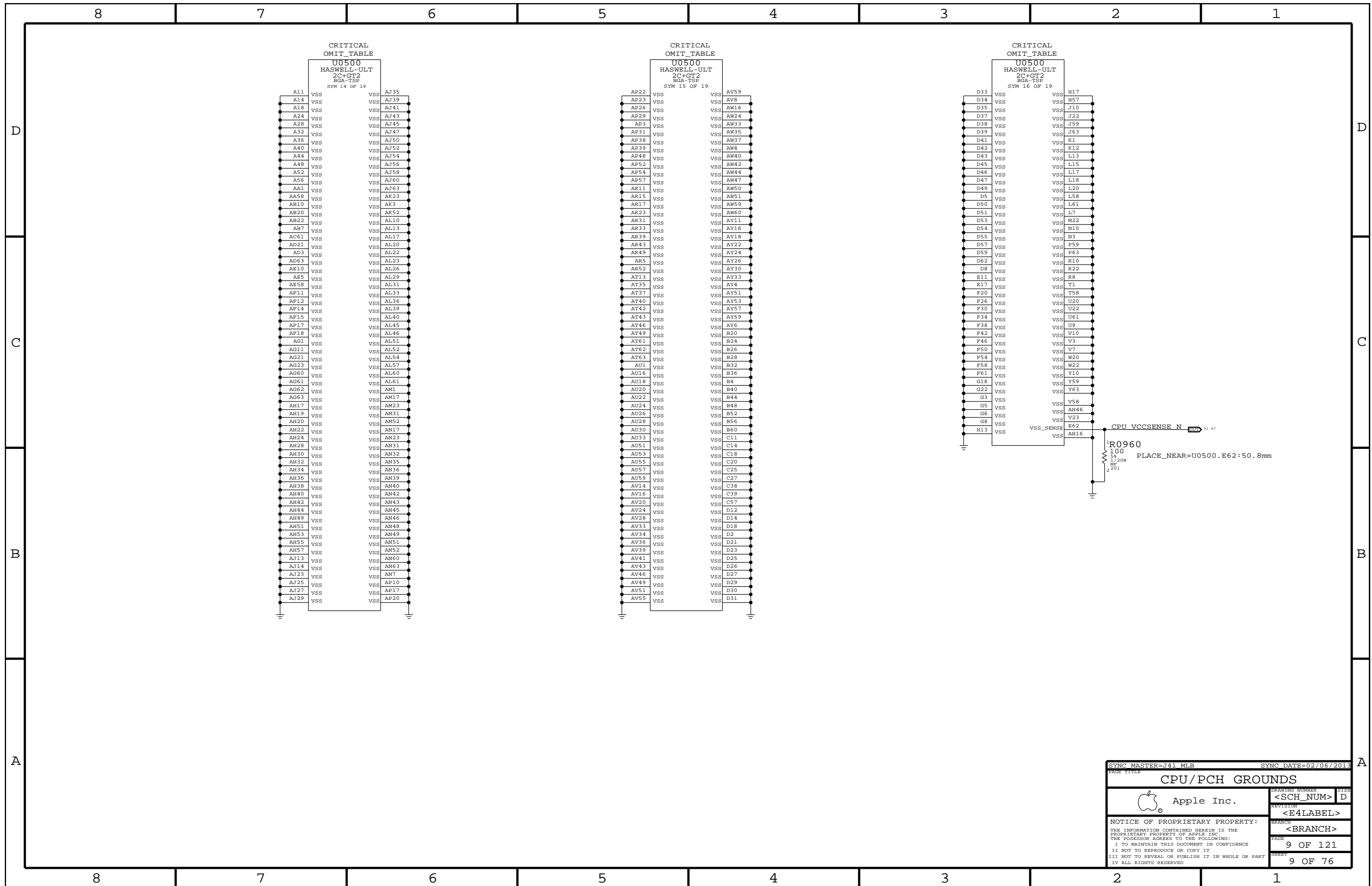
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CPU/PCH POWER

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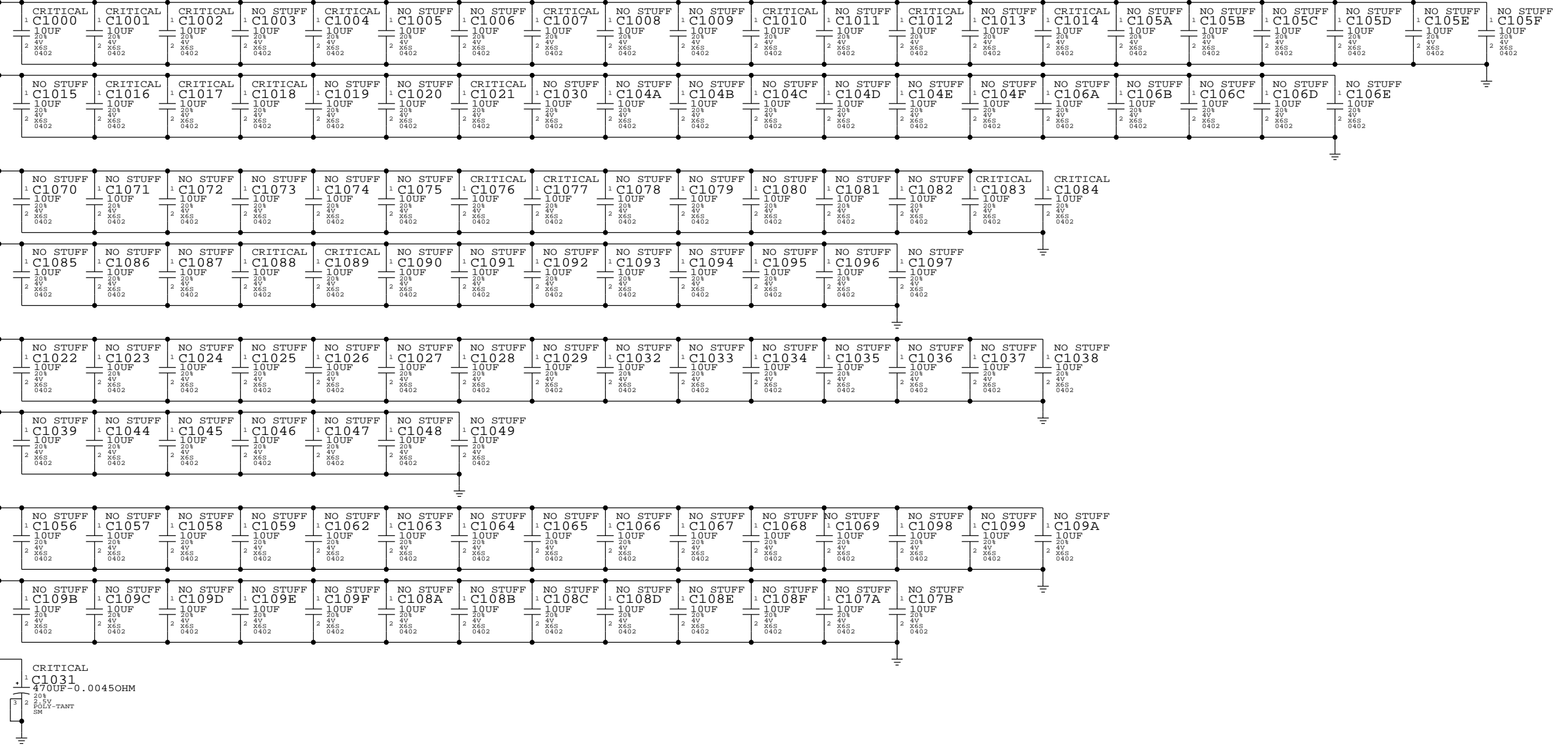
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CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
 Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

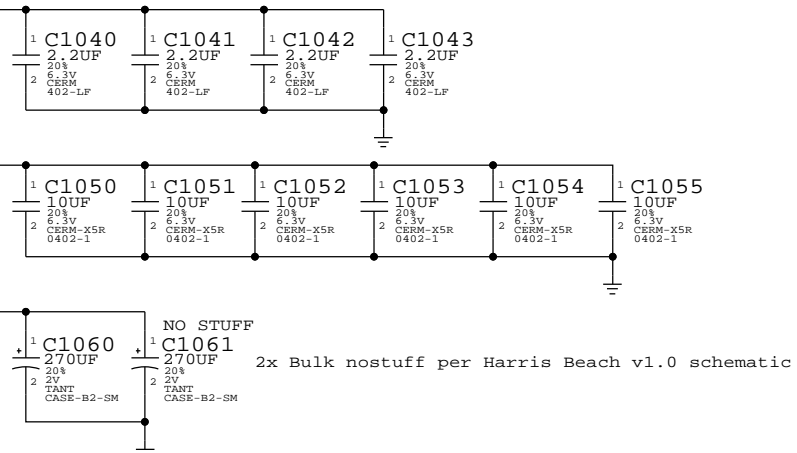
64 62 52 42 8 PPVCC_S0_CPU



CPU VDDQ DECOUPLING

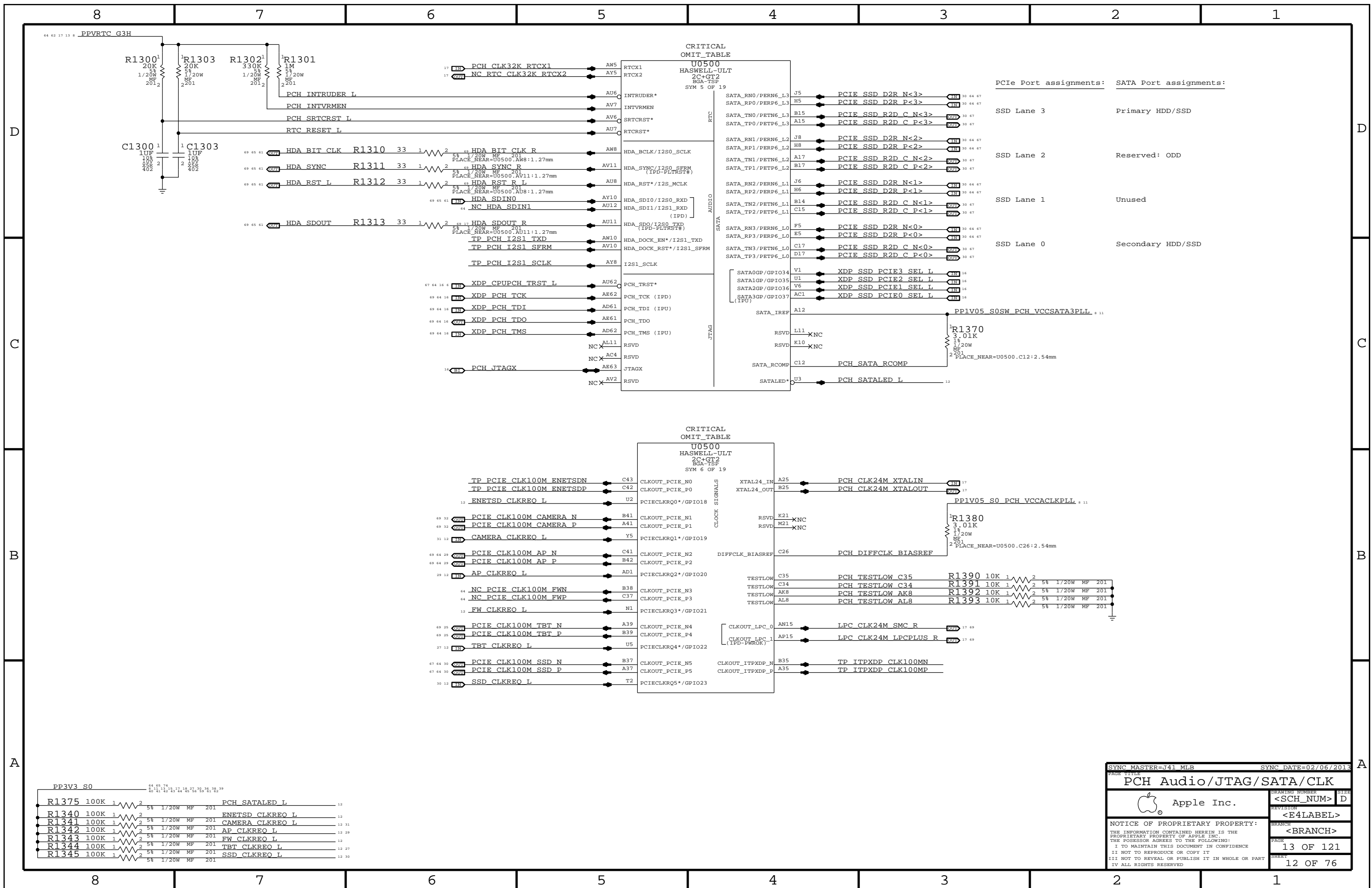
Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
 Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

42 PPVMEMIO_S0_CPU



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PCH Audio/JTAG/SATA/CLK

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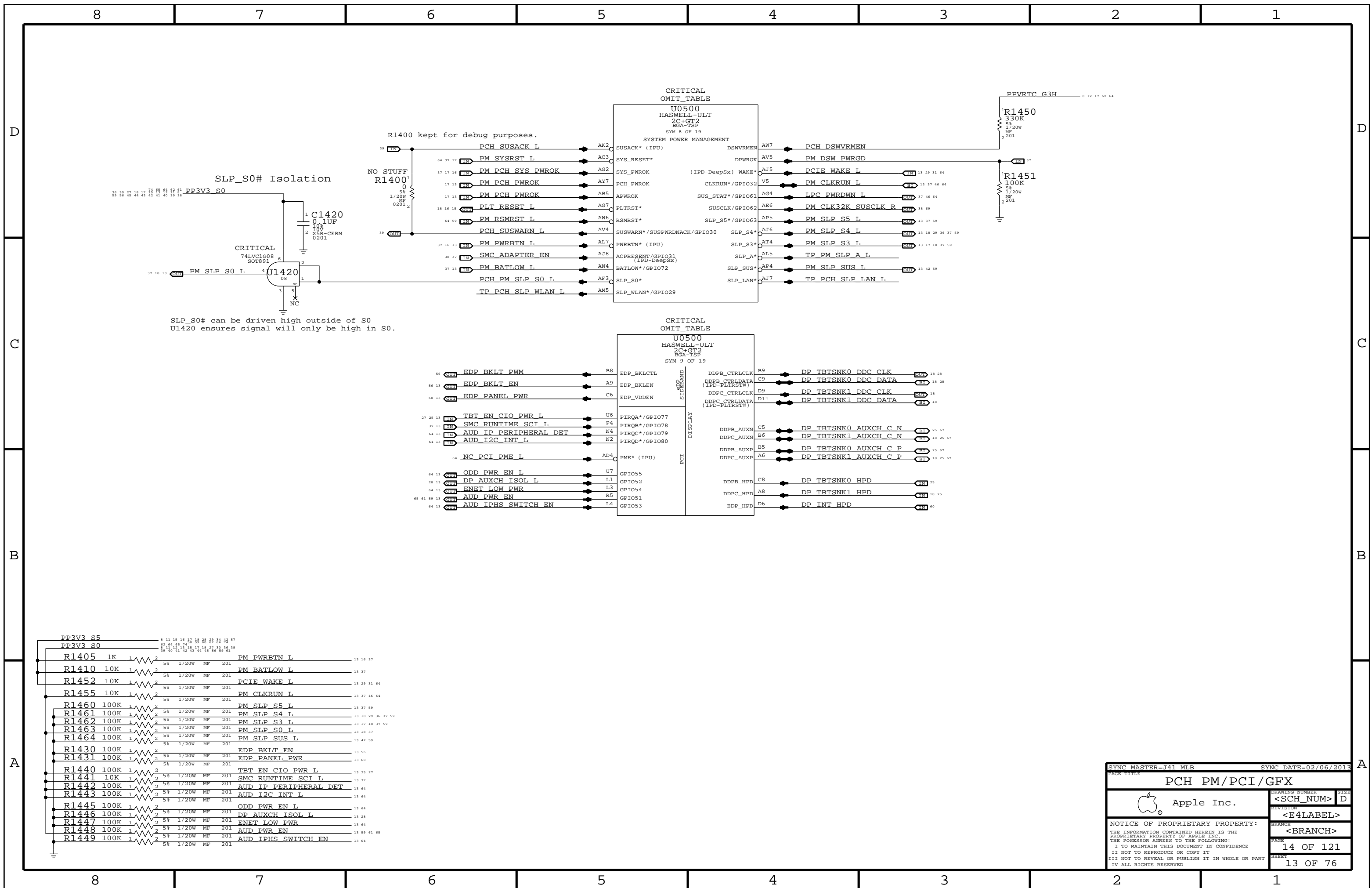
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SLP_S0# Isolation

SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.

CRITICAL OMIT_TABLE

U0500 HASWELL-ULT
2C+GT2 BGA-TSP
SYM 8 OF 19

SYSTEM POWER MANAGEMENT

AK2	SUSACK* (IPU)	DSWVRMEN	AW7	PCH_DSWVRMEN
AC3	SYS_RESET*	DPWROR	AV5	PM_DSW_PWRGD
AG2	SYS_PWROK	(IPD-DeepSx) WAKE*	AJ5	PCIE_WAKE_L
AY7	PCH_PWROK	CLKRUN*/GPIO32	V5	PM_CLKRUN_L
AB5	APWROR	SUS_STAT*/GPIO61	AG4	LPC_PWRDWN_L
AG7	PLTRST*	SUSCLK*/GPIO62	AE6	PM_CLK32K_SUSCLK_R
AW6	RSMRST*	SLP_S5*/GPIO63	AP5	PM_SLP_S5_L
AV4	SUSWARN*/SUSPWRDNACK*/GPIO30	SLP_S4*	AJ6	PM_SLP_S4_L
AL7	PWRBTN* (IPU)	SLP_S3*	AT4	PM_SLP_S3_L
AJ8	ACPRESENT*/GPIO31 (IPD-DeepSx)	SLP_A*	AL5	TP_PM_SLP_A_L
AN4	BATLOW*/GPIO72	SLP_SUS*	AP4	PM_SLP_SUS_L
AF2	SLP_S0*	SLP_LAN*	AJ7	TP_PCH_SLP_LAN_L
AM5	SLP_WLAN*/GPIO29			

CRITICAL OMIT_TABLE

U0500 HASWELL-ULT
2C+GT2 BGA-TSP
SYM 9 OF 19

B8	EDP_BKLT_PWM	EDP_BKLTCTL	B9	DP_TBTSNK0_DDC_CLK	18 28
A9	EDP_BKLT_EN	EDP_BKLEN	C9	DP_TBTSNK0_DDC_DATA	18 28
C6	EDP_PANEL_PWR	EDP_VDDEN	D9	DP_TBTSNK1_DDC_CLK	18
U6	TBT_EN_CIO_PWR_L	PIRQA*/GPIO77	D11	DP_TBTSNK1_DDC_DATA	18
P4	SMC_RUNTIME_SCI_L	PIRQB*/GPIO78	C5	DP_TBTSNK0_AUXCH_C_N	25 67
N4	AUD_IP_PERIPHERAL_DET	PIRQC*/GPIO79	B6	DP_TBTSNK1_AUXCH_C_N	18 25 67
N2	AUD_I2C_INT_L	PIRQD*/GPIO80	B5	DP_TBTSNK0_AUXCH_C_P	25 67
AD4	NC_PCI_PME_L	PME* (IPU)	A6	DP_TBTSNK1_AUXCH_C_P	18 25 67
U7	ODD_PWR_EN_L	GPIO55	C8	DP_TBTSNK0_HPD	25
L1	DP_AUXCH_ISOL_L	GPIO52	A8	DP_TBTSNK1_HPD	18 25
L3	ENET_LOW_PWR	GPIO54	D6	DP_INT_HPD	25
R5	AUD_PWR_EN	GPIO51			
L4	AUD_IPHS_SWITCH_EN	GPIO53			

PP3V3 S5	11 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57
PP3V3 S0	62 64 65 74
R1405 1K	1 2 5% 1/20W MF 201 13 16 37
R1410 10K	1 2 5% 1/20W MF 201 13 37
R1452 10K	1 2 5% 1/20W MF 201 13 29 31 64
R1455 10K	1 2 5% 1/20W MF 201 13 37 46 64
R1460 100K	1 2 5% 1/20W MF 201 13 37 59
R1461 100K	1 2 5% 1/20W MF 201 13 18 29 36 37 59
R1462 100K	1 2 5% 1/20W MF 201 13 17 18 37 59
R1463 100K	1 2 5% 1/20W MF 201 13 18 37
R1464 100K	1 2 5% 1/20W MF 201 13 42 59
R1430 100K	1 2 5% 1/20W MF 201 13 56
R1431 100K	1 2 5% 1/20W MF 201 13 60
R1440 100K	1 2 5% 1/20W MF 201 13 25 27
R1441 10K	1 2 5% 1/20W MF 201 13 37
R1442 100K	1 2 5% 1/20W MF 201 13 64
R1443 100K	1 2 5% 1/20W MF 201 13 64
R1445 100K	1 2 5% 1/20W MF 201 13 64
R1446 100K	1 2 5% 1/20W MF 201 13 28
R1447 100K	1 2 5% 1/20W MF 201 13 64
R1448 100K	1 2 5% 1/20W MF 201 13 59 61 65
R1449 100K	1 2 5% 1/20W MF 201 13 64

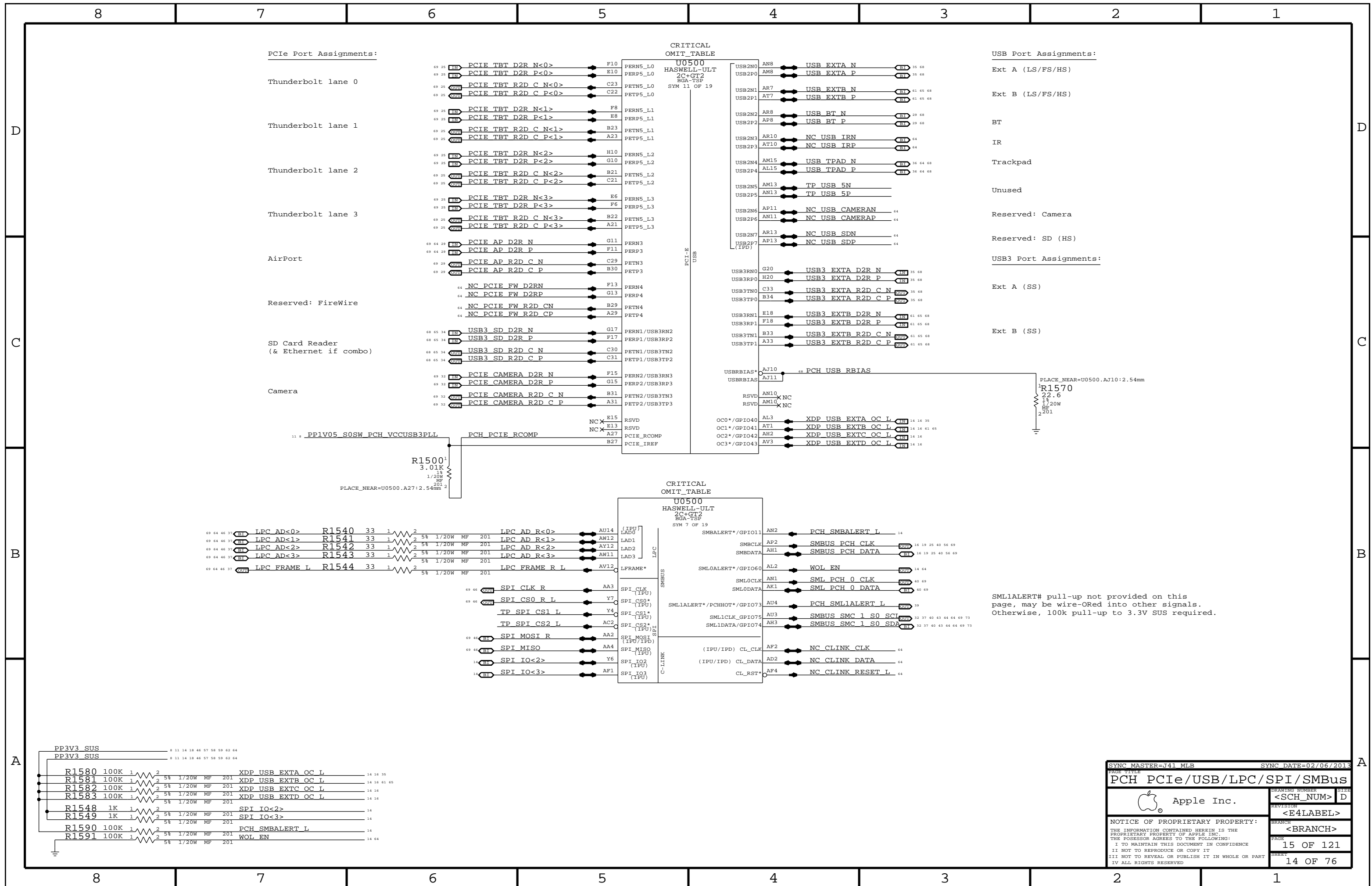
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PCH PM/PCI/GFX

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PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader (& Ethernet if combo)

Camera

CRITICAL OMIT_TABLE

U0500 HASWELL-ULT
2C+GT2 BGA-TSE
SYM 11 OF 19

PERN5_L0	F10	PERN5_L0
PERP5_L0	E10	PERP5_L0
PETN5_L0	C23	PETN5_L0
PETP5_L0	C22	PETP5_L0
PERN5_L1	F8	PERN5_L1
PERP5_L1	E8	PERP5_L1
PETN5_L1	B23	PETN5_L1
PETP5_L1	A23	PETP5_L1
PERN5_L2	H10	PERN5_L2
PERP5_L2	G10	PERP5_L2
PETN5_L2	B21	PETN5_L2
PETP5_L2	C21	PETP5_L2
PERN5_L3	E6	PERN5_L3
PERP5_L3	F6	PERP5_L3
PETN5_L3	B22	PETN5_L3
PETP5_L3	A21	PETP5_L3
PERN3	G11	PERN3
PERP3	F11	PERP3
PETN3	C29	PETN3
PETP3	B30	PETP3
PERN4	F13	PERN4
PERP4	G13	PERP4
PETN4	B29	PETN4
PETP4	A29	PETP4
PERN1/USB3RN2	G17	PERN1/USB3RN2
PERP1/USB3RP2	F17	PERP1/USB3RP2
PETN1/USB3TN2	C30	PETN1/USB3TN2
PETP1/USB3TP2	C31	PETP1/USB3TP2
PERN2/USB3RN3	F15	PERN2/USB3RN3
PERP2/USB3RP3	G15	PERP2/USB3RP3
PETN2/USB3TN3	B31	PETN2/USB3TN3
PETP2/USB3TP3	A31	PETP2/USB3TP3
RSVD	E15	RSVD
RSVD	E13	RSVD
PCIE_RCOMP	A27	PCIE_RCOMP
PCIE_IREF	B27	PCIE_IREF

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

SYNC MASTER=J41 MLB SYNC DATE=02/06/2013

PCH PCIe/USB/LPC/SPI/SMBus

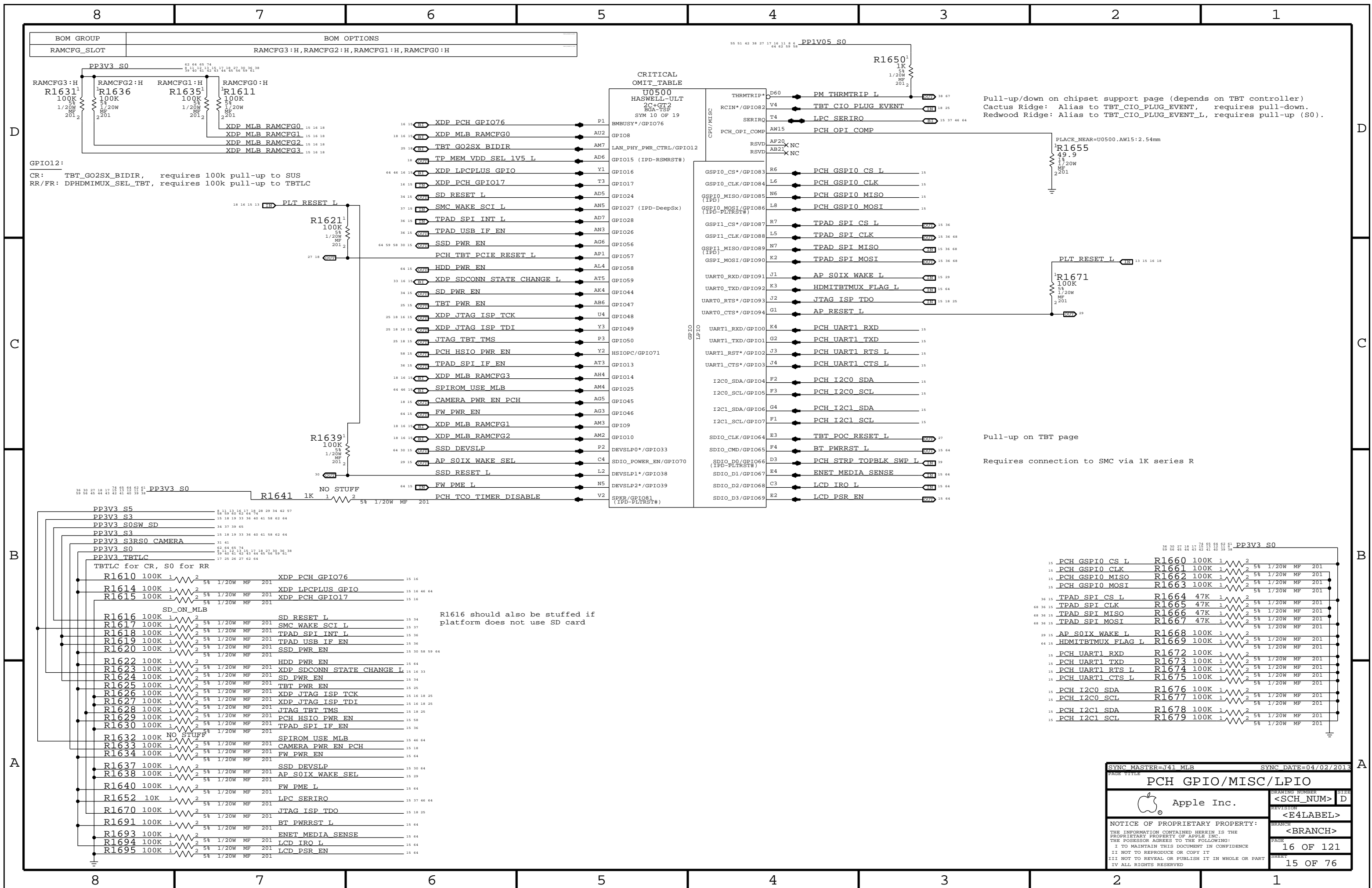
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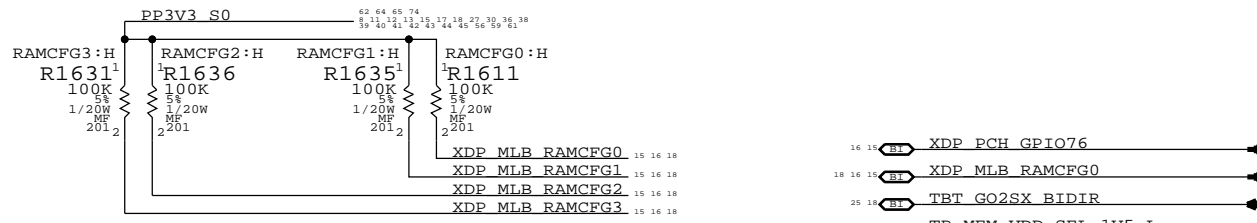
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PP3V3 SUS

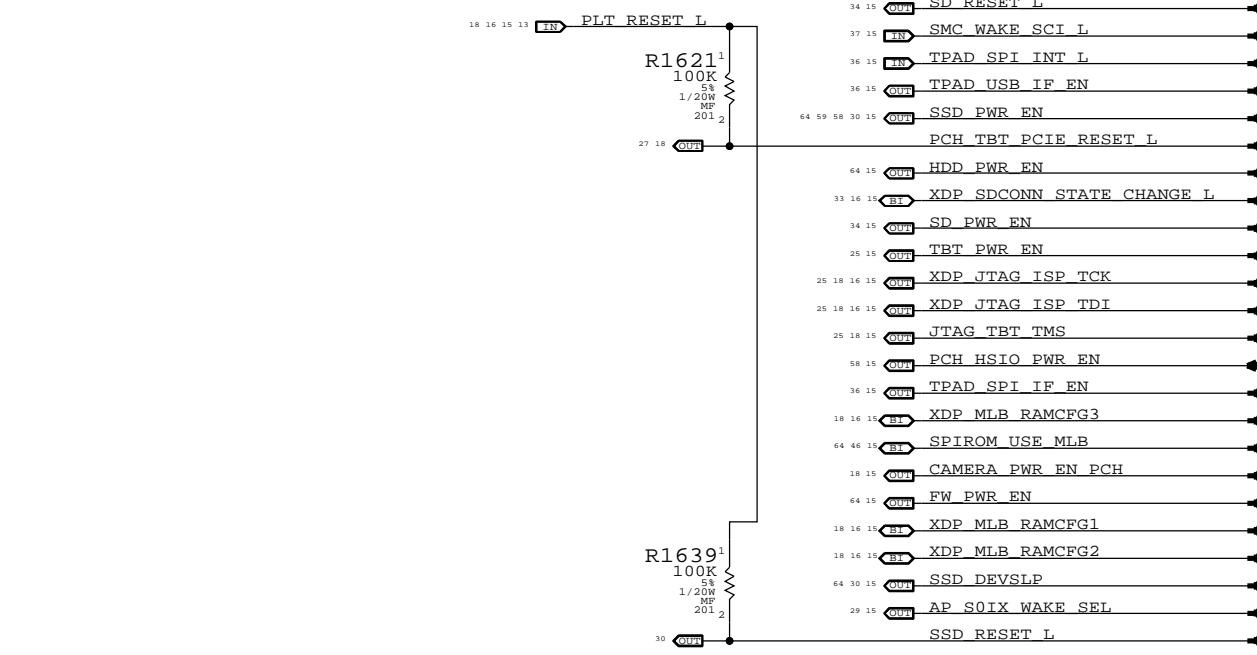
R1580	100K	1	2	XDP USB EXTA OC L	14 16 35
R1581	100K	1	2	XDP USB EXTB OC L	14 16 61 65
R1582	100K	1	2	XDP USB EXTC OC L	14 16
R1583	100K	1	2	XDP USB EXTD OC L	14 16
R1548	1K	1	2	SPI IO<2>	14
R1549	1K	1	2	SPI IO<3>	14
R1590	100K	1	2	PCH SMBALERT L	14
R1591	100K	1	2	WOL EN	14 64



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H



GPIO12:
 CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUB
 RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to BTLC



Component	Value	Power	Temp	Part	Pin
R1610	100K	5%	1/20W MF	201	XDP PCH GPIO76
R1614	100K	5%	1/20W MF	201	XDP LPCPLUS GPIO
R1615	100K	5%	1/20W MF	201	XDP PCH GPIO17
R1616	100K	5%	1/20W MF	201	SD RESET L
R1617	100K	5%	1/20W MF	201	SMC WAKE SCI L
R1618	100K	5%	1/20W MF	201	TPAD SPI INT L
R1619	100K	5%	1/20W MF	201	TPAD USB IF EN
R1620	100K	5%	1/20W MF	201	SSD PWR EN
R1622	100K	5%	1/20W MF	201	HDD PWR EN
R1623	100K	5%	1/20W MF	201	XDP SDCONN STATE CHANGE L
R1624	100K	5%	1/20W MF	201	SD PWR EN
R1625	100K	5%	1/20W MF	201	TBT PWR EN
R1626	100K	5%	1/20W MF	201	XDP JTAG ISP TCK
R1627	100K	5%	1/20W MF	201	XDP JTAG ISP TDI
R1628	100K	5%	1/20W MF	201	JTAG TBT TMS
R1629	100K	5%	1/20W MF	201	PCH HSIO PWR EN
R1630	100K	5%	1/20W MF	201	TPAD SPI IF EN
R1632	100K	NO STUFF			SPIROM USE MLB
R1633	100K	5%	1/20W MF	201	CAMERA PWR EN PCH
R1634	100K	5%	1/20W MF	201	FW PWR EN
R1637	100K	5%	1/20W MF	201	SSD DEVS LP
R1638	100K	5%	1/20W MF	201	AP SOIX WAKE SEL
R1640	100K	5%	1/20W MF	201	FW PME L
R1652	10K	5%	1/20W MF	201	LPC SERIRO
R1670	100K	5%	1/20W MF	201	JTAG ISP TDO
R1691	100K	5%	1/20W MF	201	BT PWRST L
R1693	100K	5%	1/20W MF	201	ENET MEDIA SENSE
R1694	100K	5%	1/20W MF	201	LCD IRO L
R1695	100K	5%	1/20W MF	201	LCD PSR EN

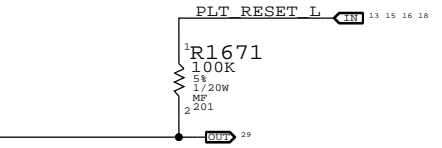
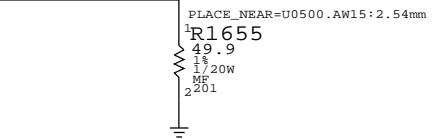
R1616 should also be stuffed if platform does not use SD card

CRITICAL OMIT TABLE

Component	Pin
U0500 HASWELL-ULT	2C+CT2 BGA-TSP SYM 10 OF 19
BMBUSY*/GPIO76	P1
GPIO8	AU2
LAN_PHY_PWR_CTRL/GPIO12	AM7
GPIO15 (IPD-RSMRST#)	AD6
GPIO16	Y1
GPIO17	T3
GPIO24	AD5
GPIO27 (IPD-DeepSx)	AN5
GPIO28	AD7
GPIO26	AN3
GPIO56	AG6
GPIO57	AP1
GPIO58	AL4
GPIO59	AT5
GPIO44	AK4
GPIO47	AB6
GPIO48	U4
GPIO49	Y3
GPIO50	P3
HSIOPC/GPIO71	Y2
GPIO13	AT3
GPIO14	AH4
GPIO25	AM4
GPIO45	AG5
GPIO46	AG3
GPIO9	AM3
GPIO10	AM2
DEVS LP0*/GPIO33	P2
SDIO_POWER_EN/GPIO70	C4
DEVS LP1*/GPIO38	L2
DEVS LP2*/GPIO39	N5
SPKR/GPIO81 (IPD-PLTRST#)	V2

Component	Pin
THRMRTRIP*	D60
RCIN*/GPIO82	V4
SERIRQ	T4
PCH_OPI_COMP	AW15
RSVD	AF20
RSVD	AB21
GPIO83	R6
GPIO84	L6
GPIO85	N6
GPIO86 (IPD-PLTRST#)	L8
GPIO87	R7
GPIO88	L5
GPIO89	N7
GPIO90	K2
UART0_RXD/GPIO91	J1
UART0_TXD/GPIO92	K3
UART0_RTS*/GPIO93	J2
UART0_CTS*/GPIO94	G1
UART1_RXD/GPIO100	K4
UART1_TXD/GPIO101	G2
UART1_RST*/GPIO102	J3
UART1_CTS*/GPIO103	J4
I2C0_SDA/GPIO104	F2
I2C0_SCL/GPIO105	F3
I2C1_SDA/GPIO106	G4
I2C1_SCL/GPIO107	F1
SDIO_CLK/GPIO104	E3
SDIO_CMD/GPIO105	F4
SDIO_D0/GPIO106 (IPD-PLTRST#)	D3
SDIO_D1/GPIO107	E4
SDIO_D2/GPIO108	C3
SDIO_D3/GPIO109	E2
PCH GSPI0 CS L	15
PCH GSPI0 CLK	15
PCH GSPI0 MISO	15
PCH GSPI0 MOSI	15
TPAD SPI CS L	15 36
TPAD SPI CLK	15 36 68
TPAD SPI MISO	15 36 68
TPAD SPI MOSI	15 36 68
AP SOIX WAKE L	15 29
HDMITBTMUX FLAG L	15 64
JTAG ISP TDO	15 18 25
AP RESET L	15 18 25
PCH UART1 RXD	15
PCH UART1 TXD	15
PCH UART1 RTS L	15
PCH UART1 CTS L	15
PCH I2C0 SDA	15
PCH I2C0 SCL	15
PCH I2C1 SDA	15
PCH I2C1 SCL	15
TBT POC RESET L	27
BT PWRST L	15 64
PCH STRP TOPBLK SWP L	39
ENET MEDIA SENSE	15 64
LCD IRO L	15 64
LCD PSR EN	15 64

Pull-up/down on chipset support page (depends on TBT controller)
 Cactus Ridge: Alias to TBT_CIO_PLUGIN_EVENT, requires pull-down.
 Redwood Ridge: Alias to TBT_CIO_PLUGIN_EVENT_L, requires pull-up (S0).



Pull-up on TBT page

Requires connection to SMC via 1K series R

Component	Value	Power	Temp	Part	Pin
R1660	100K	5%	1/20W MF	201	PCH GSPI0 CS L
R1661	100K	5%	1/20W MF	201	PCH GSPI0 CLK
R1662	100K	5%	1/20W MF	201	PCH GSPI0 MISO
R1663	100K	5%	1/20W MF	201	PCH GSPI0 MOSI
R1664	47K	5%	1/20W MF	201	TPAD SPI CS L
R1665	47K	5%	1/20W MF	201	TPAD SPI CLK
R1666	47K	5%	1/20W MF	201	TPAD SPI MISO
R1667	47K	5%	1/20W MF	201	TPAD SPI MOSI
R1668	100K	5%	1/20W MF	201	AP SOIX WAKE L
R1669	100K	5%	1/20W MF	201	HDMITBTMUX FLAG L
R1672	100K	5%	1/20W MF	201	PCH UART1 RXD
R1673	100K	5%	1/20W MF	201	PCH UART1 TXD
R1674	100K	5%	1/20W MF	201	PCH UART1 RTS L
R1675	100K	5%	1/20W MF	201	PCH UART1 CTS L
R1676	100K	5%	1/20W MF	201	PCH I2C0 SDA
R1677	100K	5%	1/20W MF	201	PCH I2C0 SCL
R1678	100K	5%	1/20W MF	201	PCH I2C1 SDA
R1679	100K	5%	1/20W MF	201	PCH I2C1 SCL

SYNC MASTER=J41 MLB	SYNC DATE=04/02/2013
PCH GPIO/MISC/LPIO	
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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System RTC Power Source & 32kHz / 25MHz Clock Generator

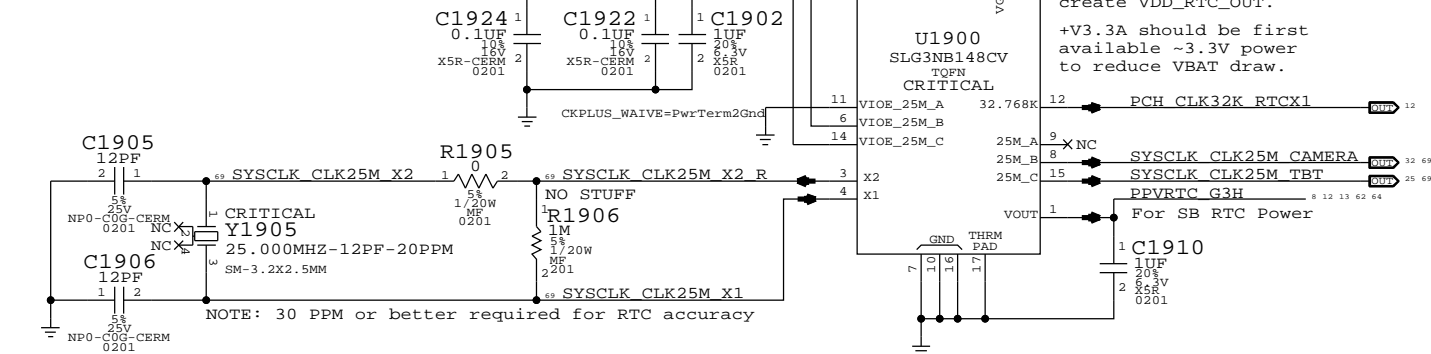
Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

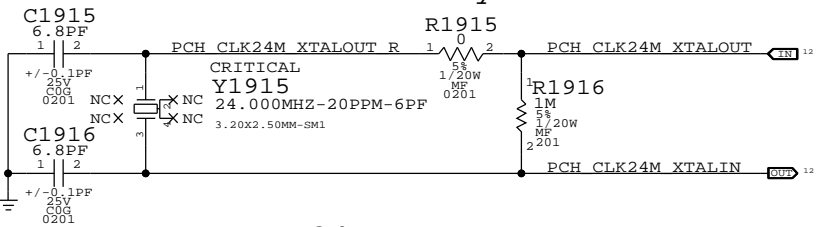
PP3V42 G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot
PP3V3 S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5

GreenCLK 25MHz Power Must be powered if any VDDIO is powered.

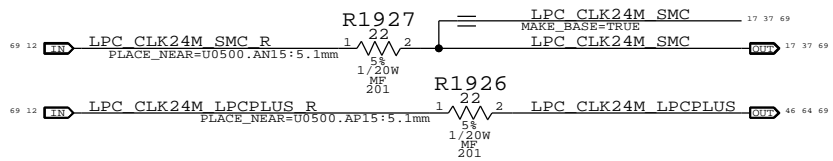
CAM XTAL Power
TBT XTAL Power



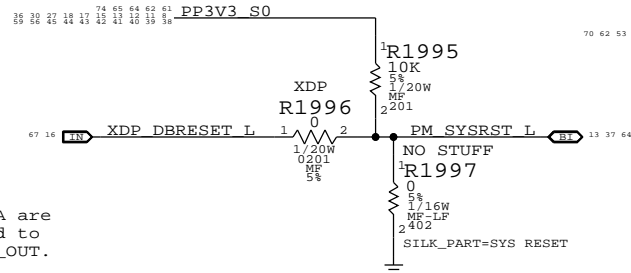
PCH 24MHz Crystal



PCH 24MHz Outputs

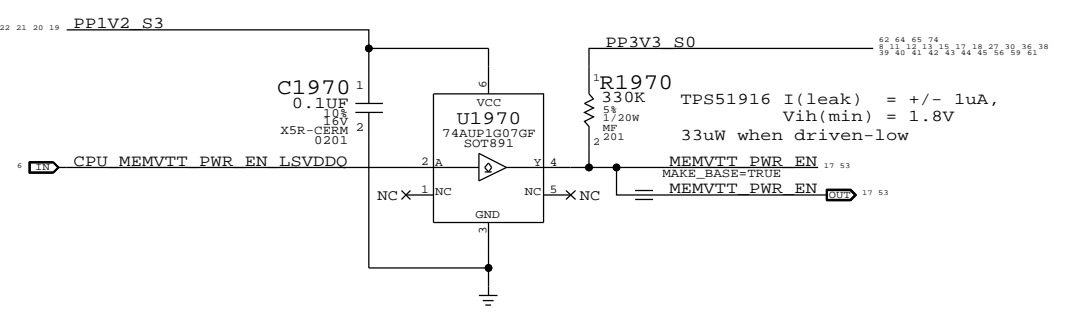


PCH Reset Button

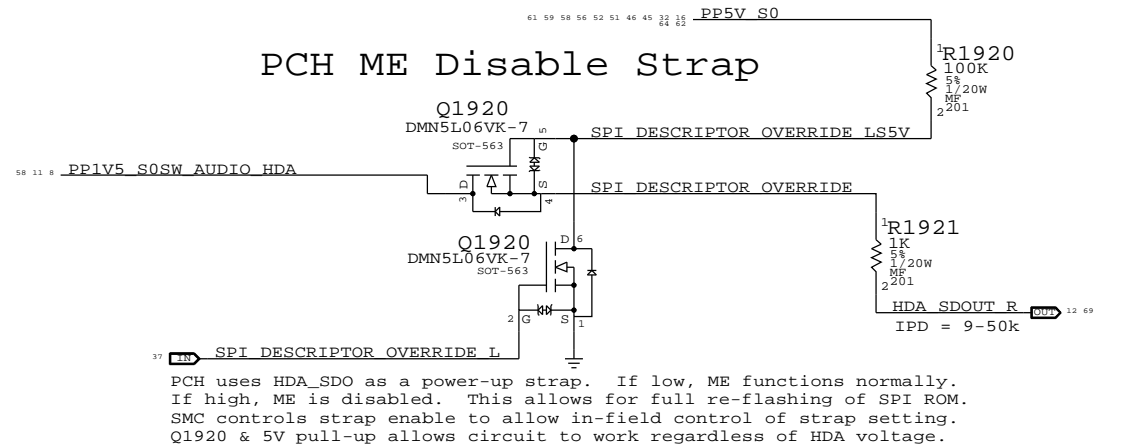


Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

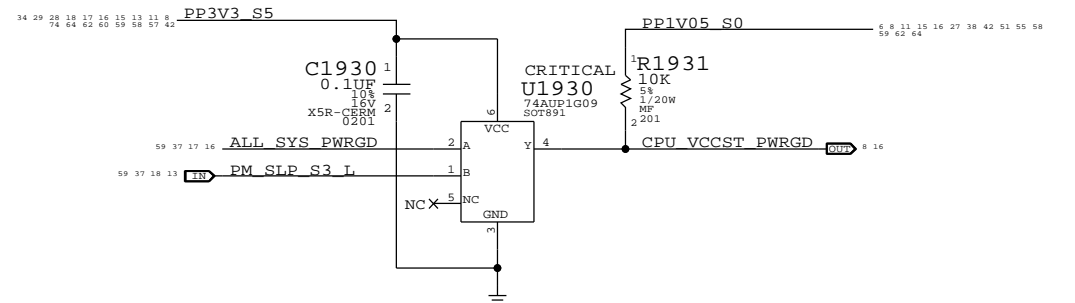


PCH ME Disable Strap

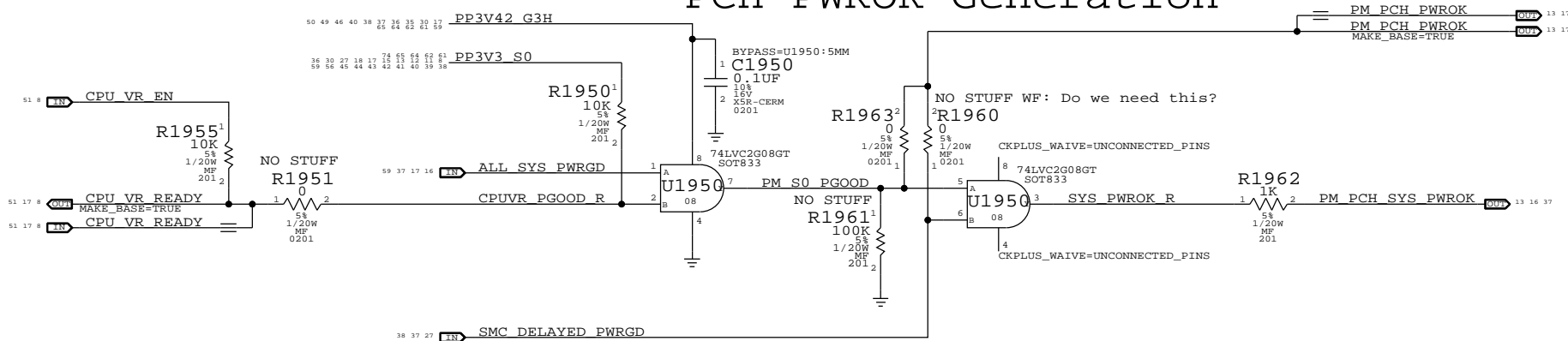


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

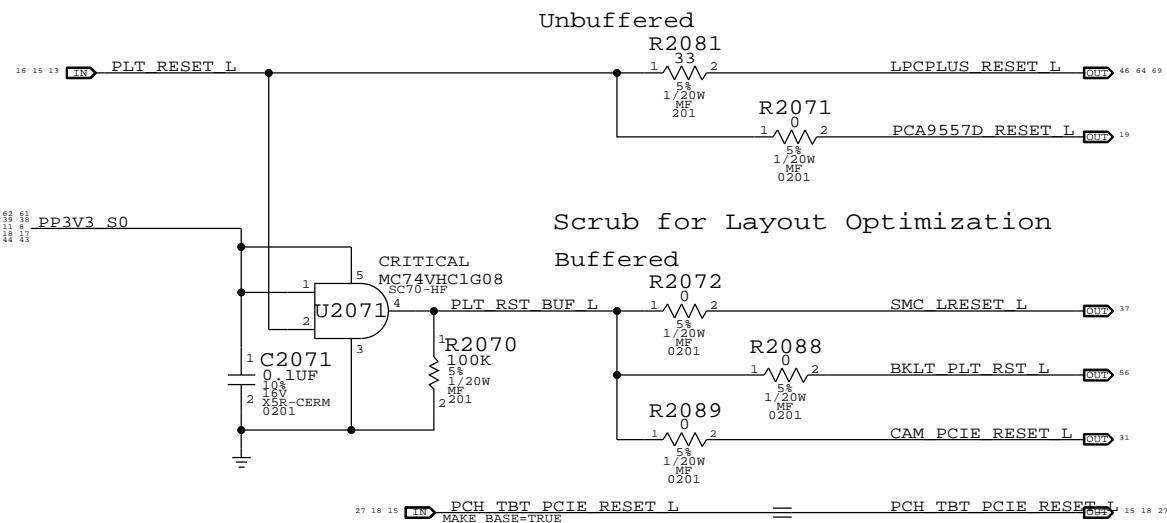


PCH PWROK Generation

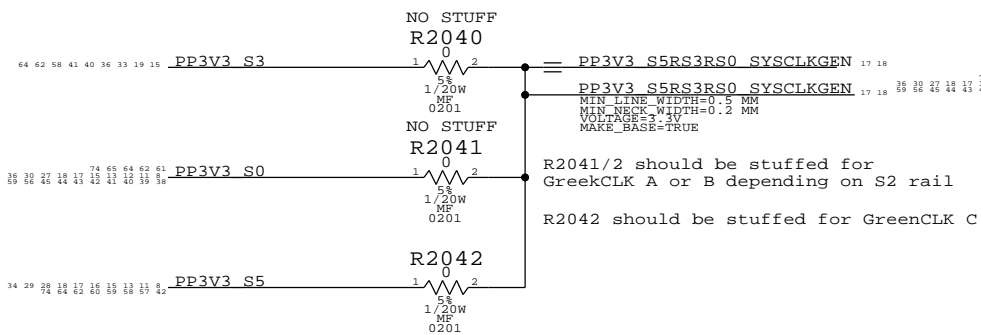


PAGE TITLE		SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
Chipset Support					
Apple Inc.		DRAWING NUMBER		SIZE	
		<SCH_NUM>		D	
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		PAGE		SHEET	
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Platform Reset Connections

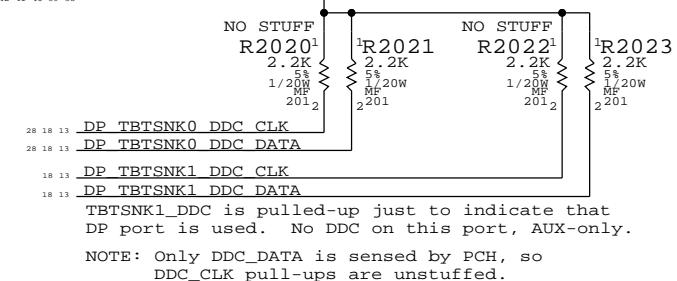


GreenCLK 25MHz Power



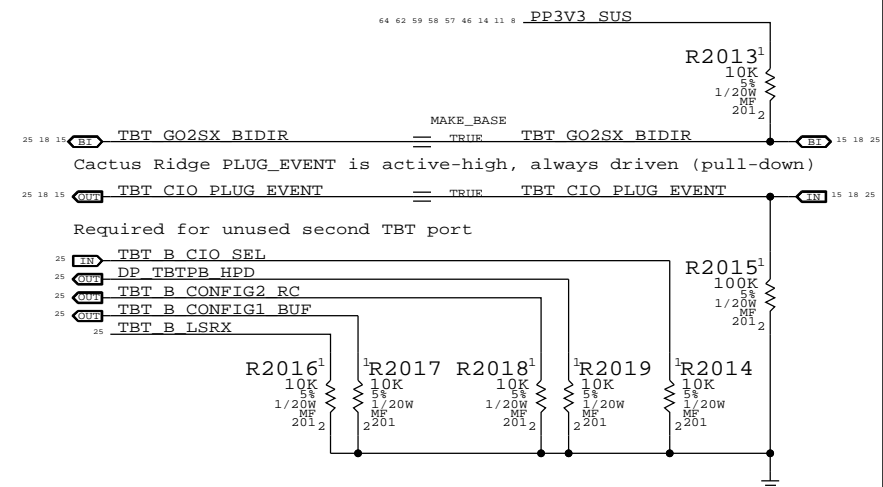
DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface. DP++ spec violation, should remove!



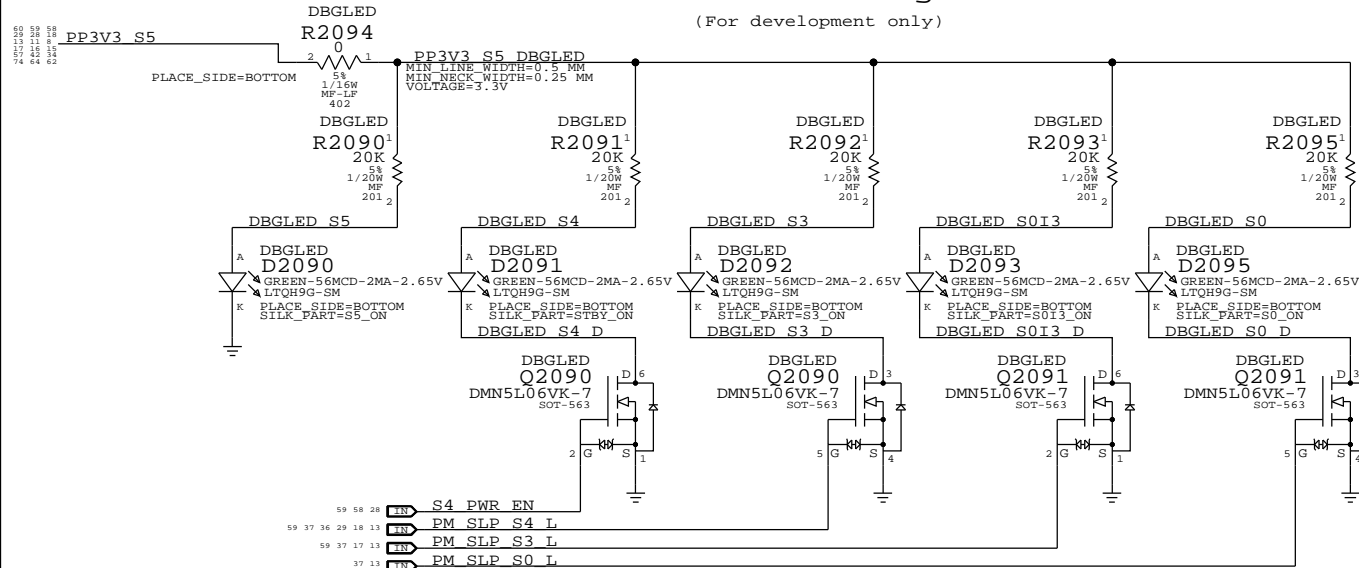
Thunderbolt Pull-up/downs

Cactus Ridge GO2SX signal pulled-up to SUS rail

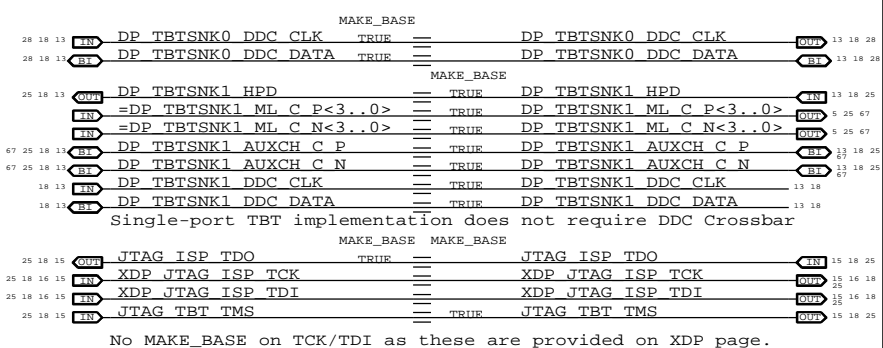


Power State Debug LEDs

(For development only)

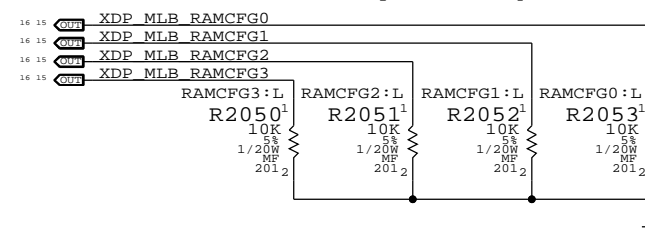


TBT Aliases

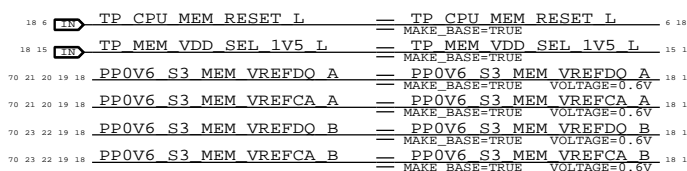


RAM Configuration Straps

Pull-downs for chip-down RAM systems



LPDDR3 Alias Support



SYNC MASTER=J41 MLB		SYNC DATE=02/15/2013	
Project Chipset Support			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

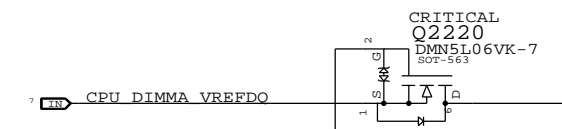
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining



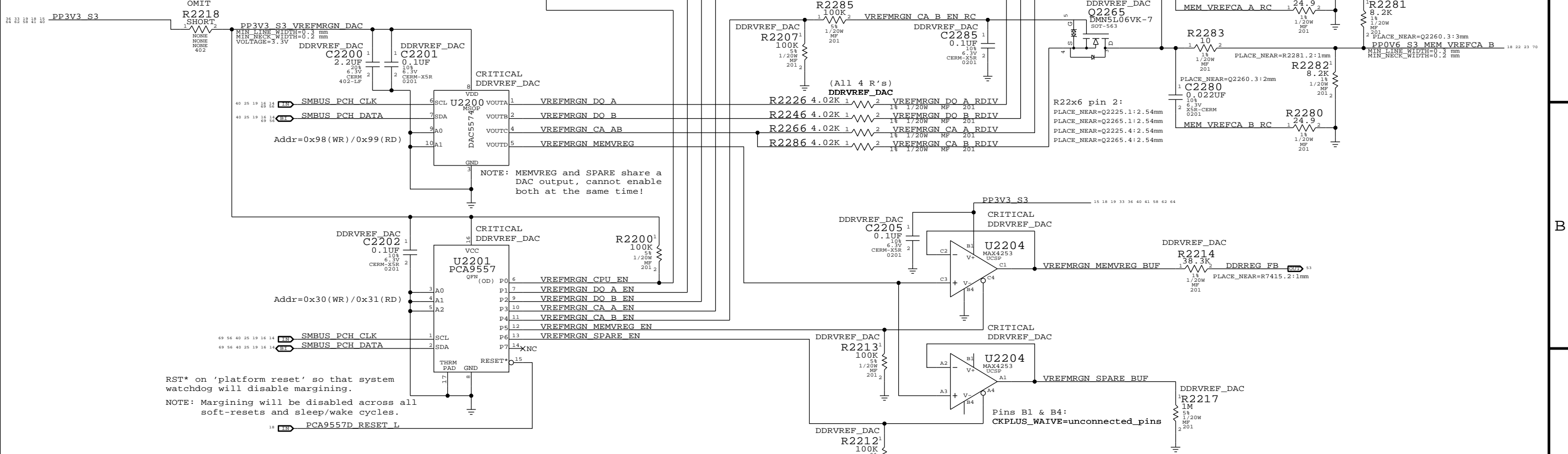
NOTE: CPU DAC output step sizes:
 DDR3 (1.5V) 7.70mV per step
 DDR3L (1.35V) 6.99mV per step
 LPDDR3 (1.2V) ???mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT



RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

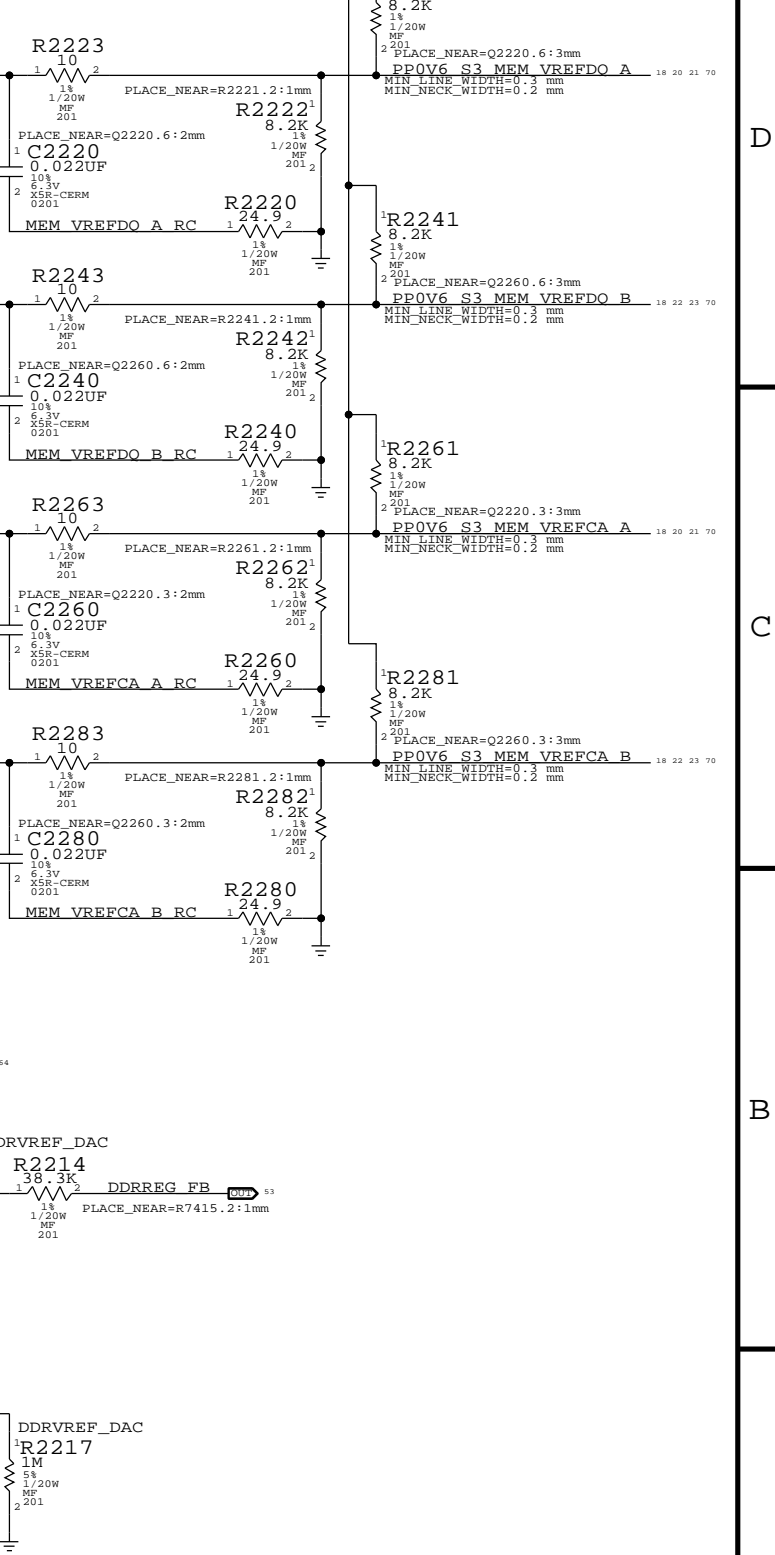
PCA9557D RESET L

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
Nominal value	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)
Margin target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)
Vref current:	+73uA - -73uA (= sourced)		+82uA - -82uA (= sourced)		+21uA - -21uA (= sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
 DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

VRef Dividers

Always used, regardless of margining option.



SYNC MASTER=J41 MLB SYNC DATE=02/12/2013

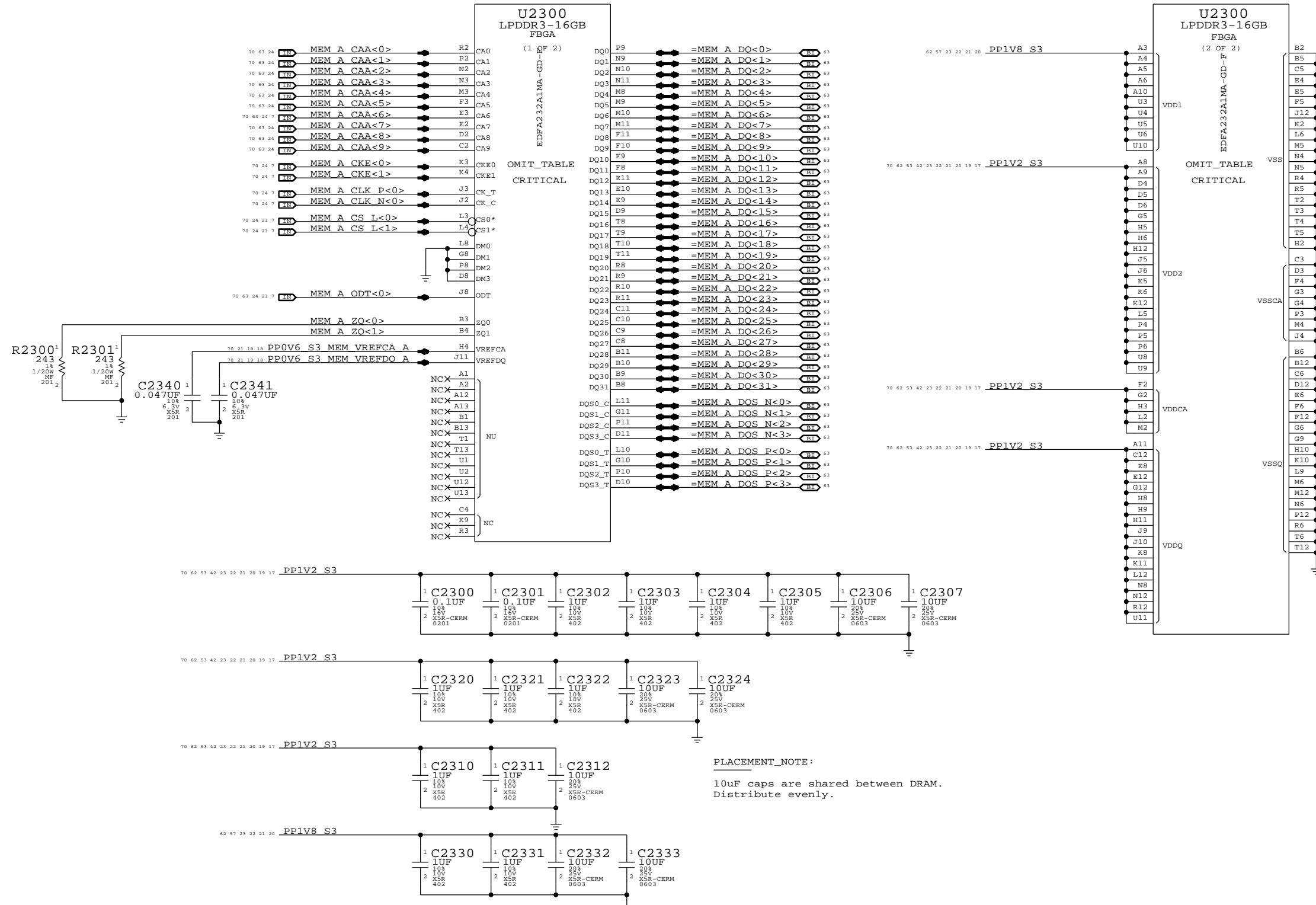
DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> D
 REVISION: <E4LABEL>
 BRANCH: <BRANCH>
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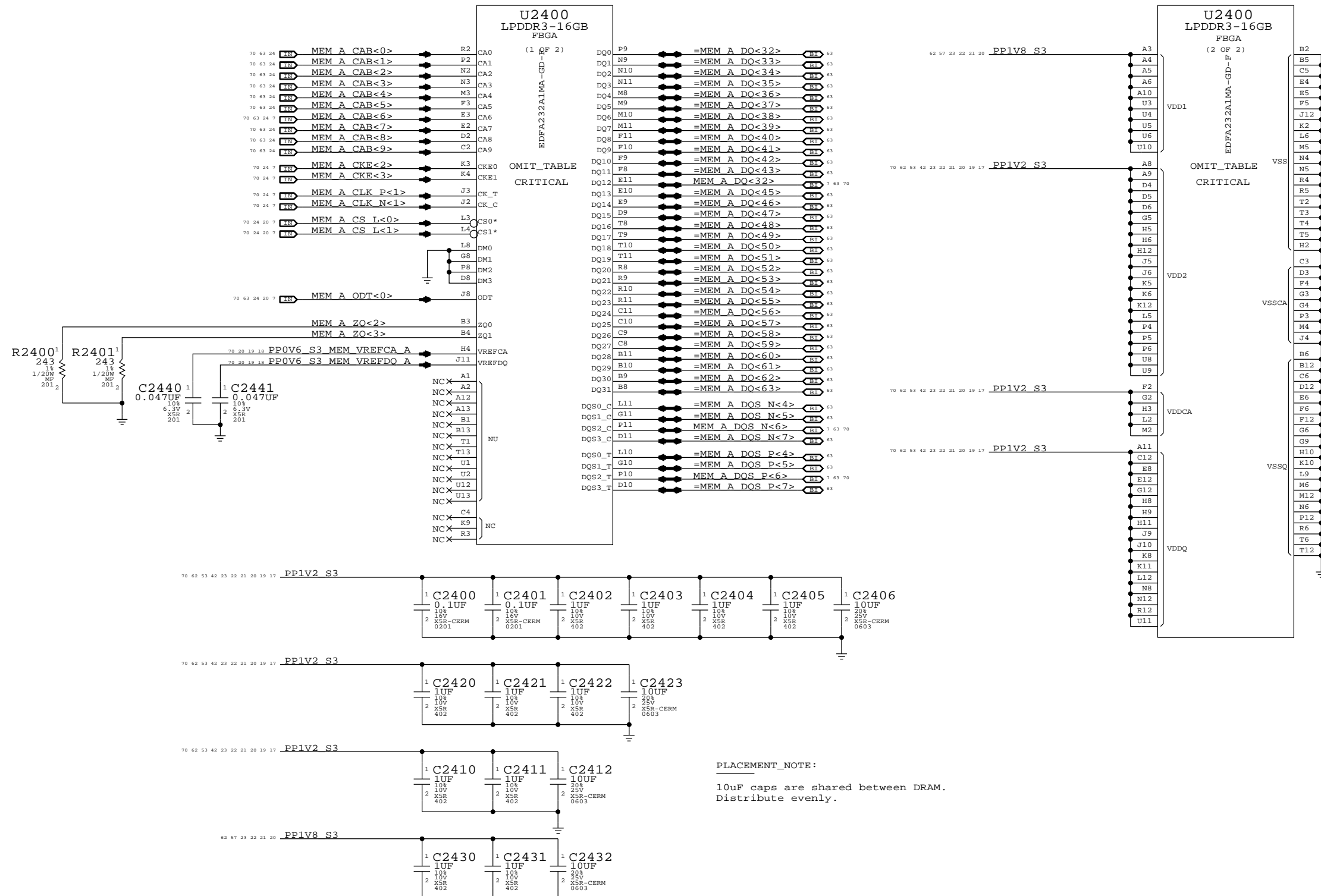
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LPDDR3 CHANNEL A (0-31)



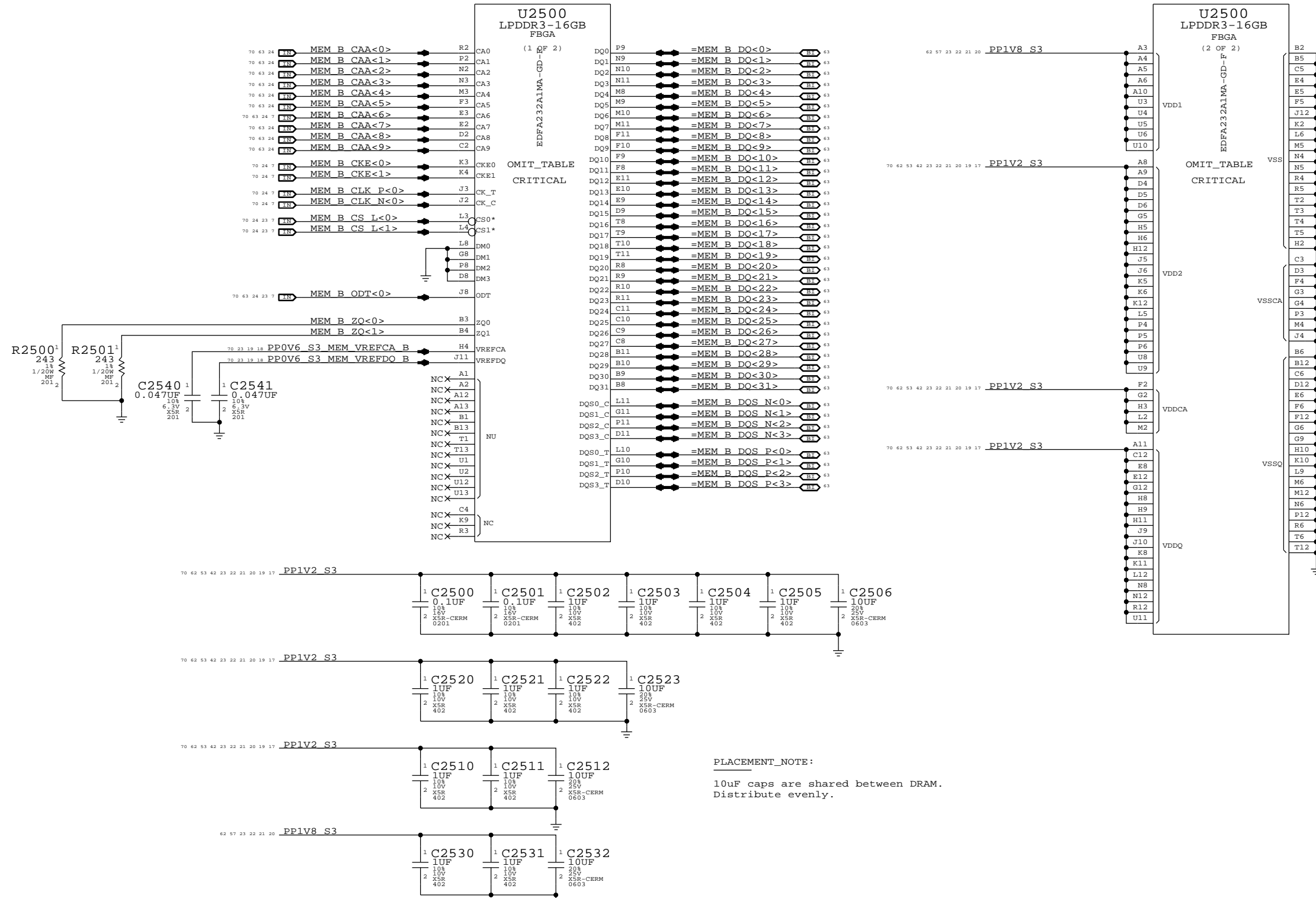
SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE LPDDR3 DRAM Channel A (0-31)			
DRAWING NUMBER Apple Inc.		DRAWING NUMBER <SCH_NUM>	SIZE D
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LPDDR3 CHANNEL A (32-63)



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PAGE TITLE LPDDR3 DRAM Channel A (32-63)			
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REVISION <E4LABEL>		BRANCH <BRANCH>	
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LPDDR3 CHANNEL B (0-31)

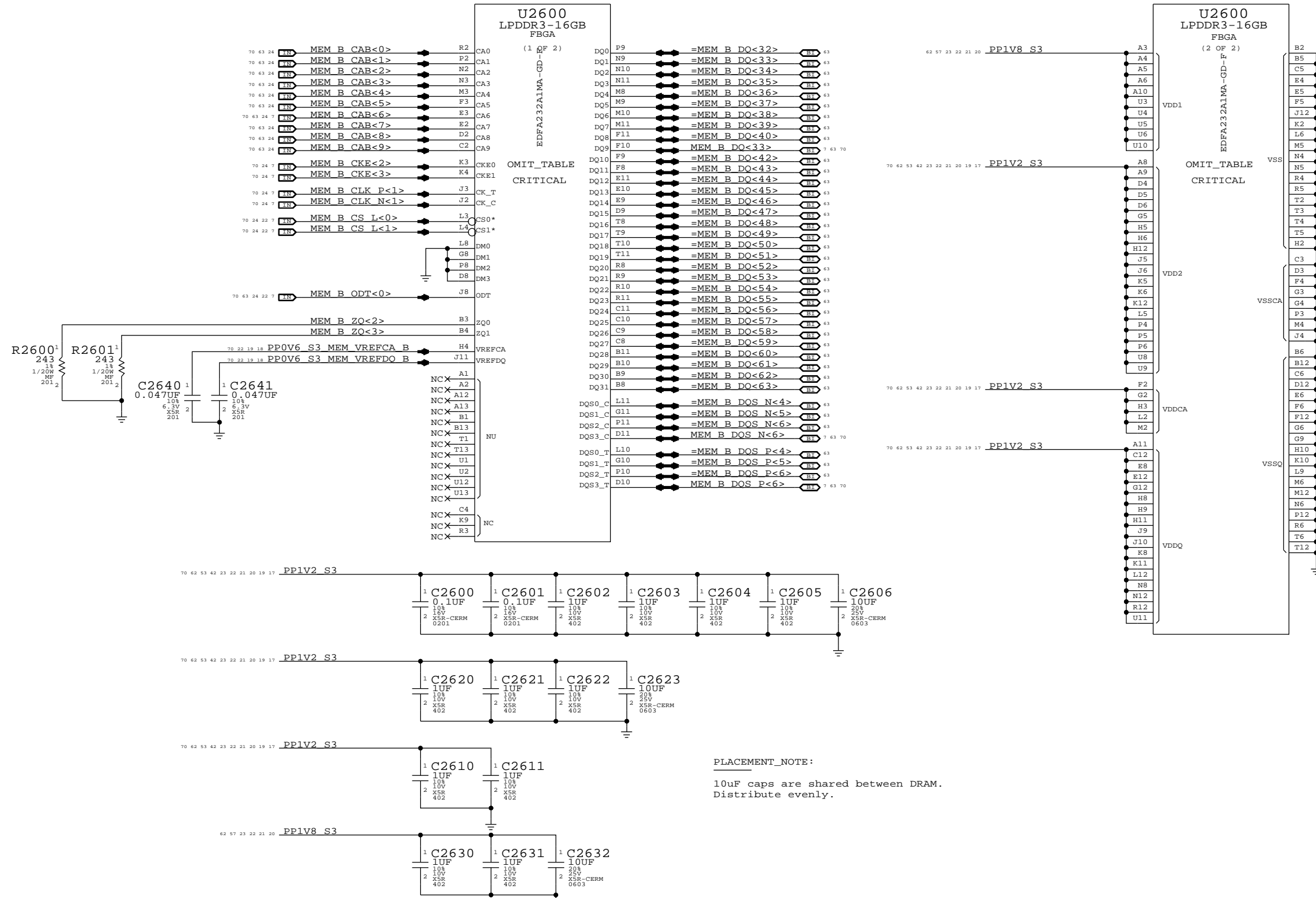


PLACEMENT_NOTE:
 10uF caps are shared between DRAM.
 Distribute evenly.

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE LPDDR3 DRAM Channel B (0-31)			
DRAWING NUMBER <SCH_NUM>		SIZE D	
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LPDDR3 CHANNEL B (32-63)

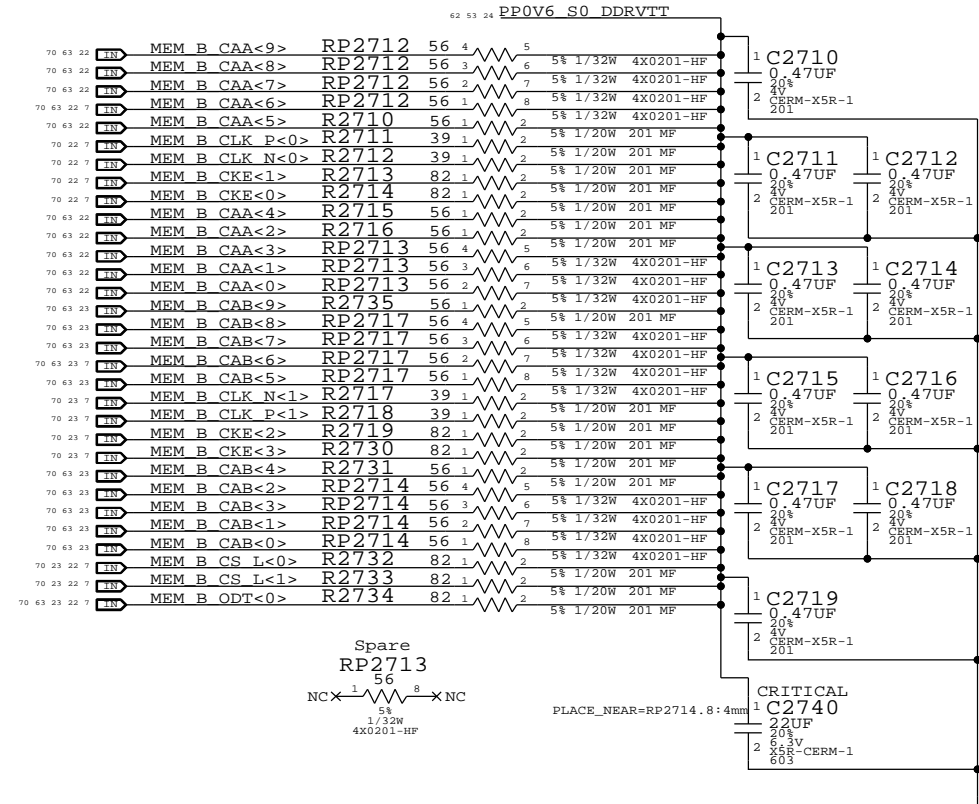
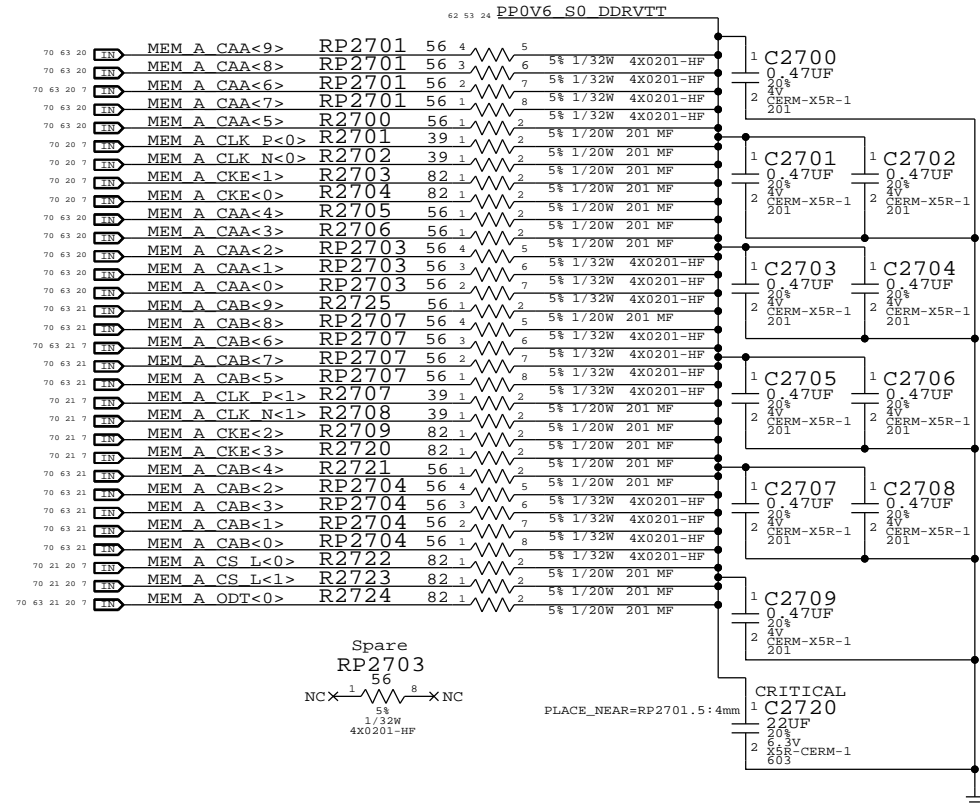


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PAGE TITLE LPDDR3 DRAM Channel B (32-63)			
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REVISION <E4LABEL>		BRANCH <BRANCH>	
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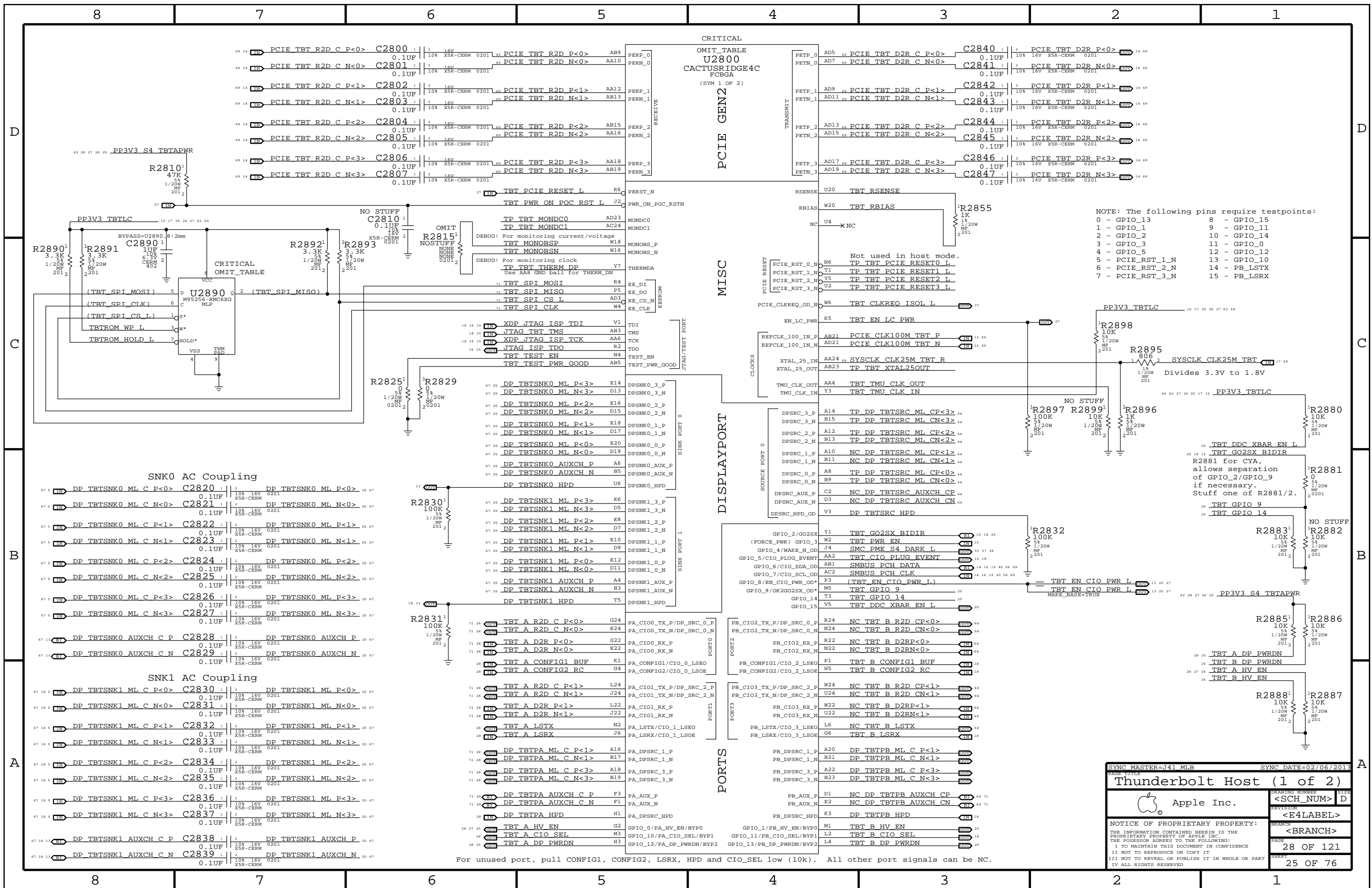
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Intel recommends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK



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LPDDR3 DRAM Termination			
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NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC MASTER=J41 MLB SYNC DATE=02/06/2013

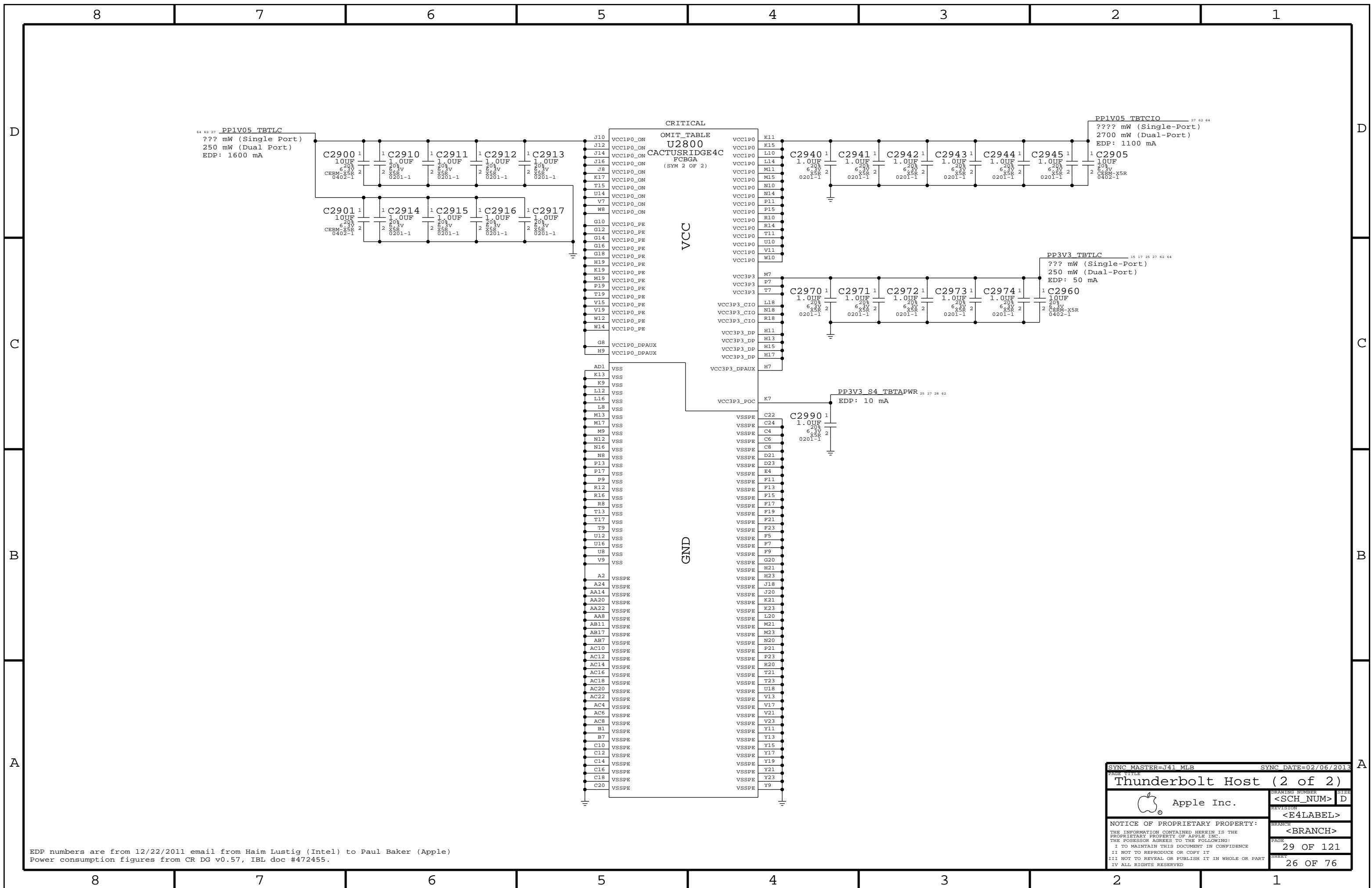
Thunderbolt Host (1 of 2)

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For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.



EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
 Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
Thunderbolt Host (2 of 2)			
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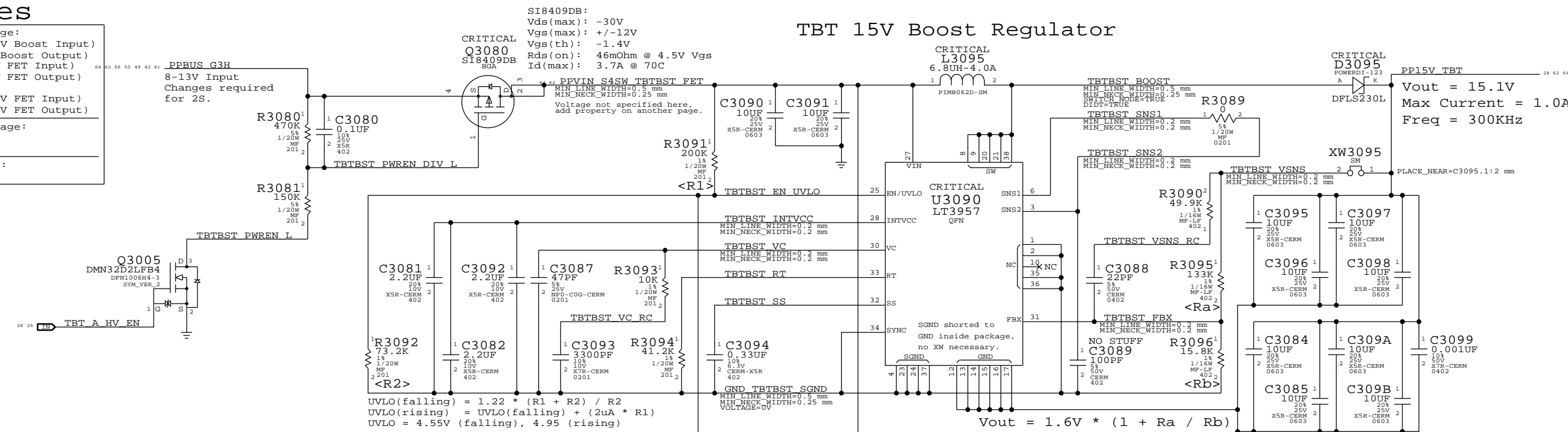
Page Notes

Power aliases required by this page:
 - =PPVIN_SW_TBTBST (8-13V Boost Input)
 - =PP15V_TBT_REG (15V Boost Output)
 - =PP3V3_TBT_P3V3TBTFTET (3.3V FET Input)
 - =PP3V3_TBT_FET (3.3V FET Output)
 - =PP3V3_S0_TBTTPWRCTL
 - =PP1V05_TBT_P1V05TBTFTET (1.05V FET Input)
 - =PP1V05_TBT_FET (1.05V FET Output)

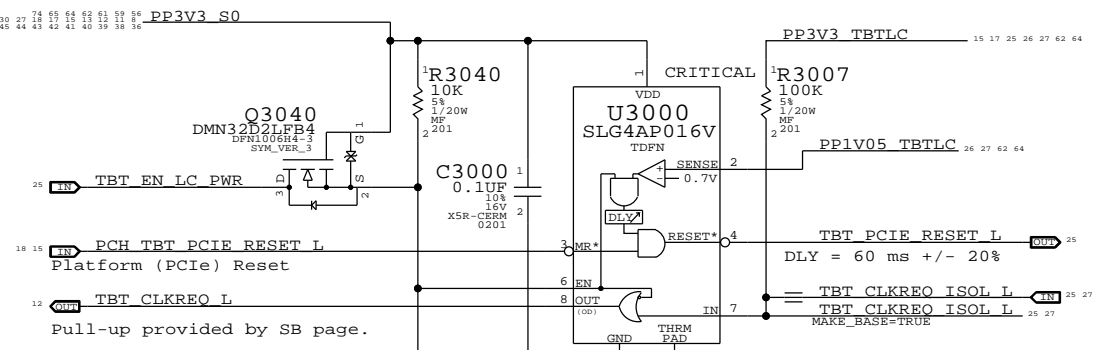
Signal aliases required by this page:
 - =TBT_CLKREQ_L
 - =TBT_RESET_L

BOM options provided by this page:
 (NONE)

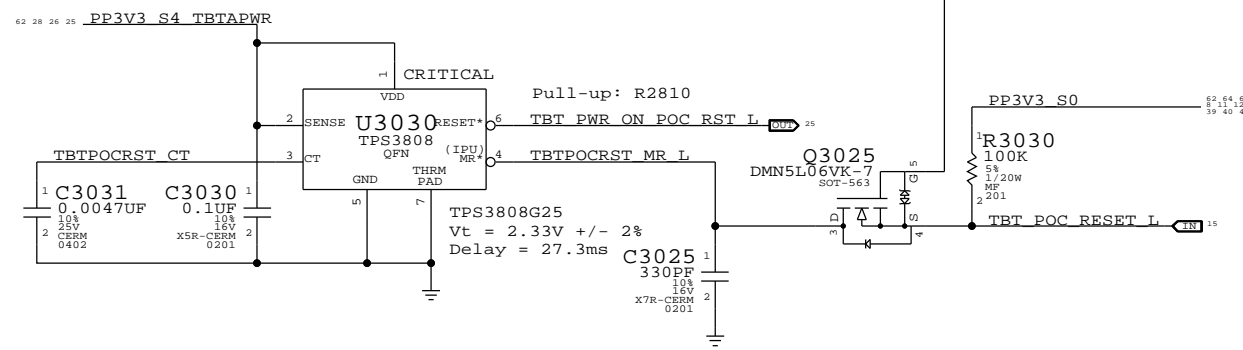
TBT 15V Boost Regulator



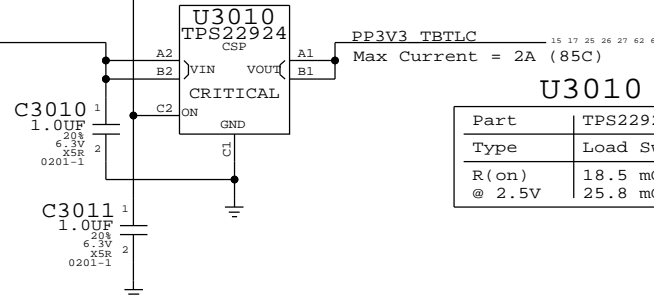
Supervisor & CLKREQ# Isolation



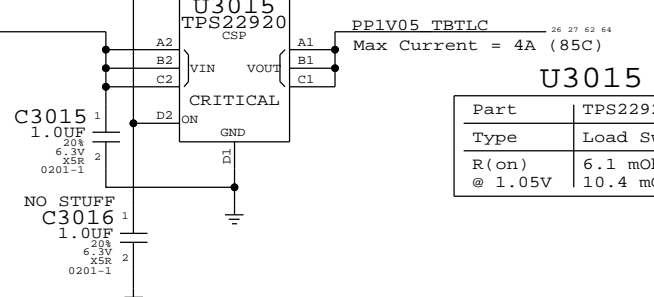
TBT "POC" Power-up Reset



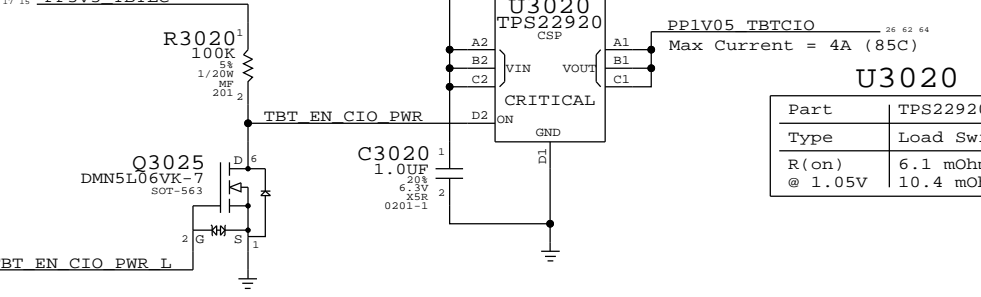
3.3V TBT "LC" Switch



1.05V TBT "LC" Switch



1.05V TBT "CIO" Switch



Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ
@ 1.05V	10.4 mOhm Max

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ
@ 1.05V	10.4 mOhm Max

SYNC MASTER=J41 MLB SYNC DATE=02/06/2013

TBT Power Support

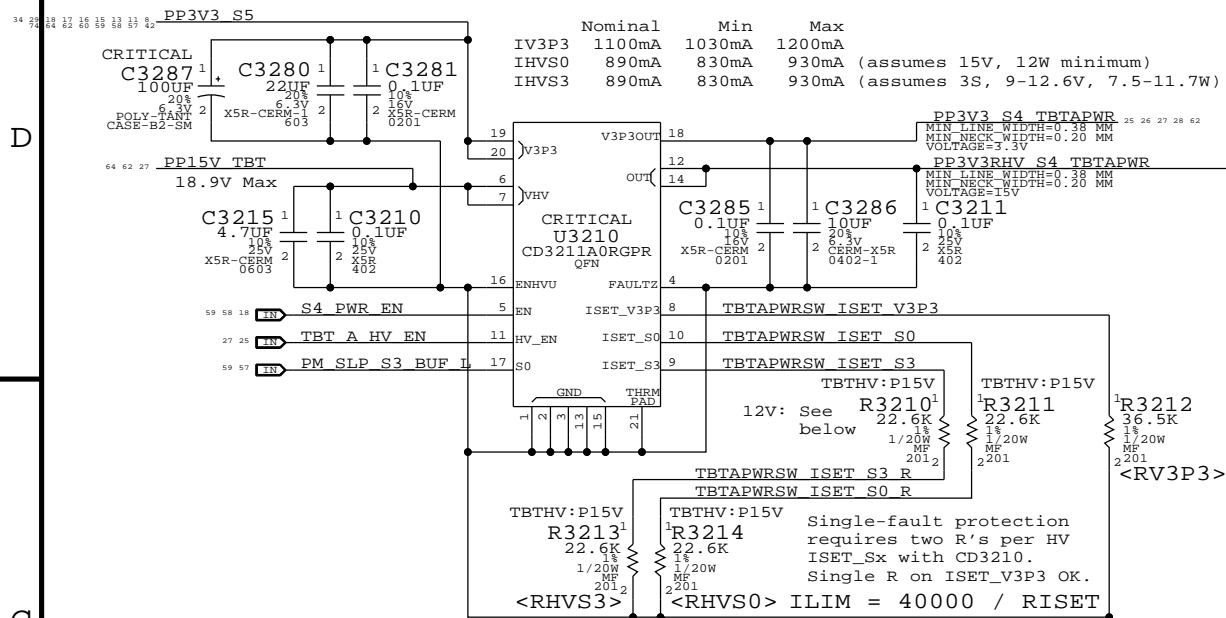
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 REVISION: <E4LABEL>
 BRANCH: <BRANCH>
 PAGE: 30 OF 121
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3.3V/HV Power MUX

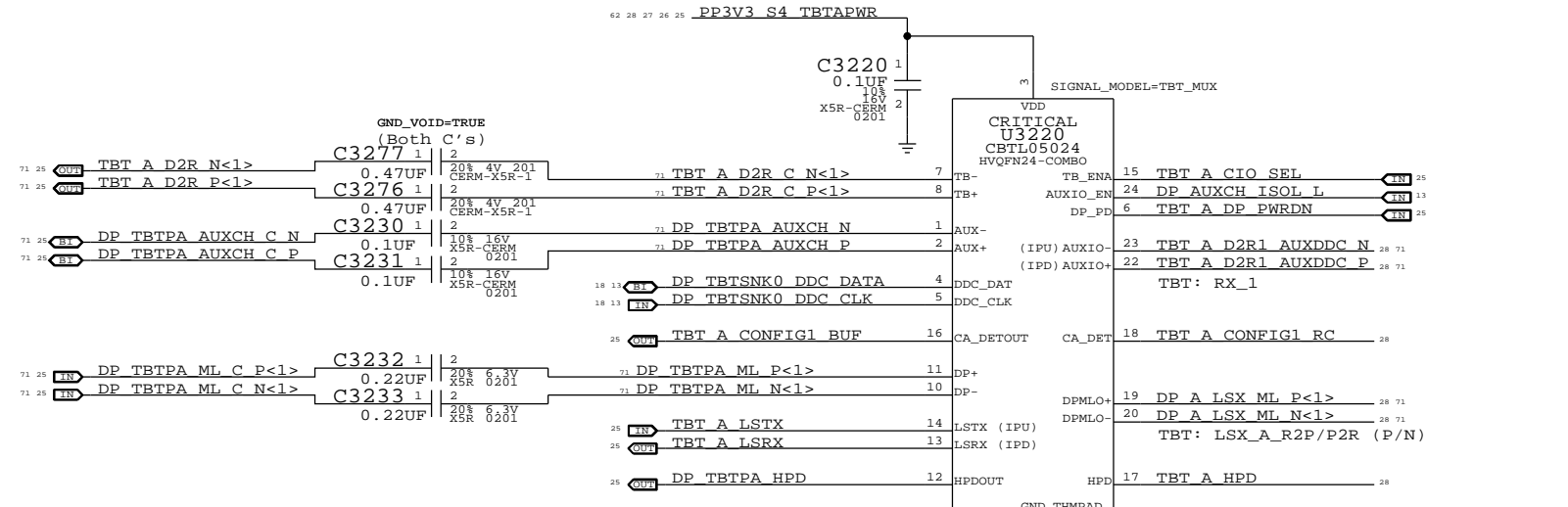
V3P3 must be S4 to support wake from Thunderbolt device attach.



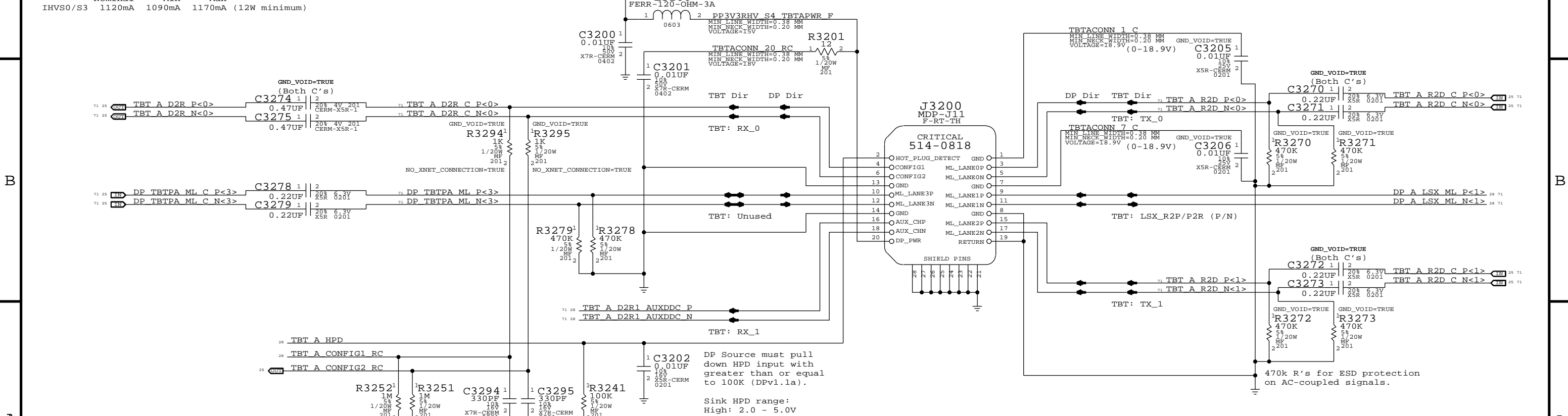
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)



Thunderbolt Connector A



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

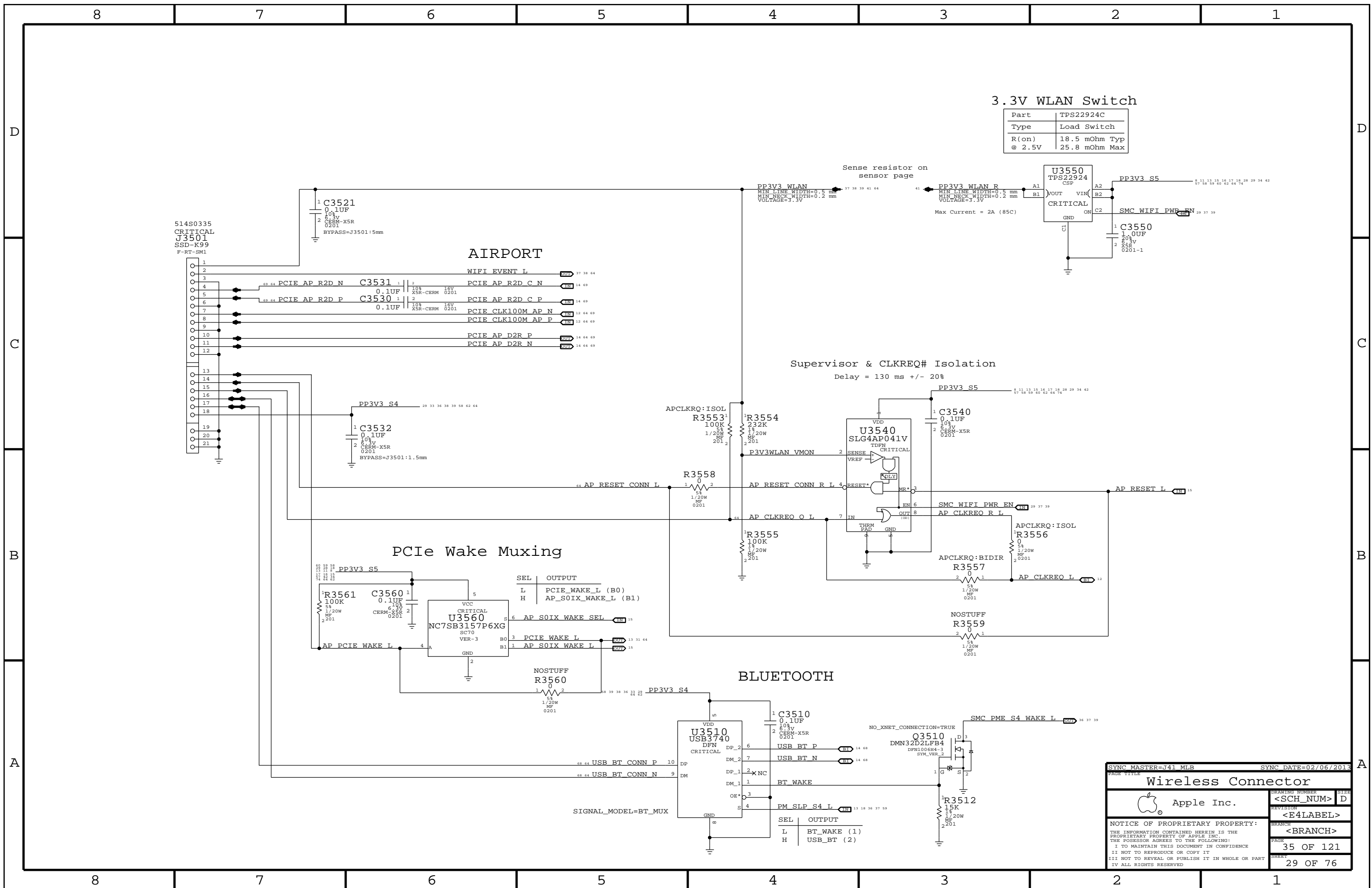
SYNC MASTER=J41 MLB SYNC DATE=02/07/2013

Thunderbolt Connector A

Apple Inc.

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3.3V WLAN Switch

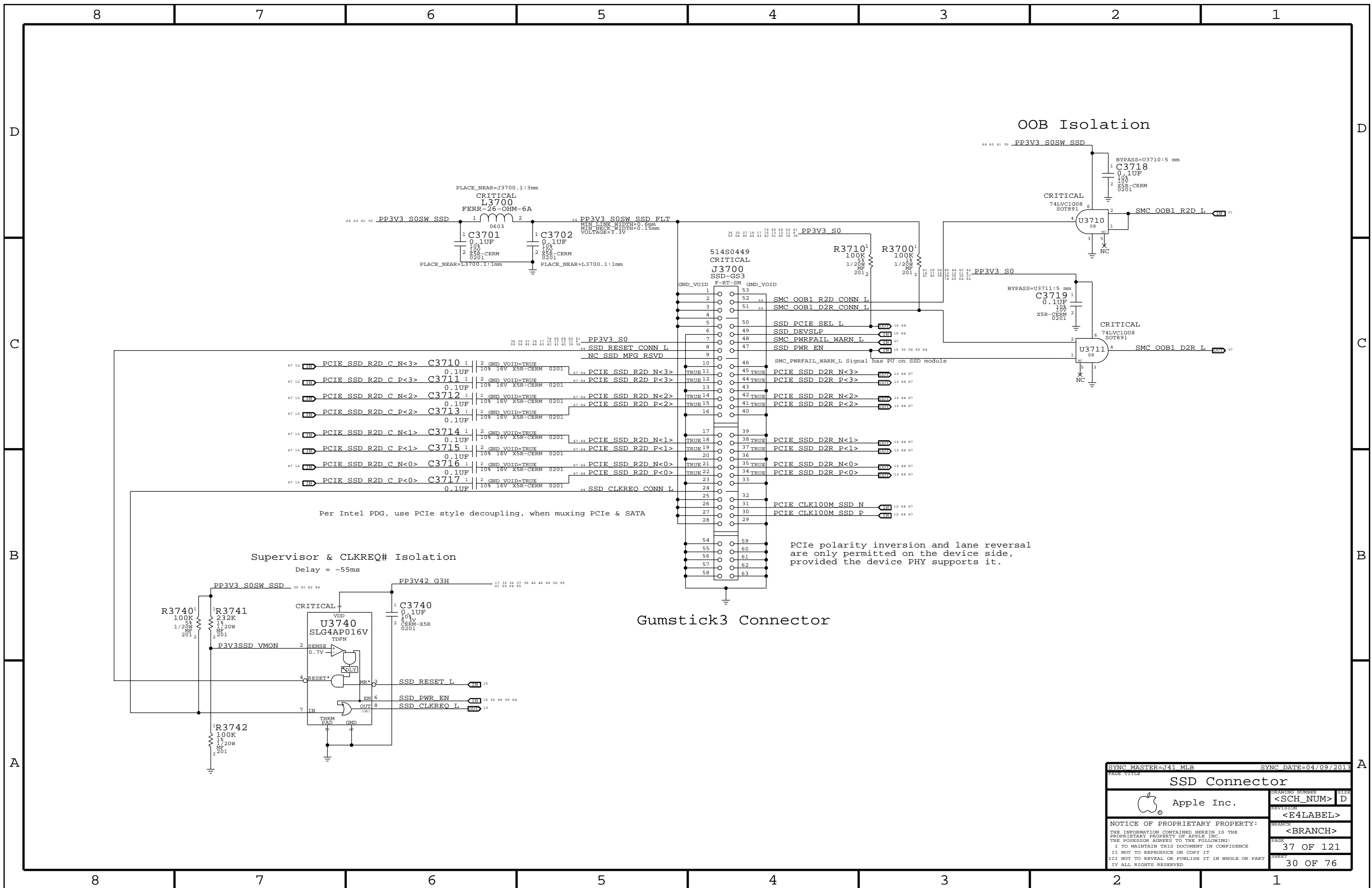
Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

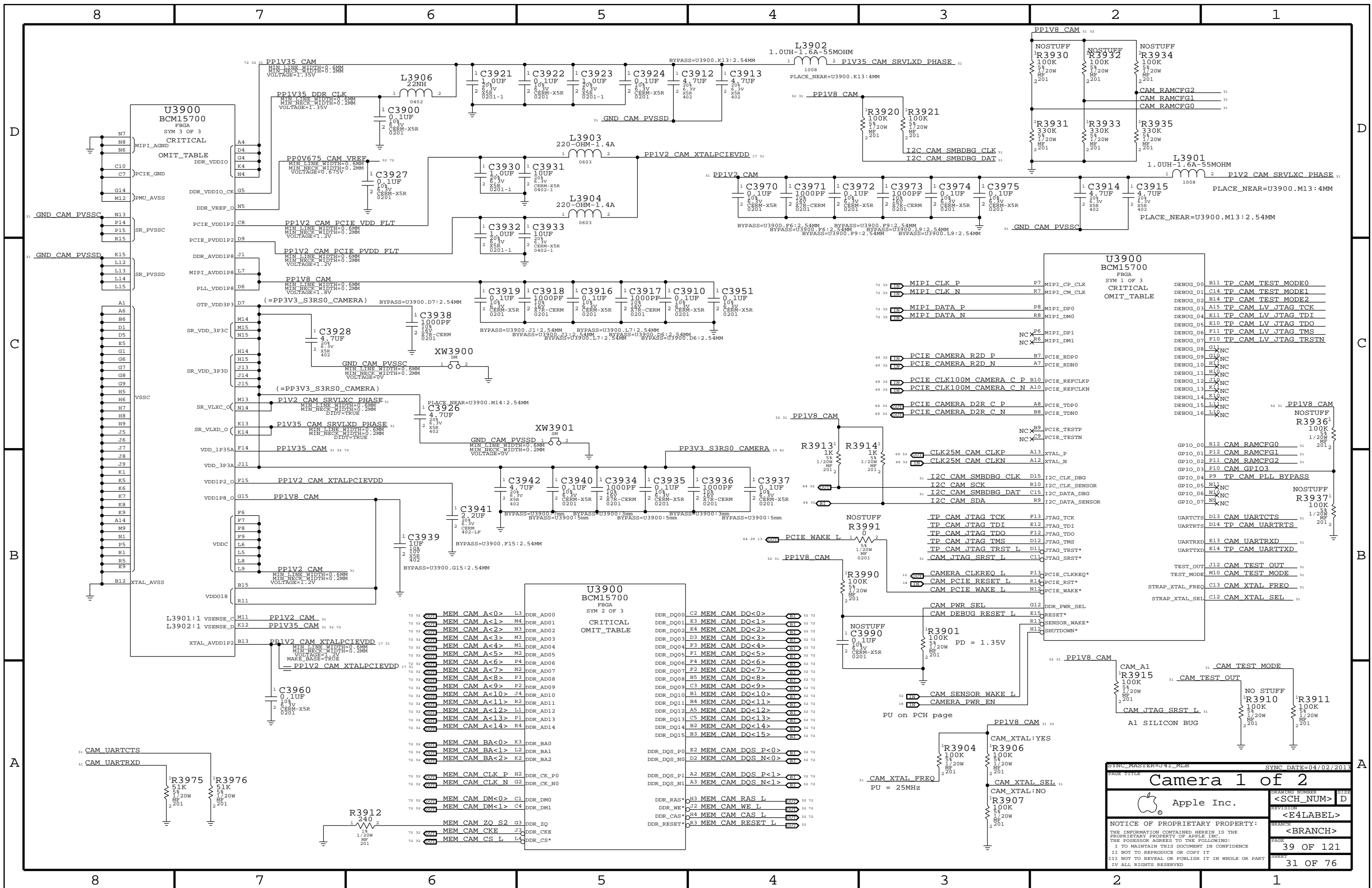
PCie Wake Muxing

BLUETOOTH

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
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Apple Inc.		<SCH_NUM>	D
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SSD Connector			
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		REVISION	
		<E4LABEL>	
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		SHEET	30 OF 76

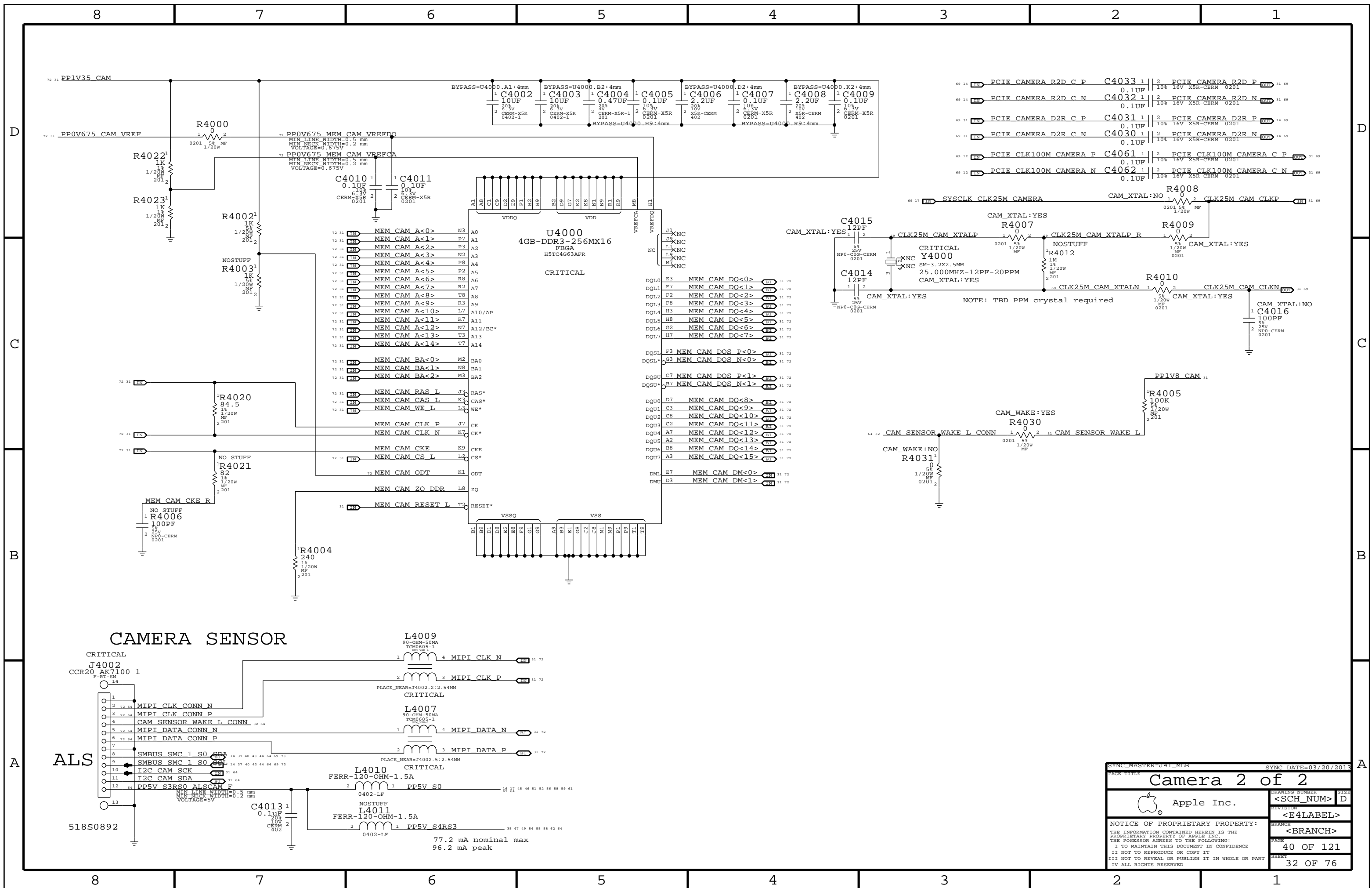


Camera 1 of 2

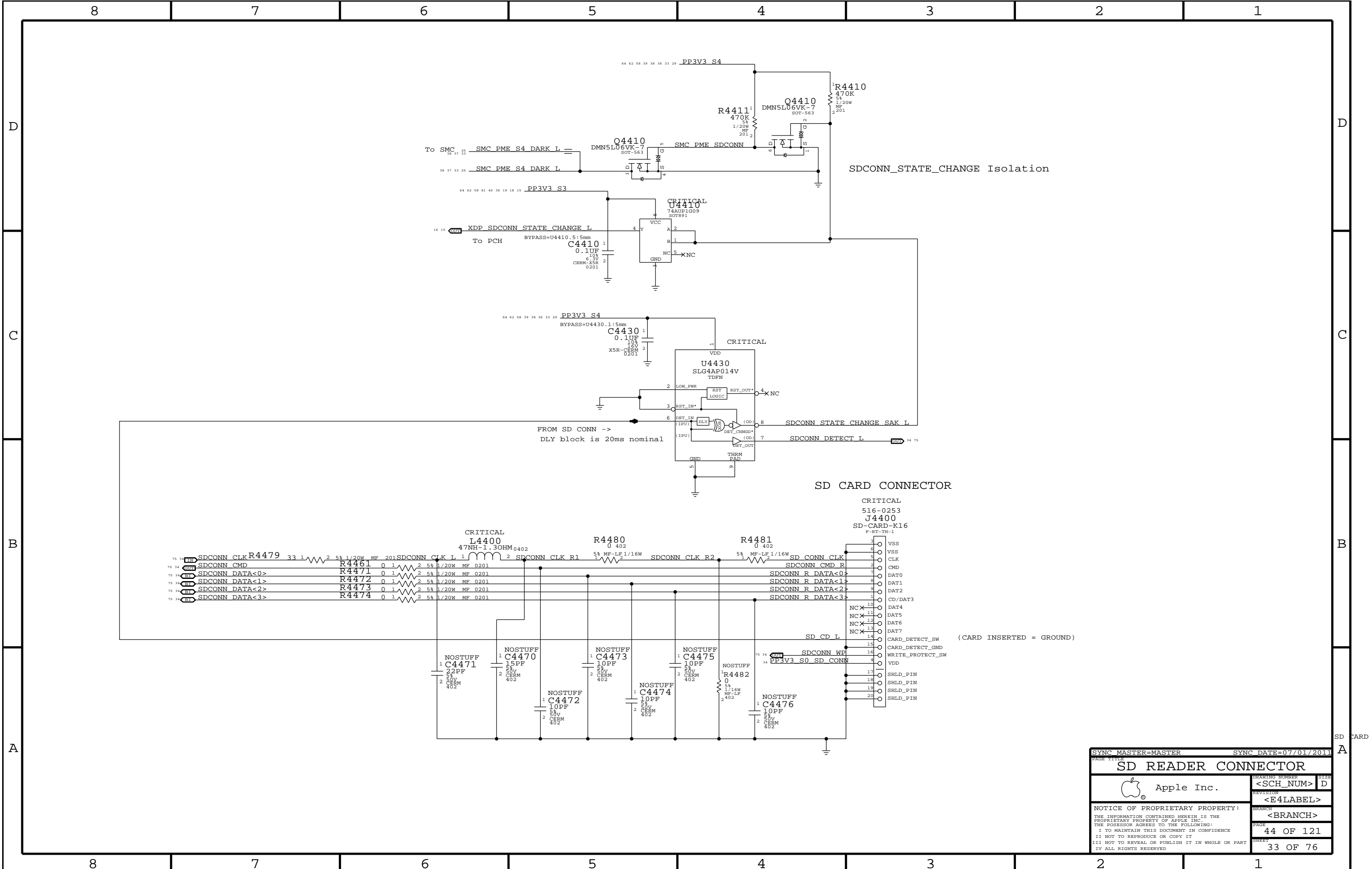
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SHEET	31 OF 76	

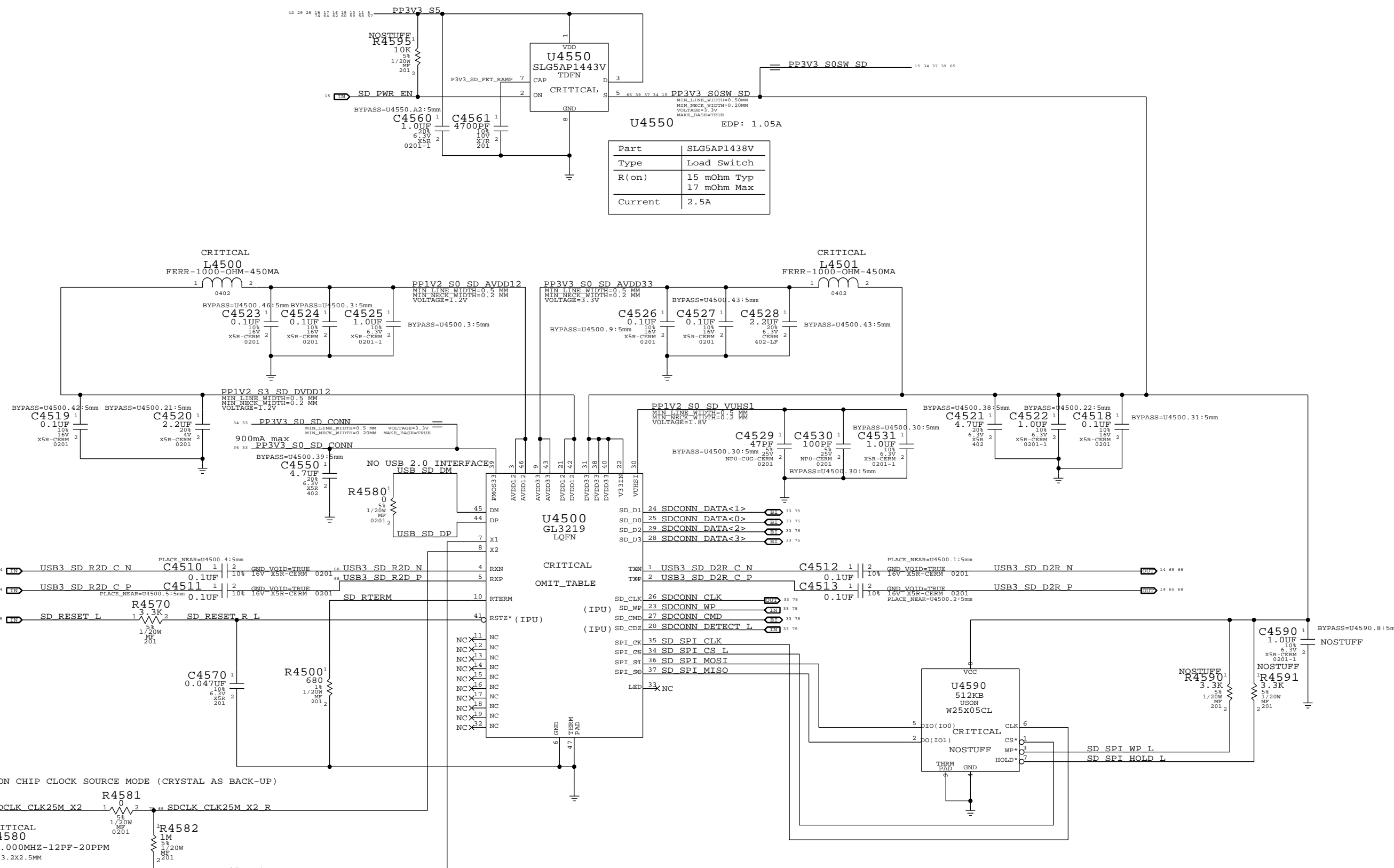


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Camera 2 of 2			
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SYNC_MASTER=MASTER		SYNC_DATE=07/01/2011	
SD READER CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	44 OF 121
		SHEET	33 OF 76

3.3V S3 SD Card Switch

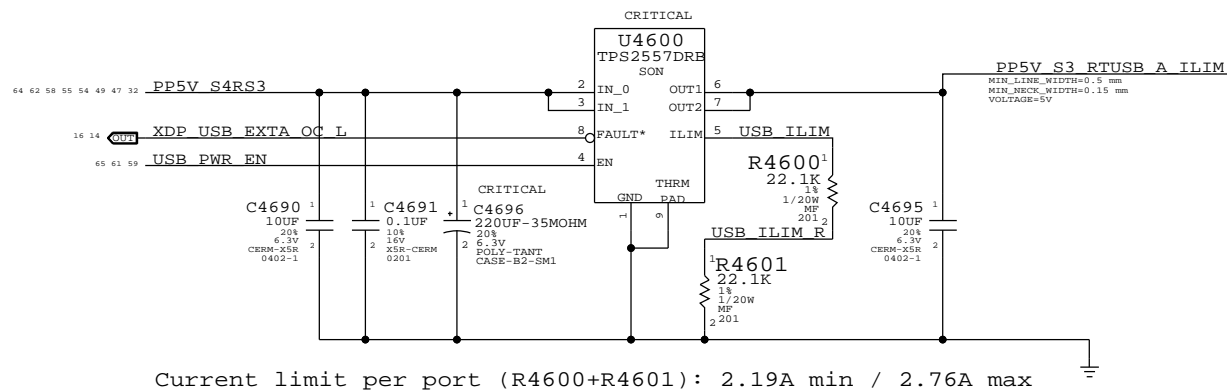


Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ
Current	2.5A

SYNC MASTER=MASTER		SYNC DATE=10/11/2010	
SD CONTROLLER (GL3219)			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	45 OF 121
		SHEET	34 OF 76

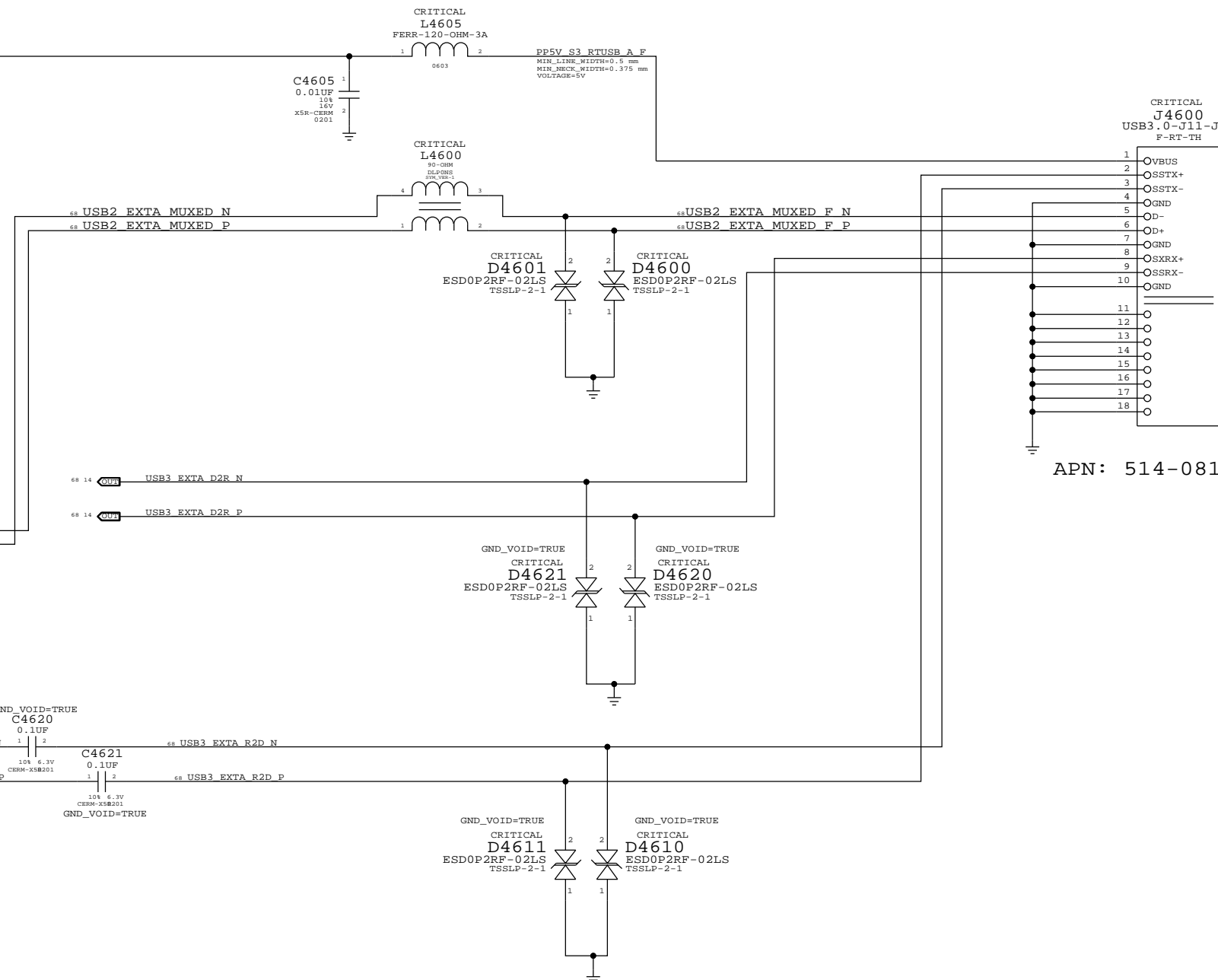
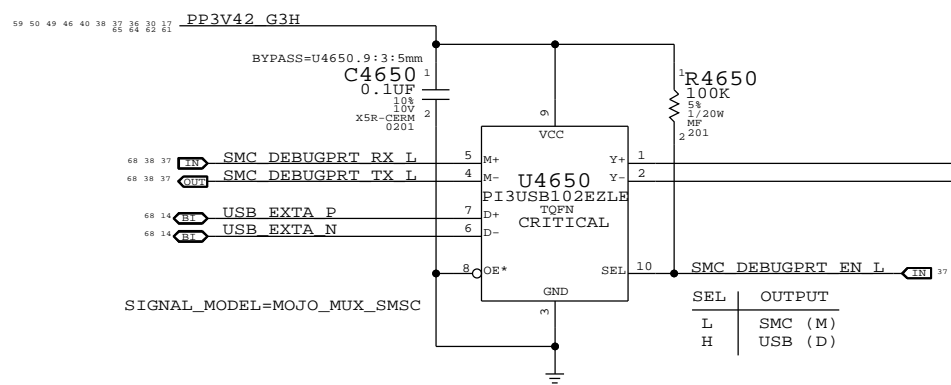
Right USB Port A

USB Port Power Switch



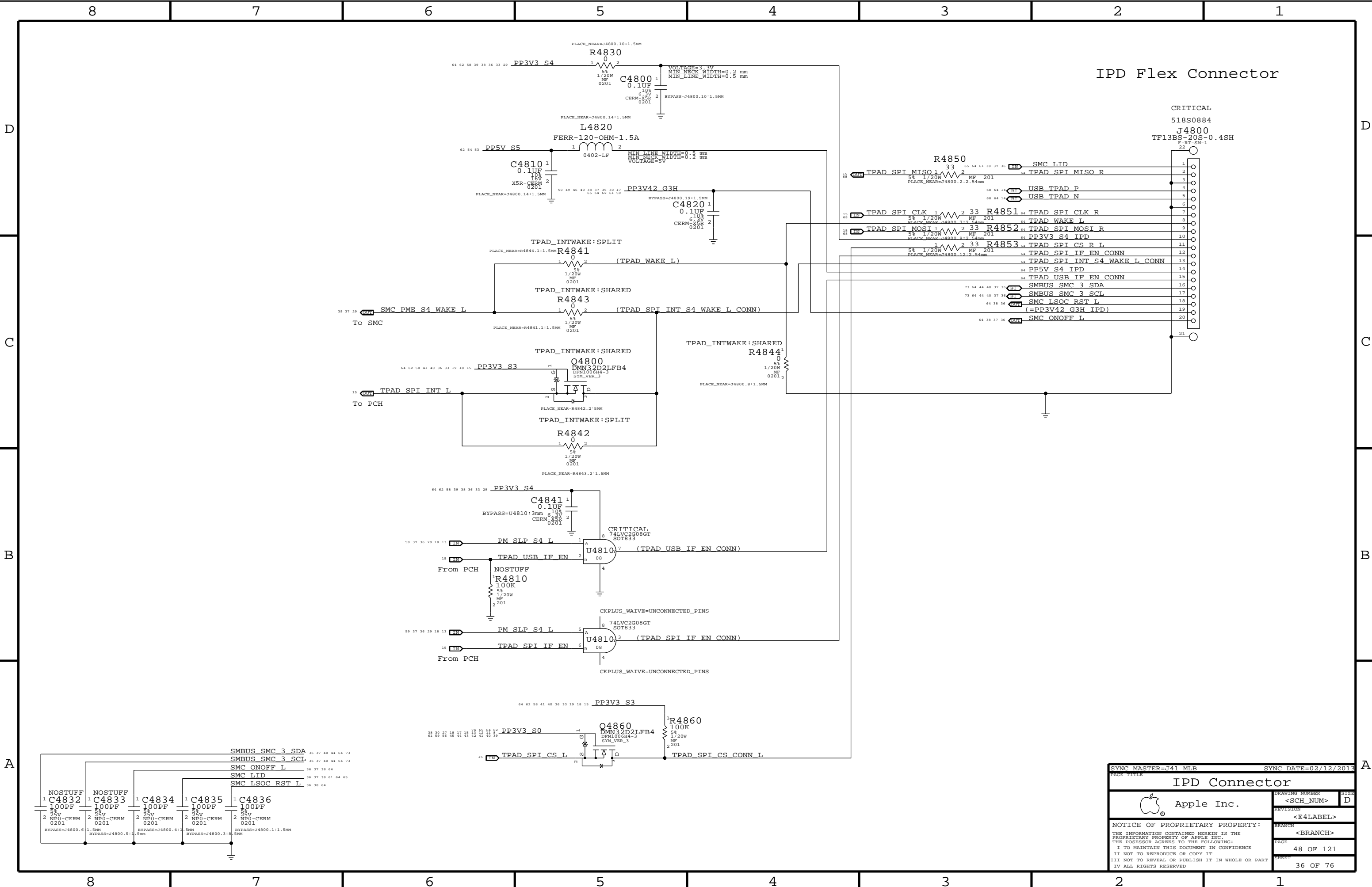
Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux



APN: 514-0819

SYNC MASTER=J41 MLB		SYNC DATE=02/07/2013	
External A USB3 Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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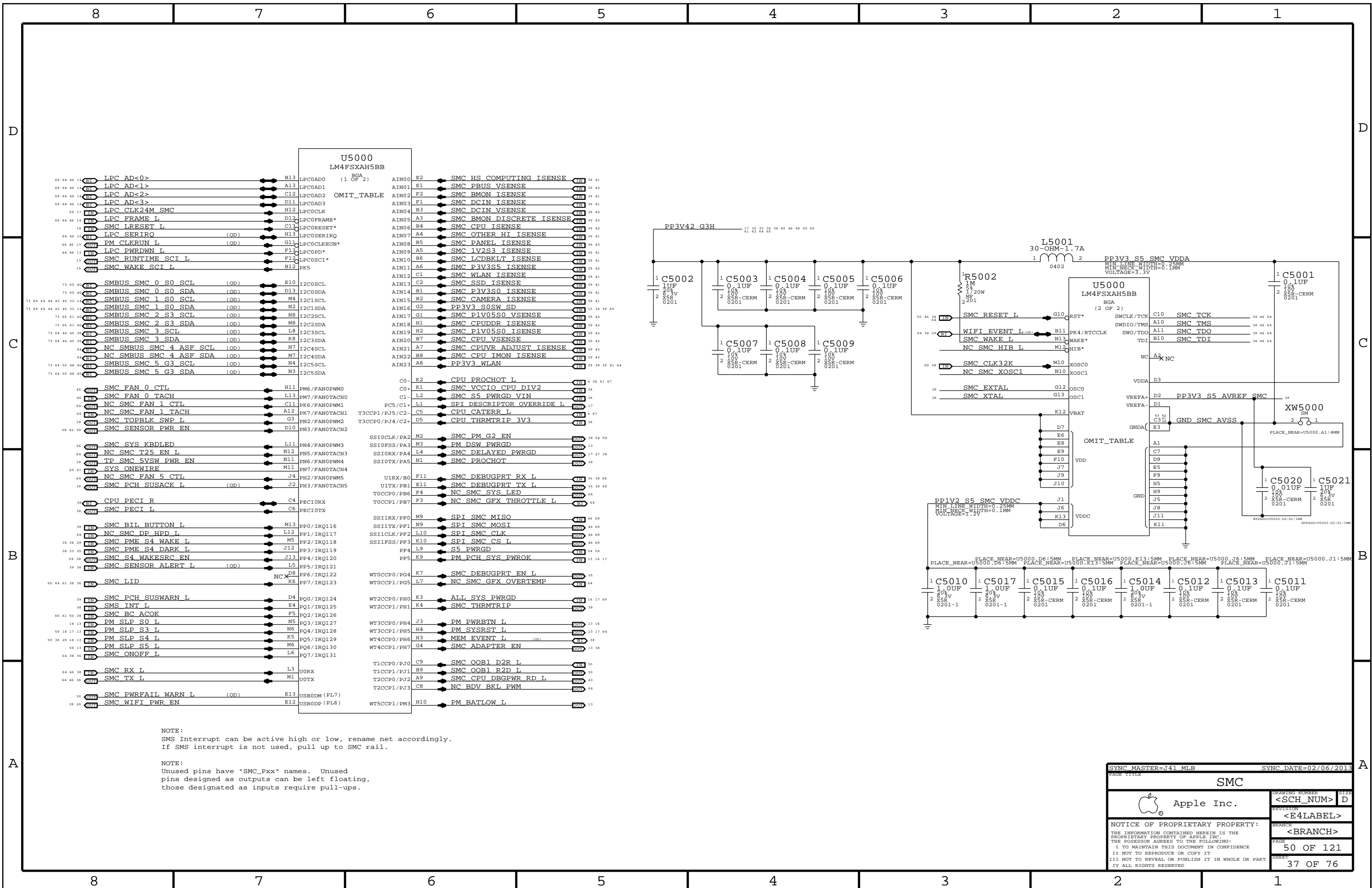


IPD Flex Connector

CRITICAL
518S0884
J4800
TF13BS-20S-0.4SH
F-RT-SM-1

33	65	64	61	38	37	36	TPAD SPI MISO L	TPAD SPI MISO R
68	64	14	68	64	14	68	USB TPAD P	USB TPAD N
68	64	14	68	64	14	68	TPAD SPI CLK L	TPAD SPI CLK R
68	64	14	68	64	14	68	TPAD SPI MOSI L	TPAD SPI MOSI R
68	64	14	68	64	14	68	TPAD SPI CS R L	TPAD SPI CS R R
68	64	14	68	64	14	68	TPAD SPI IF EN CONN	TPAD SPI IF EN CONN
68	64	14	68	64	14	68	TPAD SPI INT S4 WAKE L CONN	TPAD SPI INT S4 WAKE L CONN
68	64	14	68	64	14	68	PP5V S4 IPD	PP5V S4 IPD
68	64	14	68	64	14	68	TPAD USB IF EN CONN	TPAD USB IF EN CONN
73	64	44	40	37	36	73	SMBUS SMC 3 SDA	SMBUS SMC 3 SDA
73	64	44	40	37	36	73	SMBUS SMC 3 SCL	SMBUS SMC 3 SCL
64	38	36	64	38	36	64	SMC LSOC RST L	SMC LSOC RST L
64	38	36	64	38	36	64	(=PP3V42_G3H_IPD)	(=PP3V42_G3H_IPD)
64	38	36	64	38	36	64	SMC ONOFF L	SMC ONOFF L

SYNC MASTER=J41 MLB		SYNC DATE=02/12/2013	
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IPD Connector			
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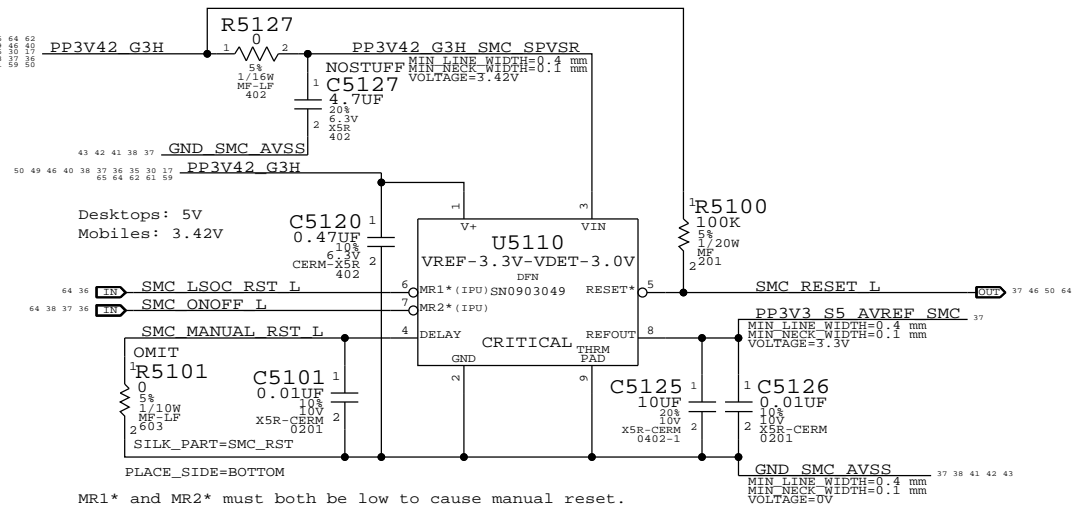


NOTE:
 SMS Interrupt can be active high or low, rename net accordingly.
 If SMS interrupt is not used, pull up to SMC rail.

NOTE:
 Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

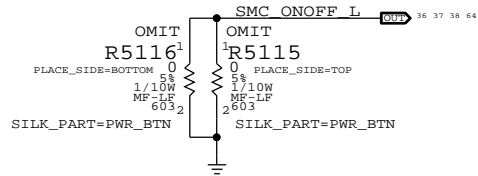
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SMC			
Apple Inc.		DRAWING NUMBER	SIZE
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SMC Reset "Button", Supervisor & AVREF Supply



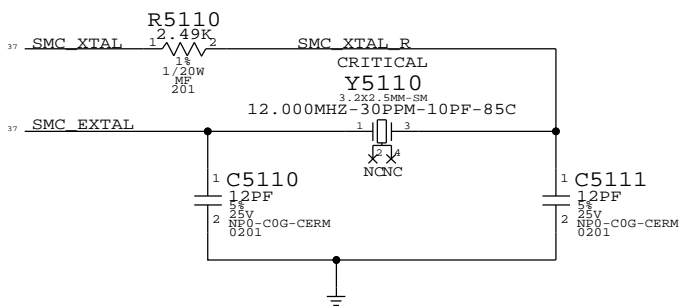
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

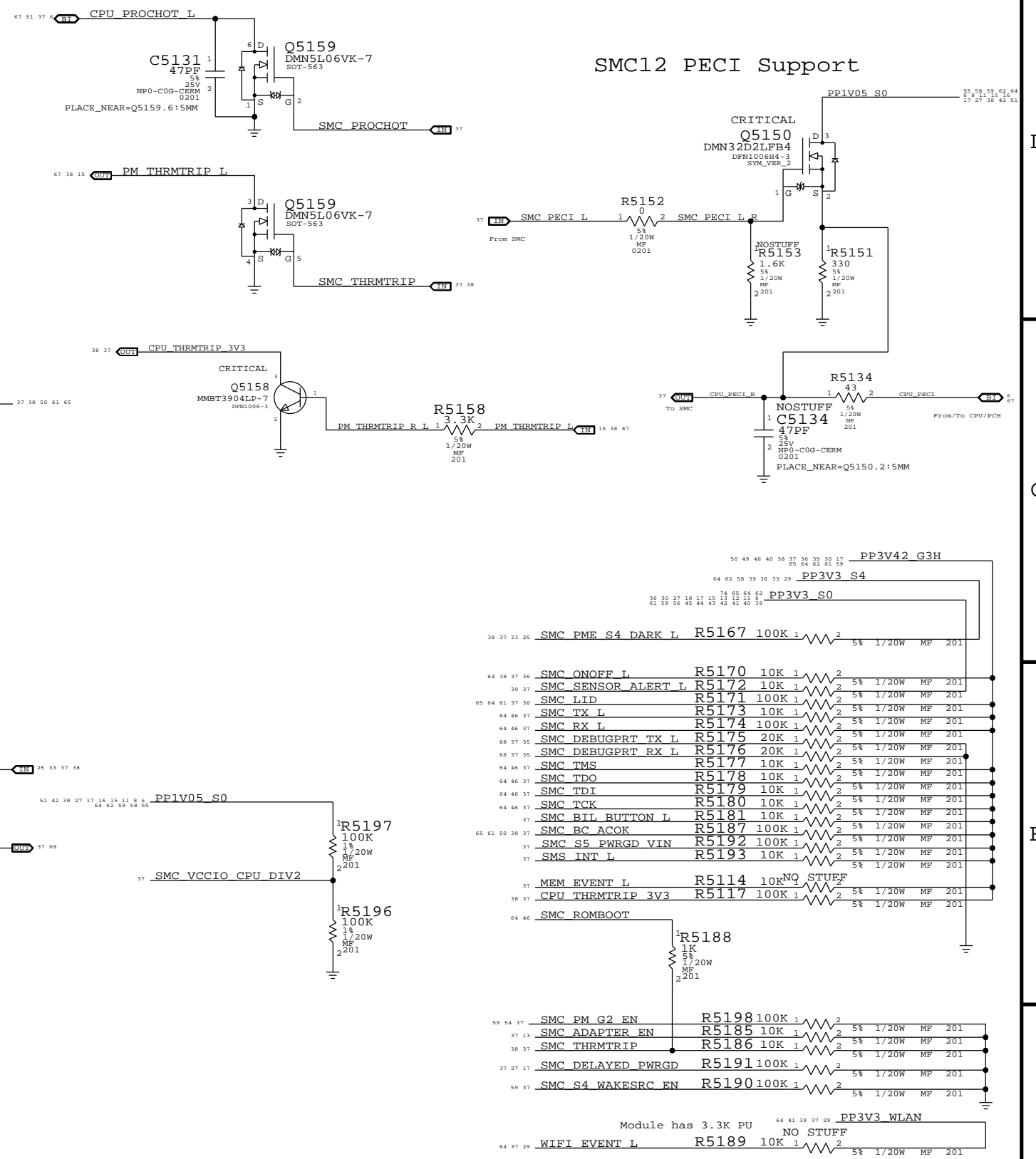


SMC Crystal Circuit

SMC USB Clock require these crystal values: 5, 6, 8, 10, 12, 16, 18, 20, 24, 25 MHz



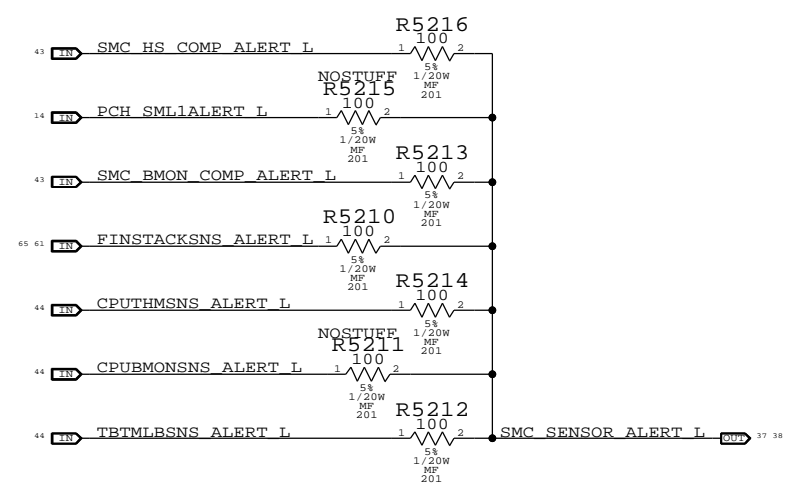
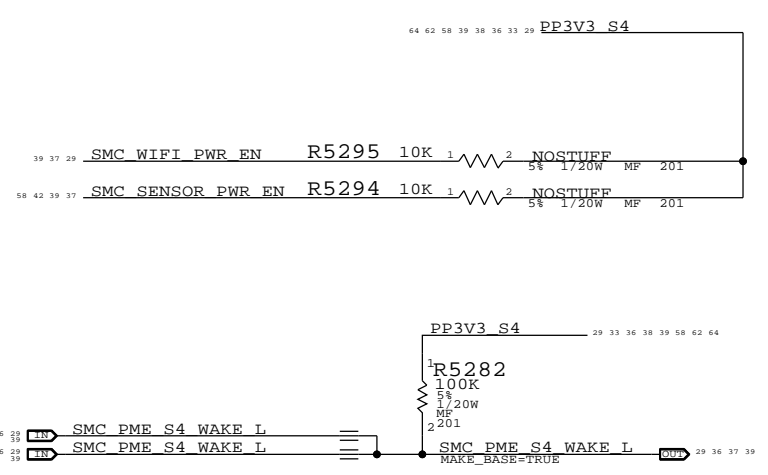
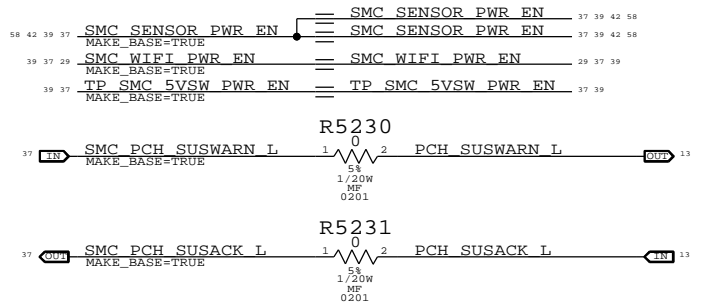
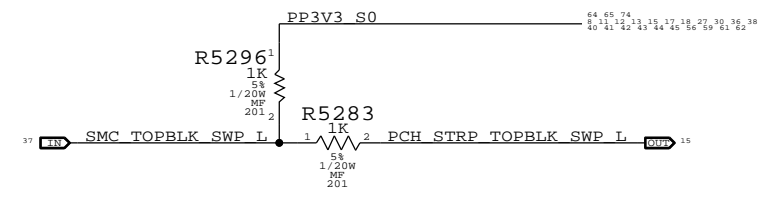
SMC12 PECl Support



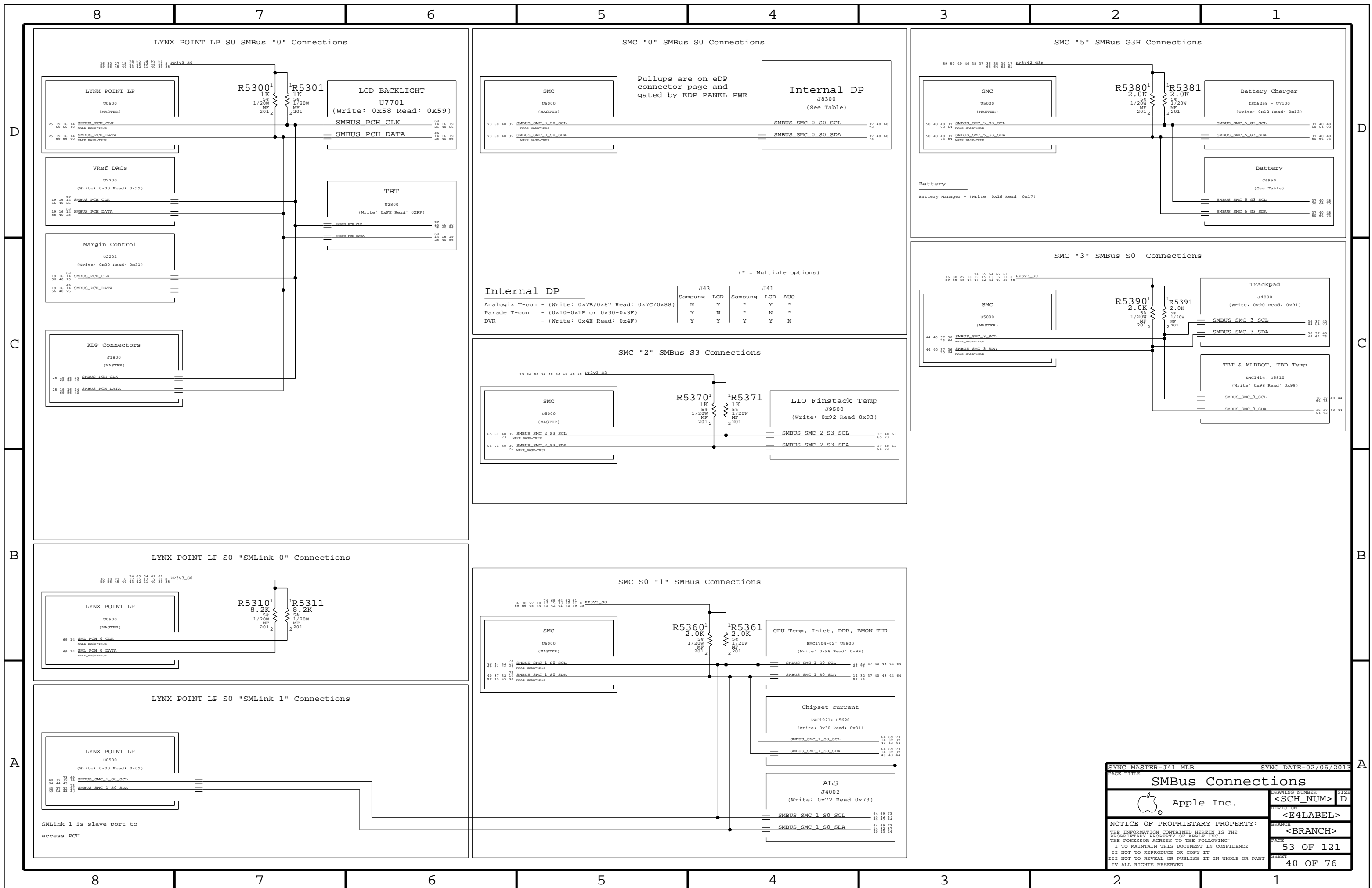
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SMC Shared Support			
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41 39 37	SMC HS COMPUTING ISENSE	SMC HS COMPUTING ISENSE	37 39 41
42 39 37	SMC PBUS VSENSE	SMC PBUS VSENSE	37 39 42
41 39 37	SMC BMON ISENSE	SMC BMON ISENSE	37 39 41
41 39 37	SMC DCIN ISENSE	SMC DCIN ISENSE	37 39 41
42 39 37	SMC DCIN VSENSE	SMC DCIN VSENSE	37 39 42
43 39 37	SMC BMON DISCRETE ISENSE	SMC BMON DISCRETE ISENSE	37 39 43
42 39 37	SMC CPU ISENSE	SMC CPU ISENSE	37 39 42
41 39 37	SMC OTHER HI ISENSE	SMC OTHER HI ISENSE	37 39 41
43 39 37	SMC PANEL ISENSE	SMC PANEL ISENSE	37 39 43
41 39 37	SMC 1V2S3 ISENSE	SMC 1V2S3 ISENSE	37 39 41
41 39 37	SMC LCDBKLT ISENSE	SMC LCDBKLT ISENSE	37 39 41
42 39 37	SMC P3V3S5 ISENSE	SMC P3V3S5 ISENSE	37 39 42
41 39 37	SMC WLAN ISENSE	SMC WLAN ISENSE	37 39 41
41 39 37	SMC SSD ISENSE	SMC SSD ISENSE	37 39 41
41 39 37	SMC P3V3S0 ISENSE	SMC P3V3S0 ISENSE	37 39 41
41 39 37	SMC CAMERA ISENSE	SMC CAMERA ISENSE	37 39 41
	PP3V3 SOSW_SD	PP3V3 SD alias on page 103	
42 39 37	SMC P1V05S0 VSENSE	SMC P1V05S0 VSENSE	37 39 42
42 39 37	SMC CPUDDR ISENSE	SMC CPUDDR ISENSE	37 39 42
42 39 37	SMC P1V05S0 ISENSE	SMC P1V05S0 ISENSE	37 39 42
42 39 37	SMC CPU VSENSE	SMC CPU VSENSE	37 39 42
43 39 37	SMC CPUVR ADJUST ISENSE	SMC CPUVR ADJUST ISENSE	37 39 43
43 39 37	SMC CPU IMON ISENSE	SMC CPU IMON ISENSE	37 39 43
64 41 39 38 37 29	PP3V3 WLAN	PP3V3 WLAN	29 37 38 39 41 64

Top-Block Swap



SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
SMC Project Support			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	<BRANCH>
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			39 OF 76



(* = Multiple options)

	J43	J41
Internal DP		
Analoxix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N Y	* Y *
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y N	* N *
DVR - (Write: 0x4E Read: 0x4F)	Y Y	Y Y N

SYNC MASTER=J41 MLB SYNC DATE=02/06/2013

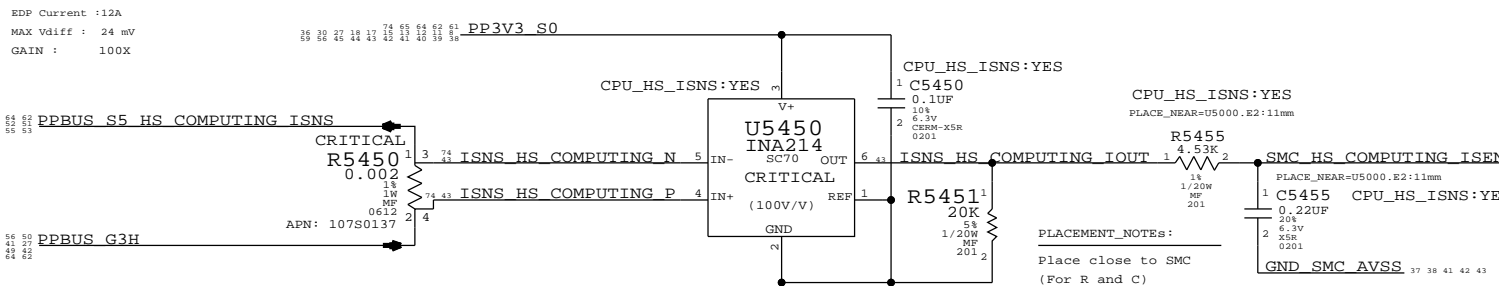
SMBus Connections

Apple Inc.

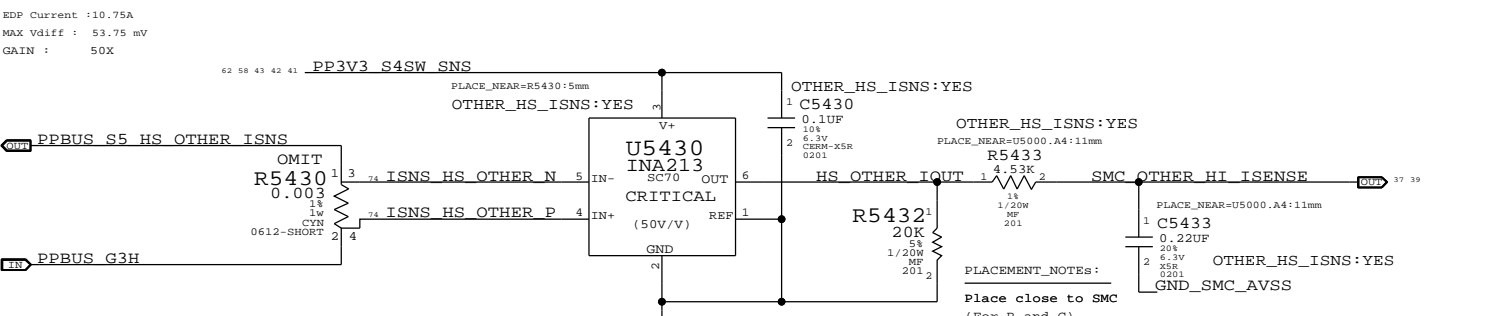
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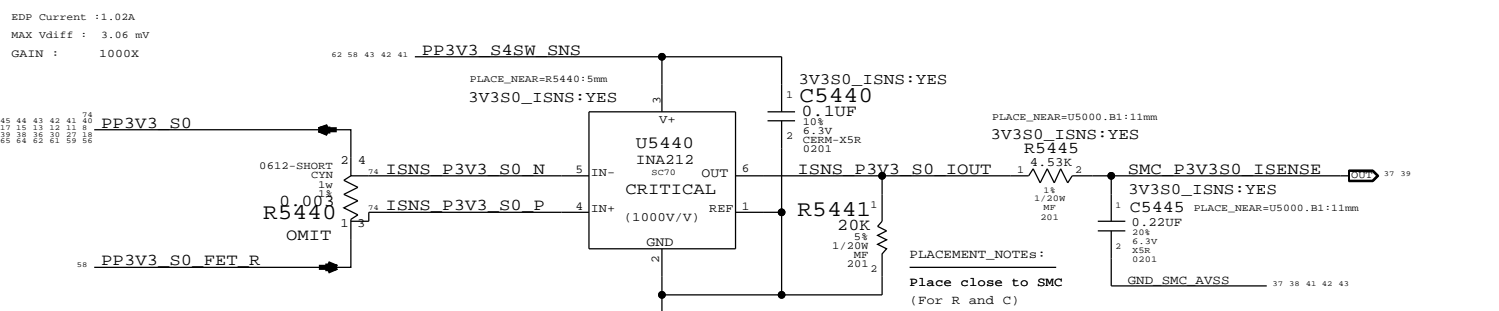
ICOR : COMPUTING High Side Current Sense



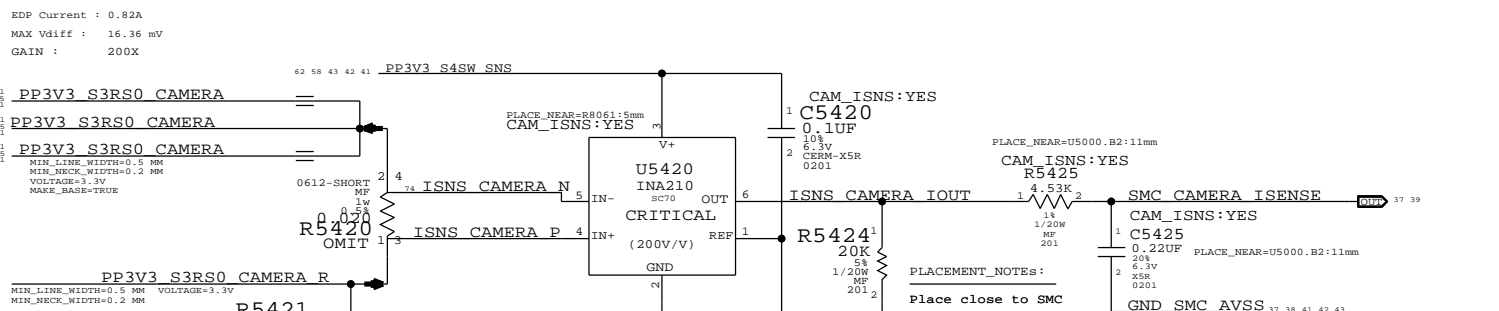
IOOR : OTHER High Side Current Sense



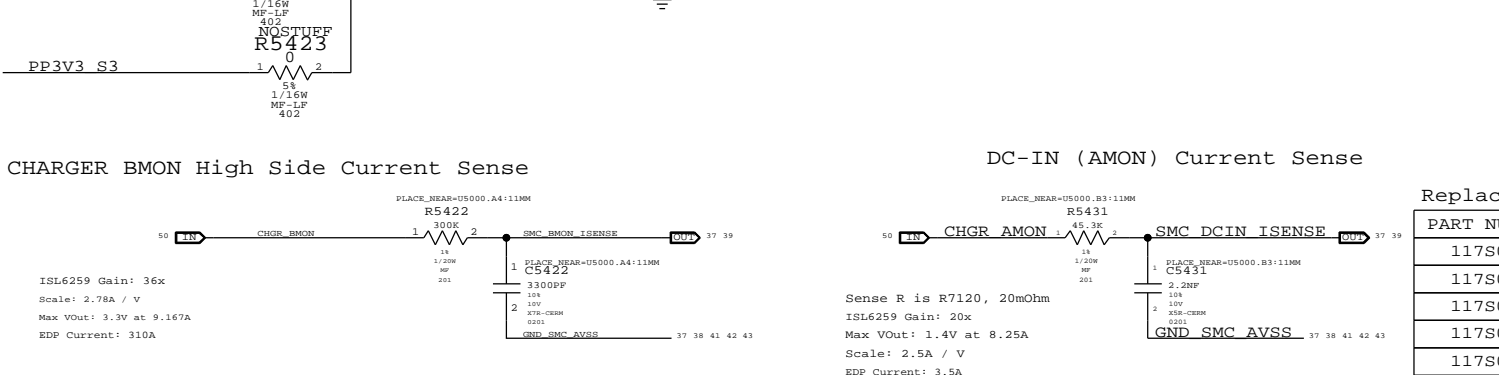
IROC : 3.3V S0 FET Current Sense



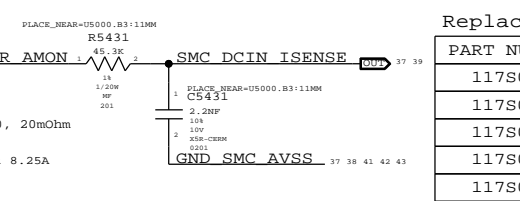
IS2C : 3.3V Camera Current Sense



CHARGER BMON High Side Current Sense



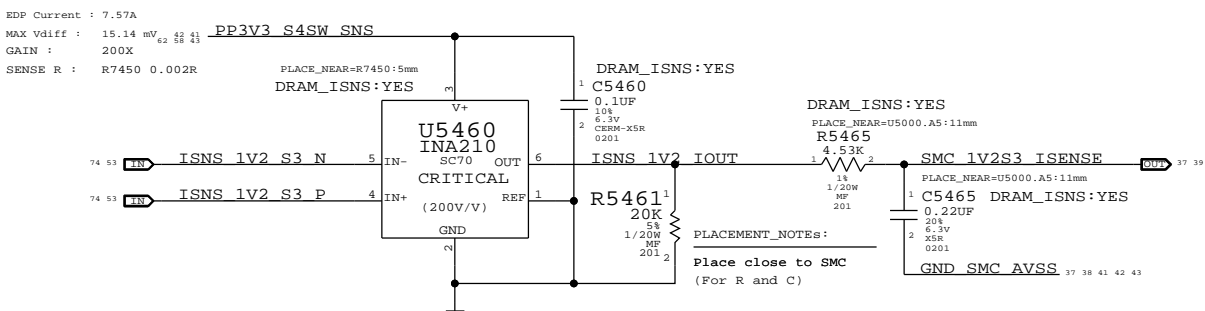
DC-IN (AMON) Current Sense



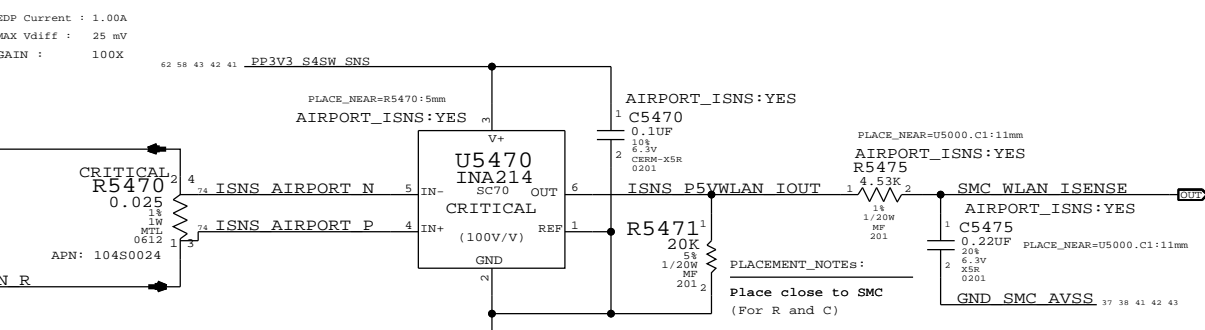
Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

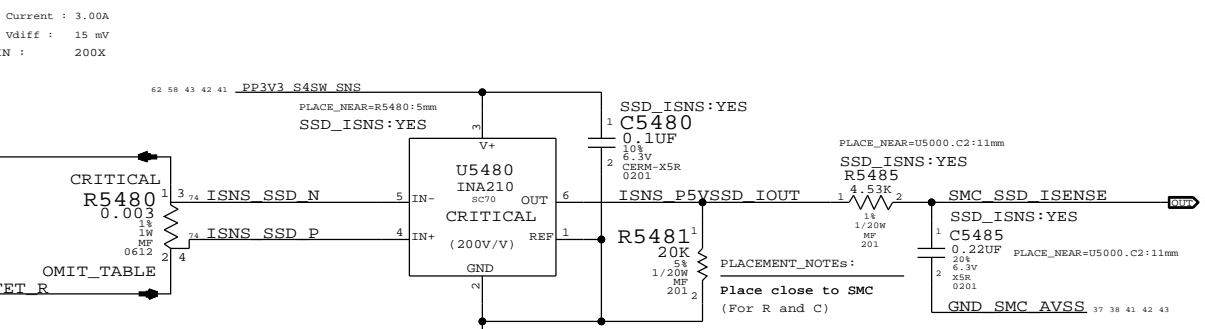
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)



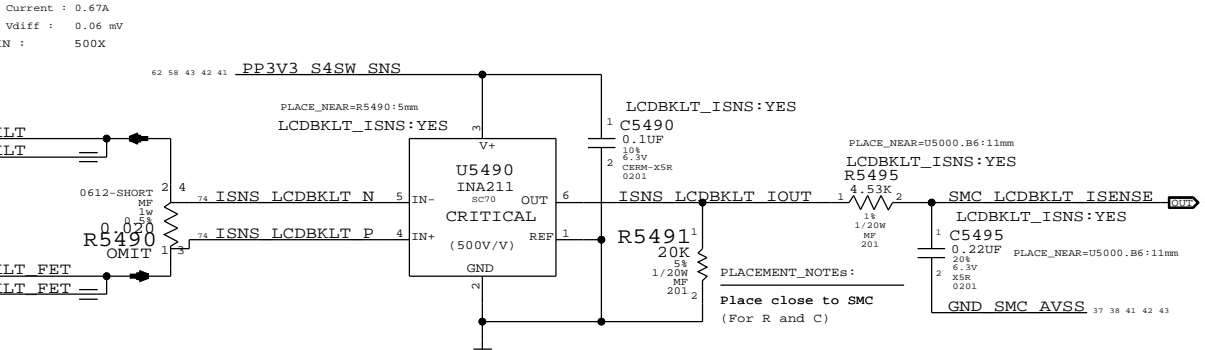
IAPC :AirPort Current Sense



ISDC : SSD Current Sense



IBLC : LCD Backlight Driver Input Current Sense



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

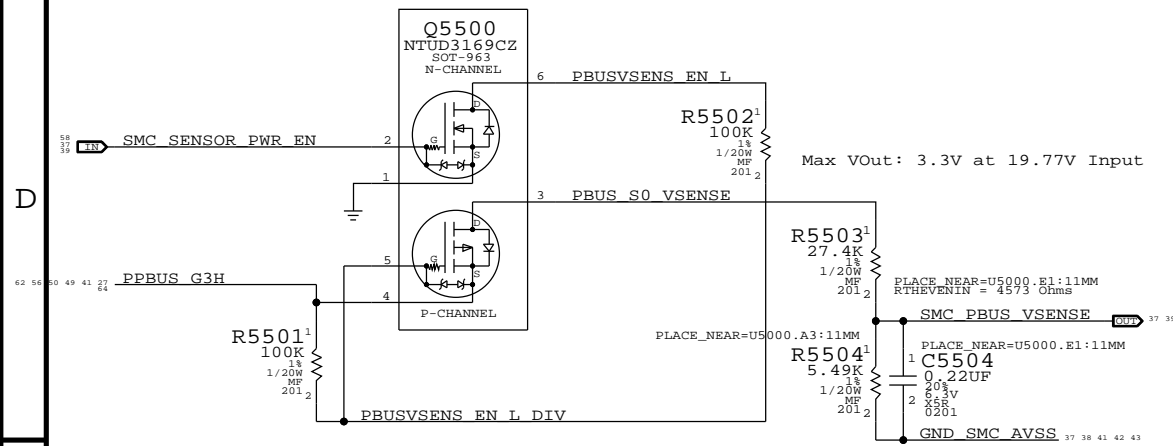
High Side Current Sensing

Apple Inc.

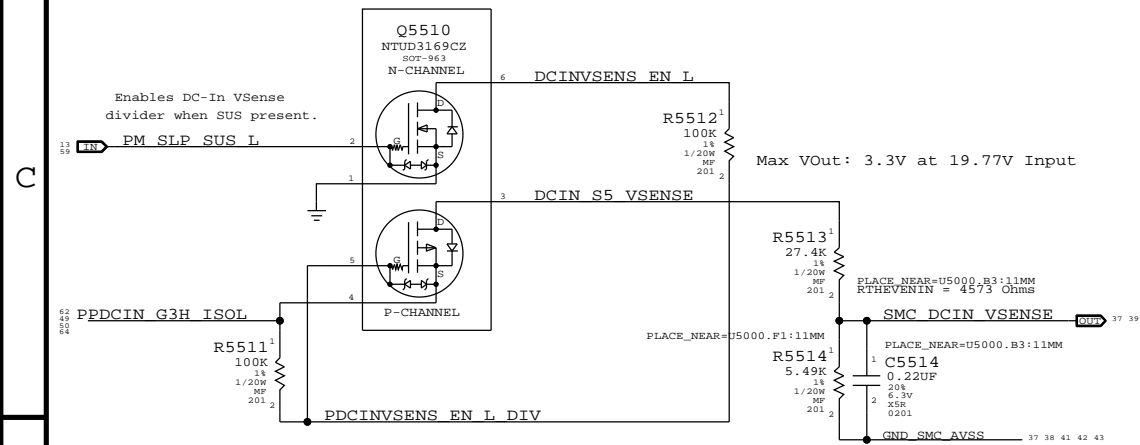
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DRAWING NUMBER: <SCH_NUM> D
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 PAGE: 54 OF 121
 SHEET: 41 OF 76

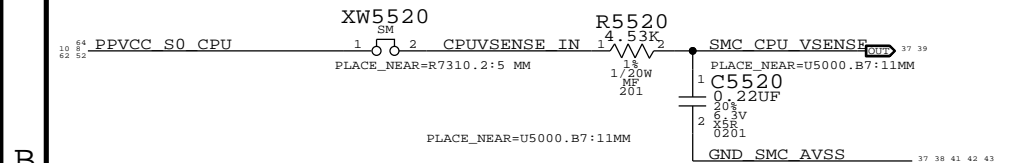
VP0R: PBUS Voltage Sense Enable & Filter



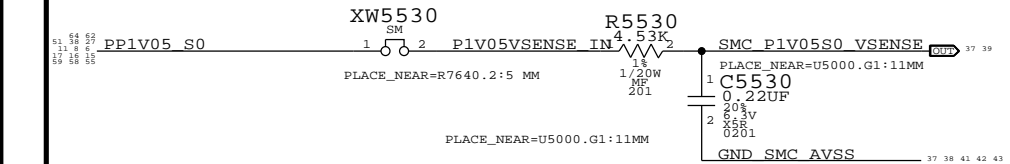
VD0R: DC-In Voltage Sense Enable & Filter



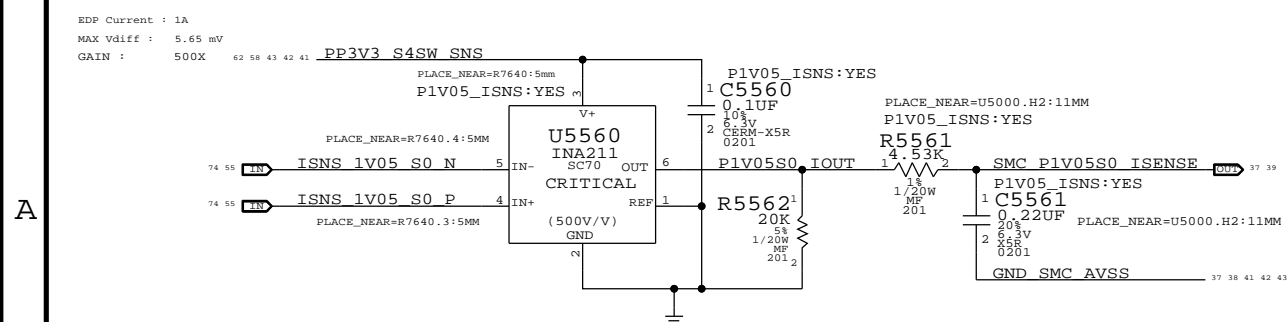
CPU Vcore Voltage Sense / Filter



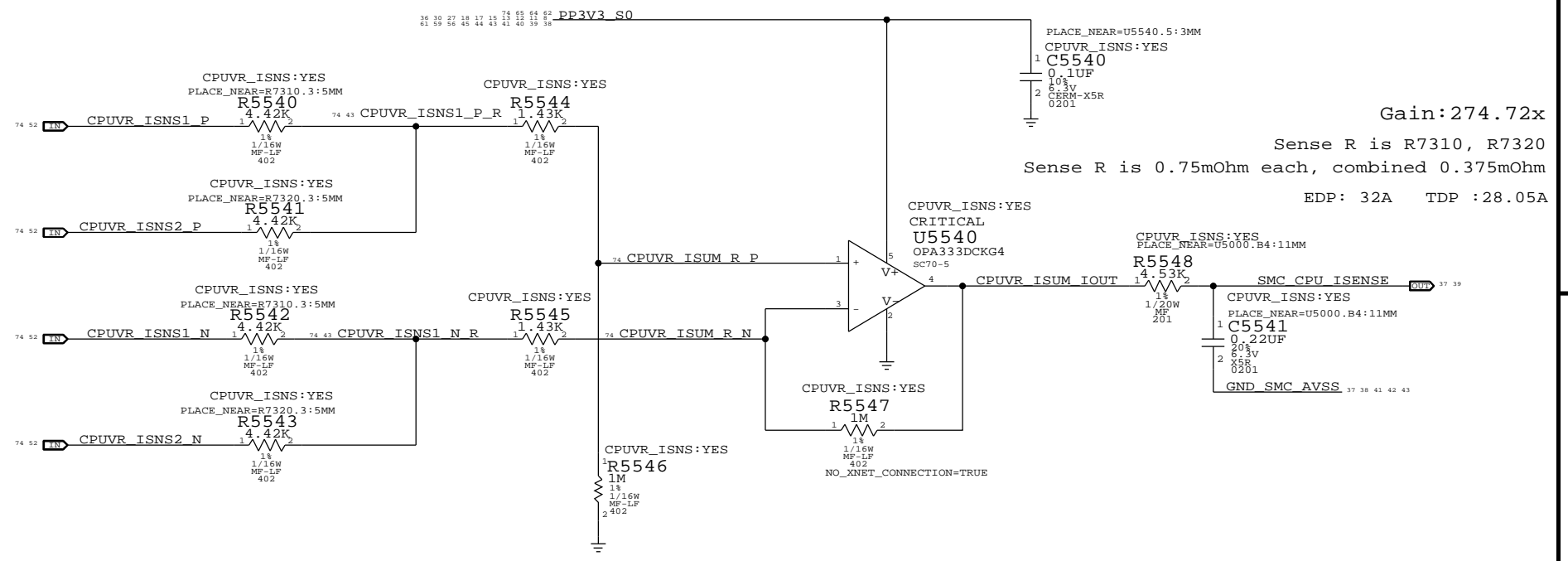
1.05V Voltage Sense / Filter



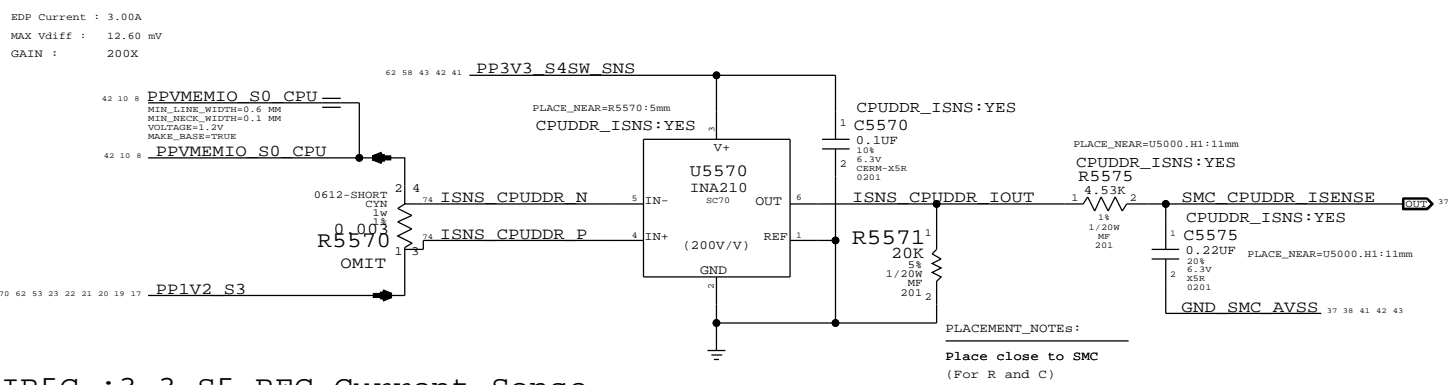
IC1C: 1.05V S0 CURRENT SENSE / FILTER



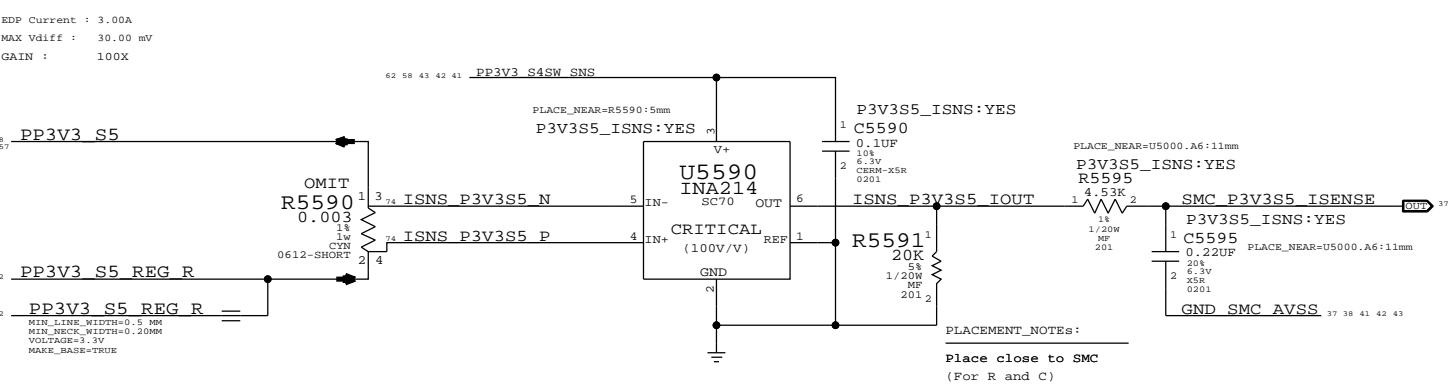
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C : 3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

Voltage & Load Side Current Sensing

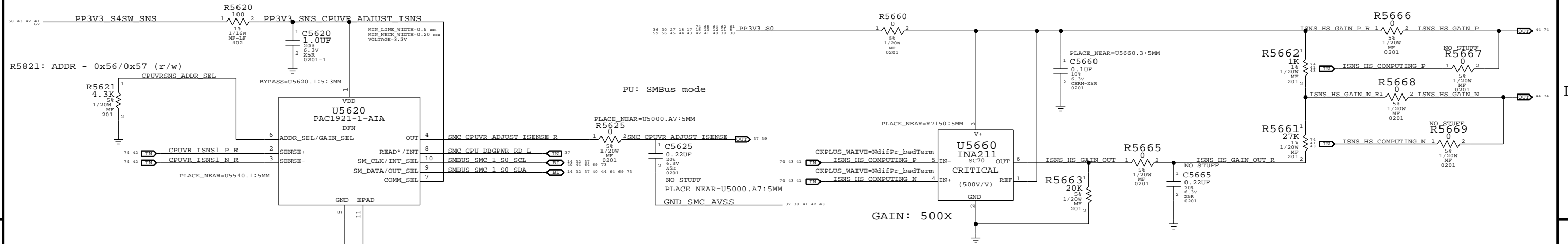
Apple Inc.

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 REVISION <E4LABEL>
 BRANCH <BRANCH>
 PAGE 55 OF 121
 SHEET 42 OF 76

ICS3 : Adjustable Gain CPU VR Current

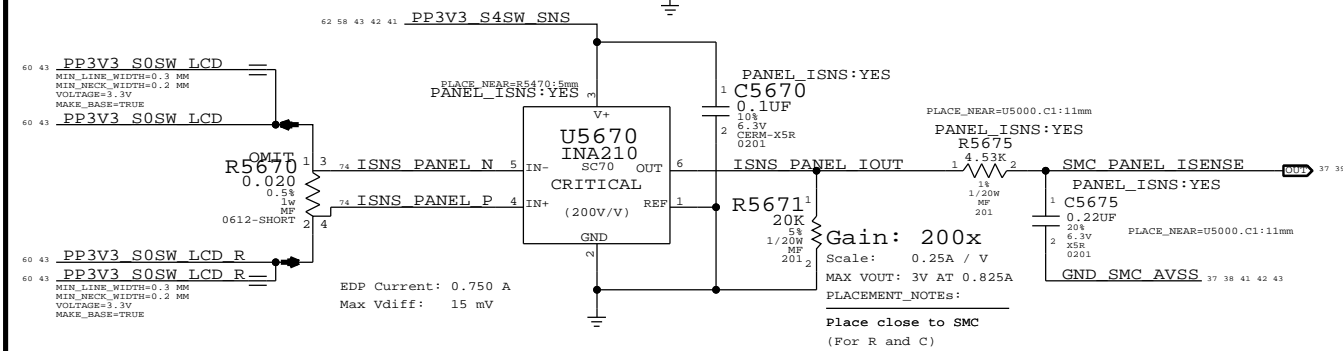
Sense Pins gain stage for U5800 (EMC1704)



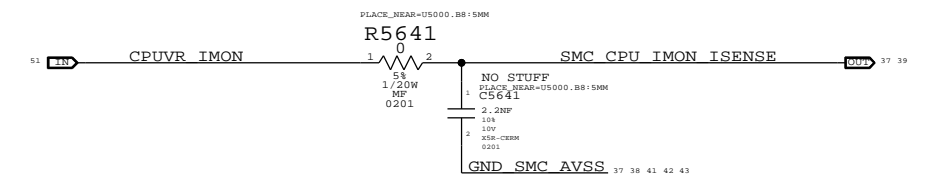
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the minimum current threshold at 0.100mA

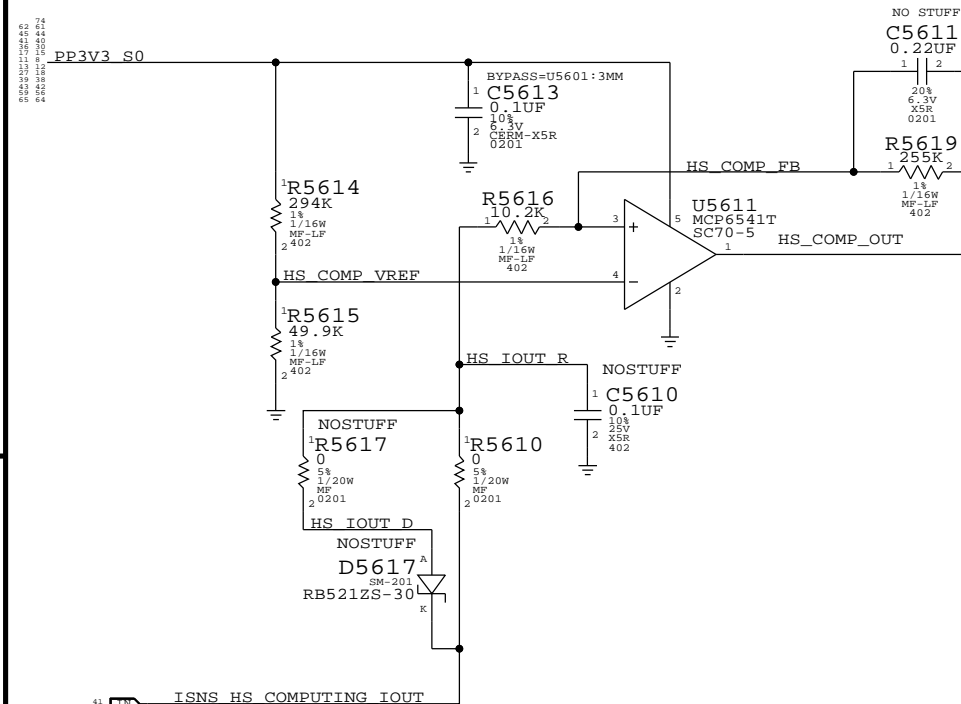
ILDC :LCD Panel Current Sense / Filter



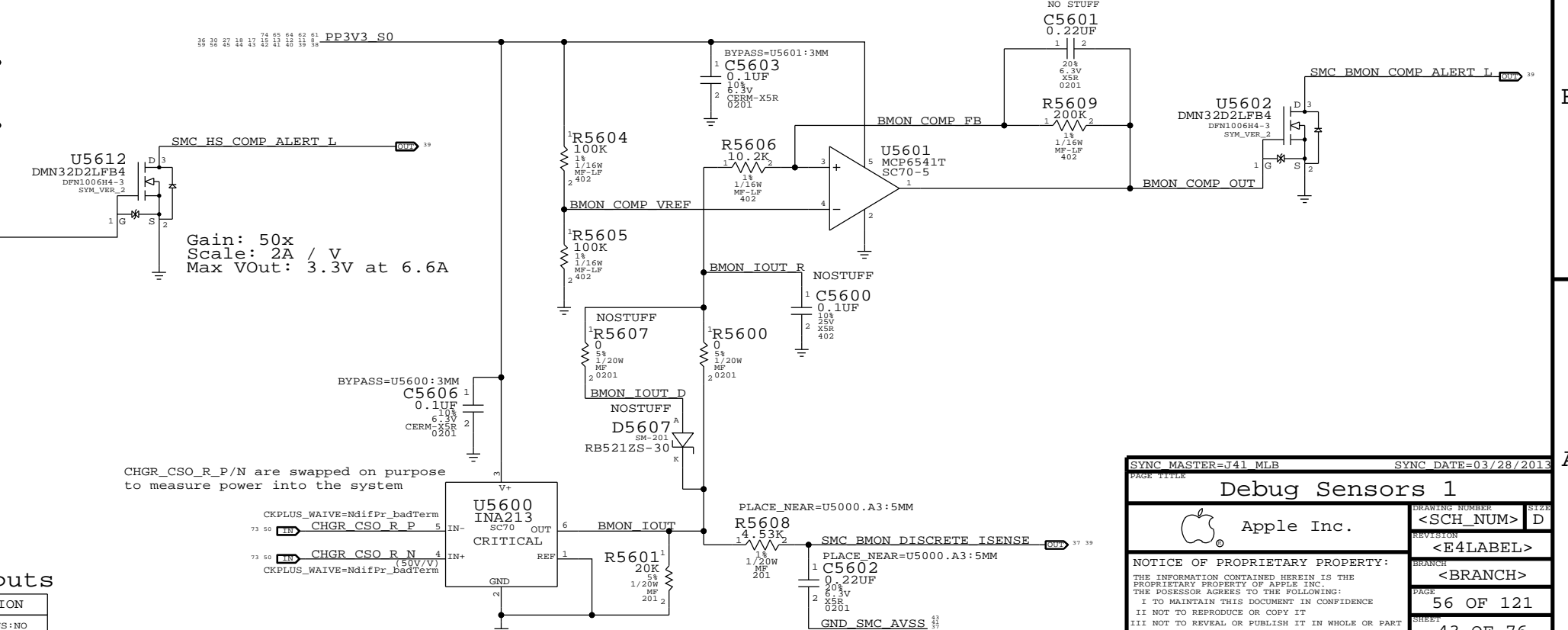
VR IMON Current Sense Filter



Discrete High side Current threshold



BMON : Discrete BMON Current Sense / Filter



Vref = 0.406mV Vth = 0.442 = 1A from Battery
 Vtl = 0.290mV = 0.687A from battery
 Hysteresis TBD based on RC value changes

CHGR_CSO_R/P/N are swapped on purpose to measure power into the system

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=J41 MLB SYNC DATE=03/28/2013

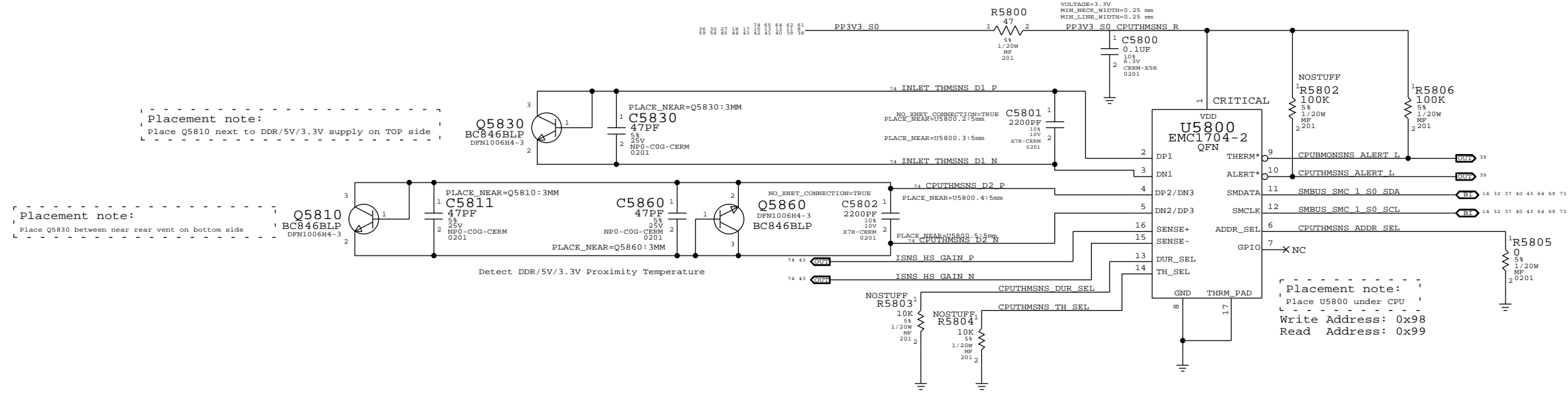
Debug Sensors 1

Apple Inc.

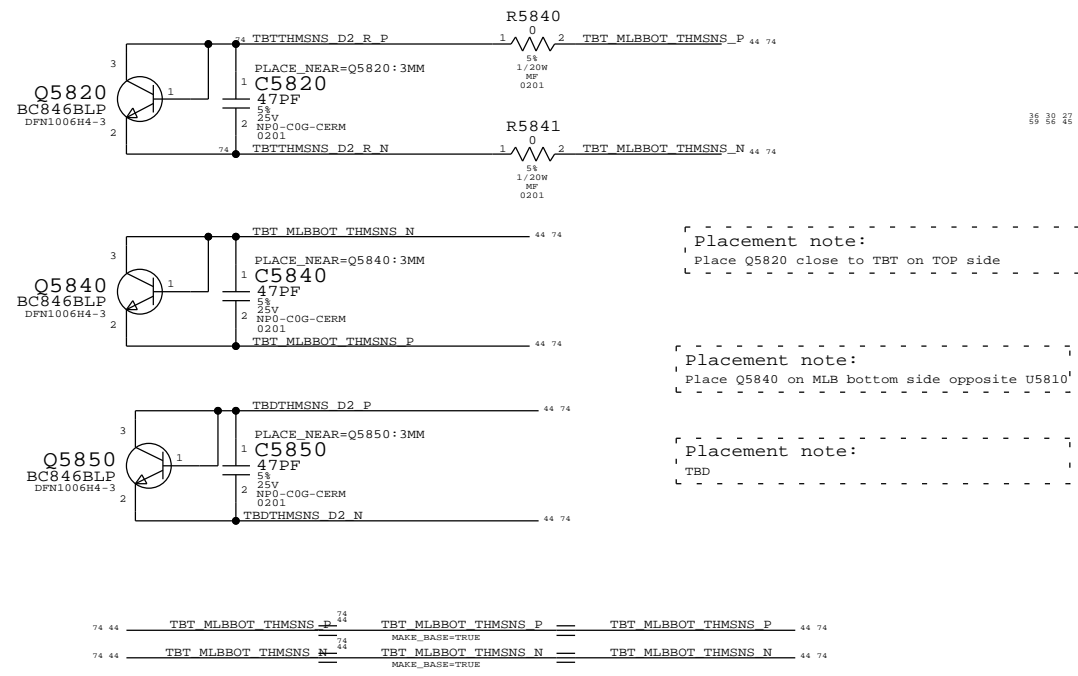
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 REVISION: <E4LABEL>
 BRANCH: <BRANCH>
 PAGE: 56 OF 121
 SHEET: 43 OF 76

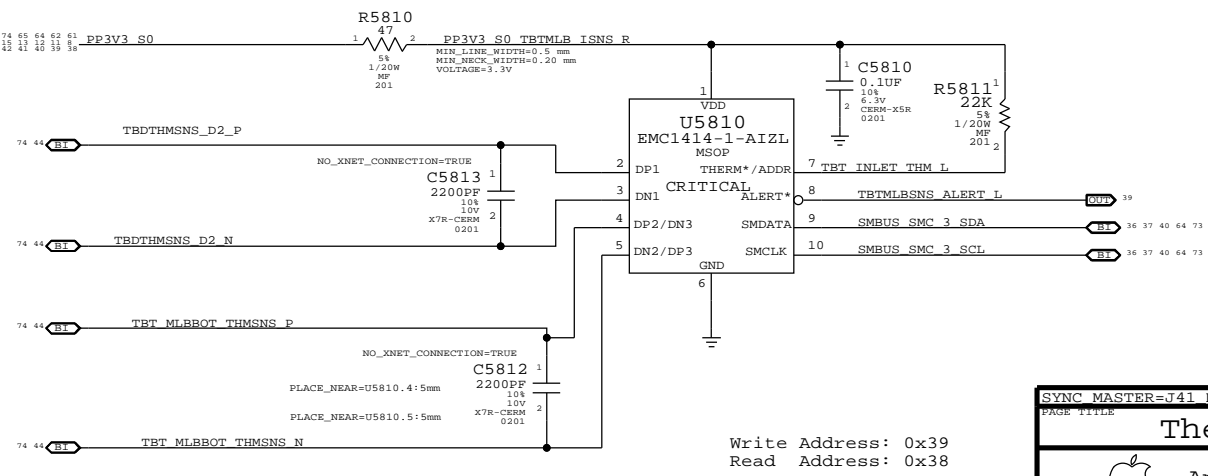
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors

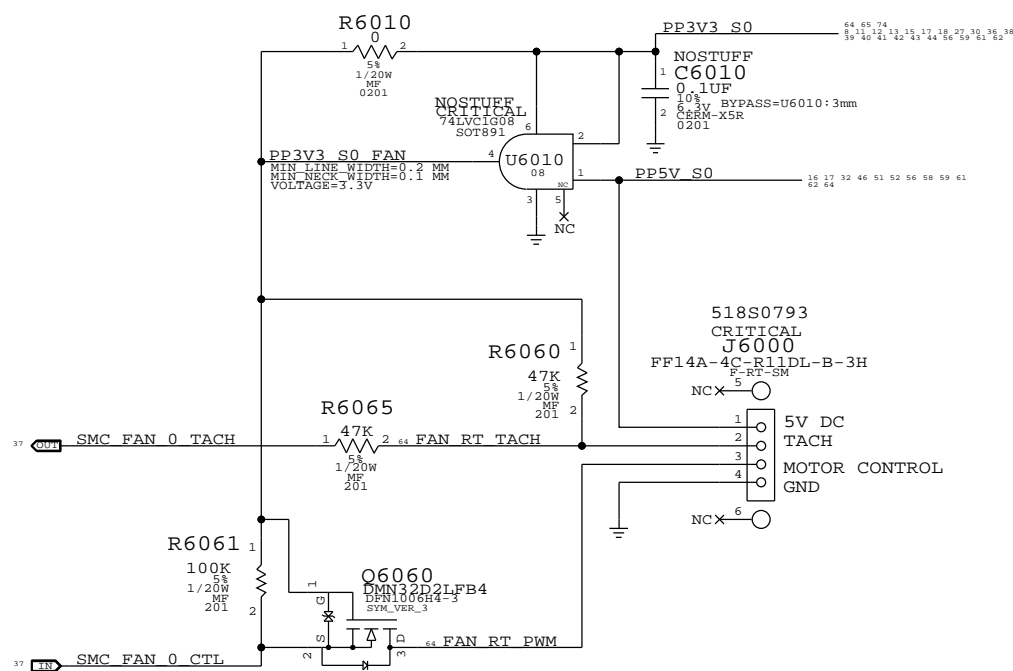


TBT, MLBBOT and TBD Temp Sensor



SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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		<BRANCH>	
		PAGE	58 OF 121
		SHEET	44 OF 76

FAN CONNECTOR



SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
Fan			
		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		PAGE	60 OF 121
		SHEET	45 OF 76

D

D

C

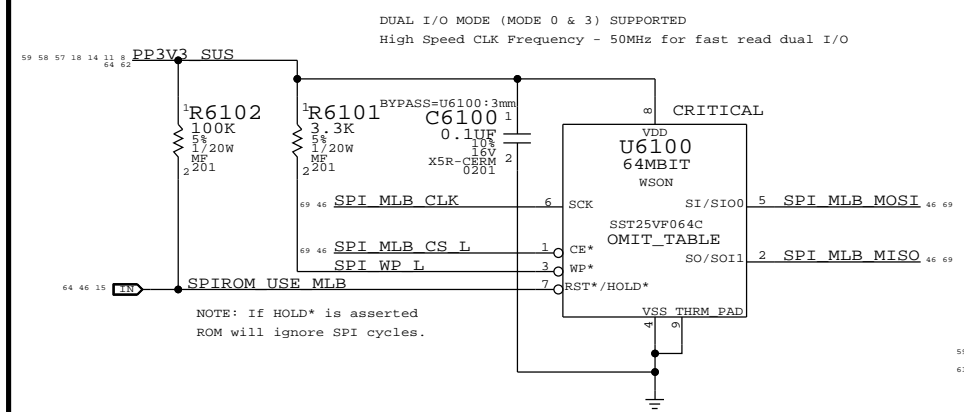
C

B

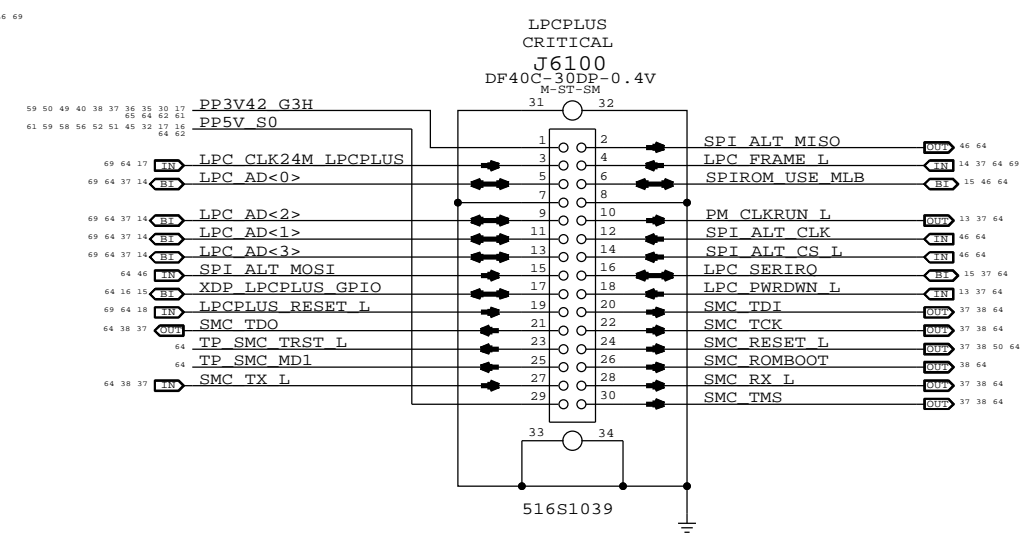
B

A

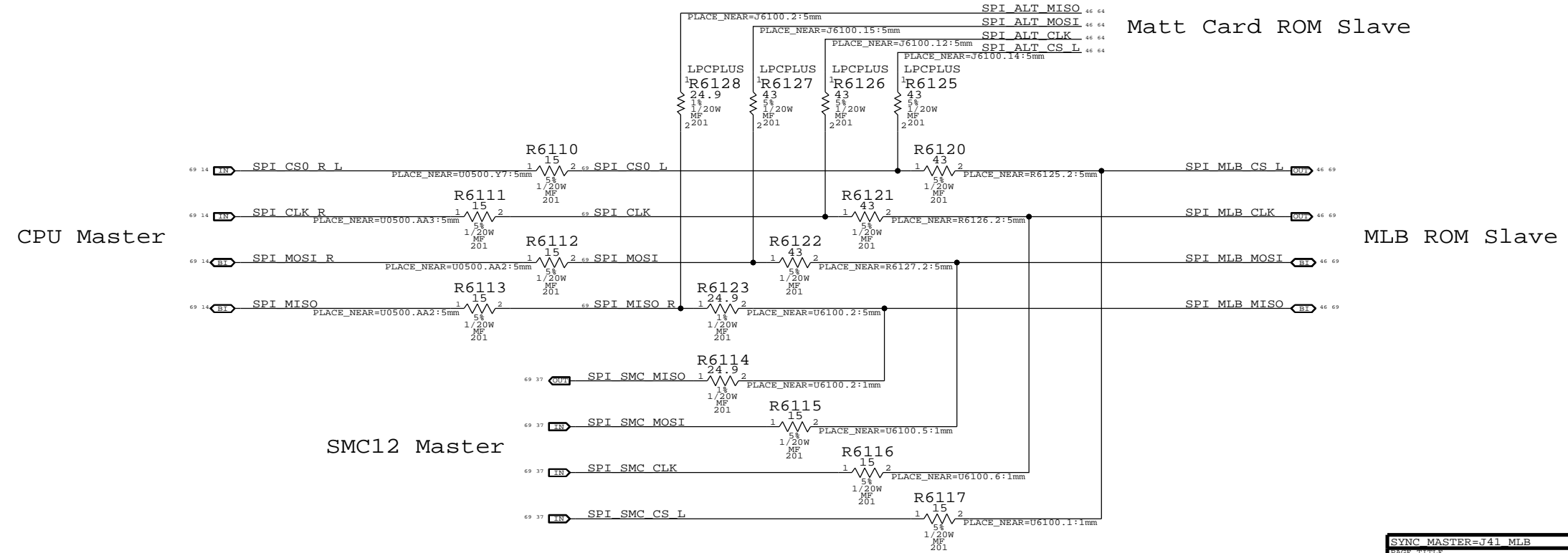
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LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=J41 MLB		SYNC DATE=04/02/2013	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
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		SHEET	46 OF 76

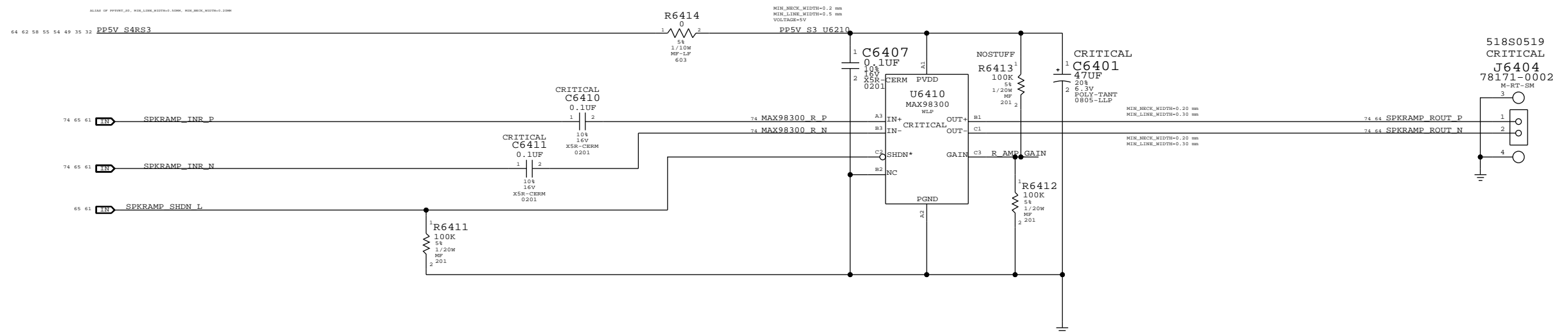
8 7 6 5 4 3 2 1

SPEAKER AMPLIFIERS

APN: 353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ
GAIN 6DB

Right Speaker Connector



D

D

C

C

B

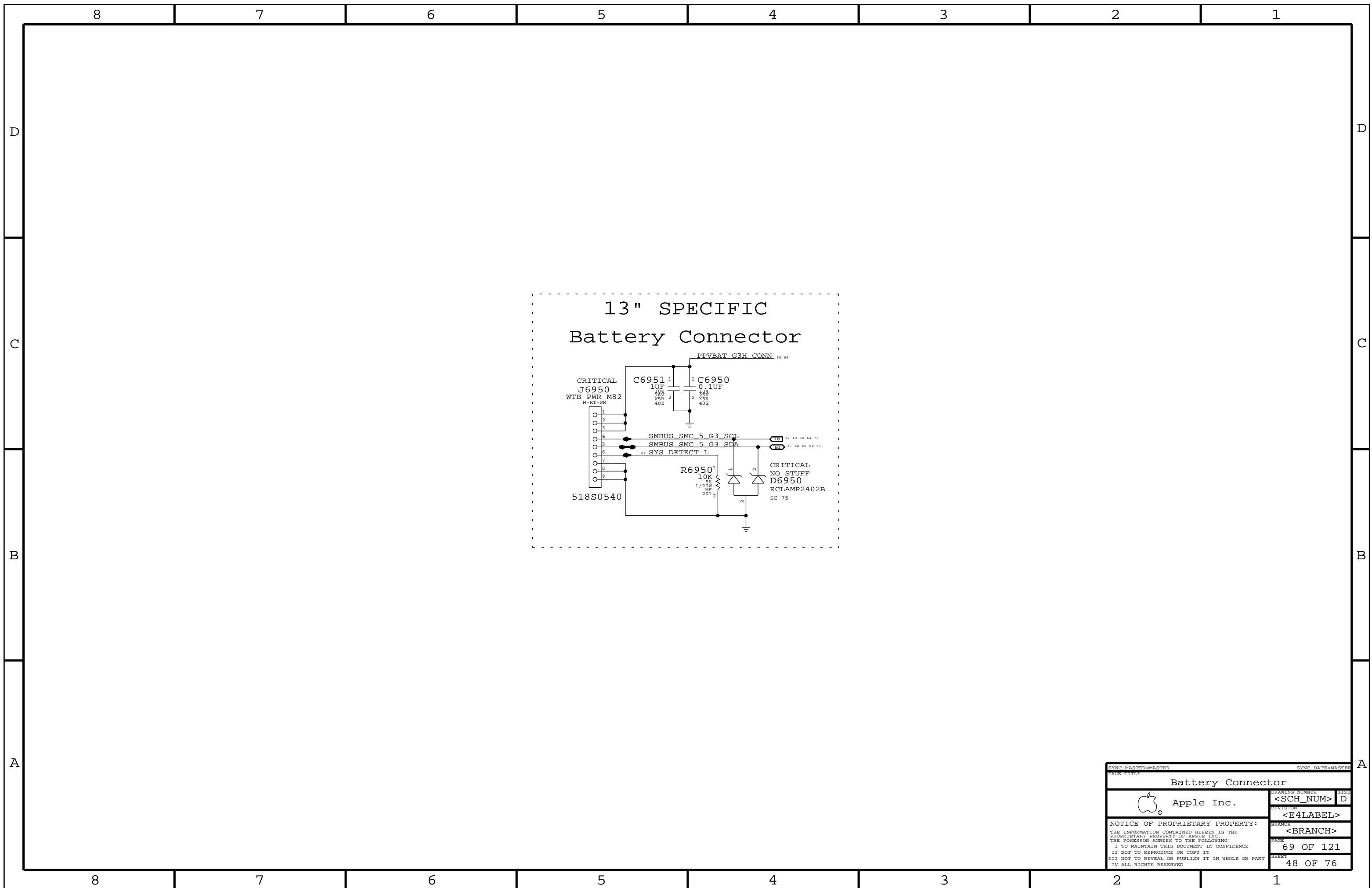
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A

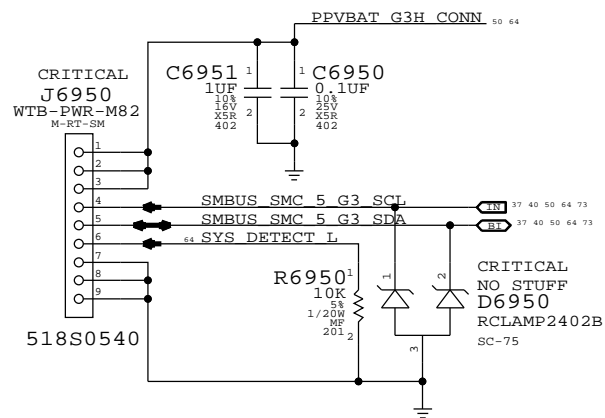
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8 7 6 5 4 3 2 1

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE Audio: Speaker Amp			
DRAWING NUMBER <SCH_NUM>		SIZE D	
REVISION <E4LABEL>		BRANCH <BRANCH>	
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PAGE 64 OF 121		SHEET 47 OF 76	



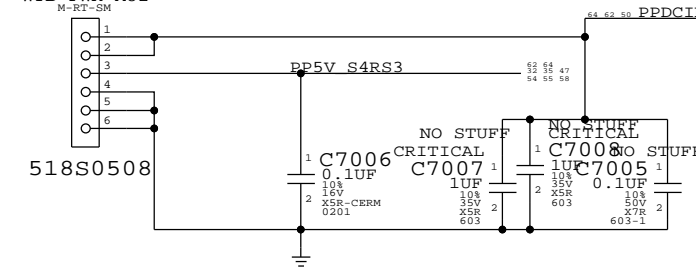
13" SPECIFIC Battery Connector



SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE Battery Connector			
DRAWING NUMBER <SCH_NUM>		SIZE D	
REVISION <E4LABEL>		BRANCH <BRANCH>	
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PAGE 69 OF 121		SHEET 48 OF 76	

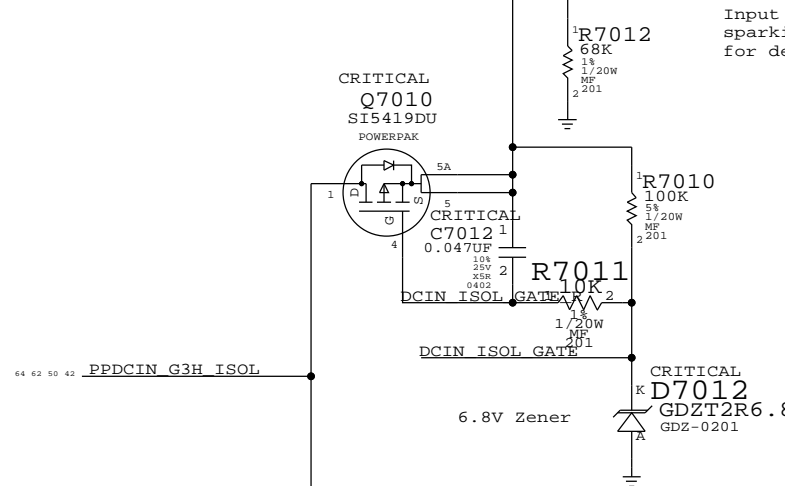
MLB to LIO Power Cable Connector

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM



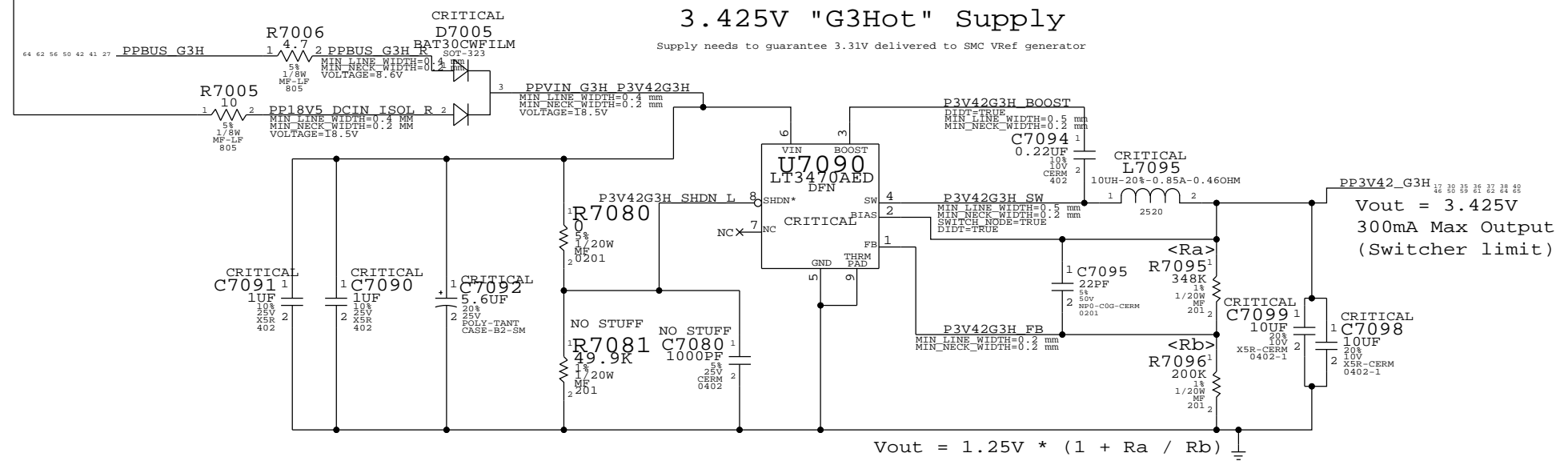
Input impedance of 68K meets sparkitecture requirements for detection of B121 (16.5V)

CRITICAL
Q7010
SI5419DU
POWERPAK



3.425V "G3Hot" Supply

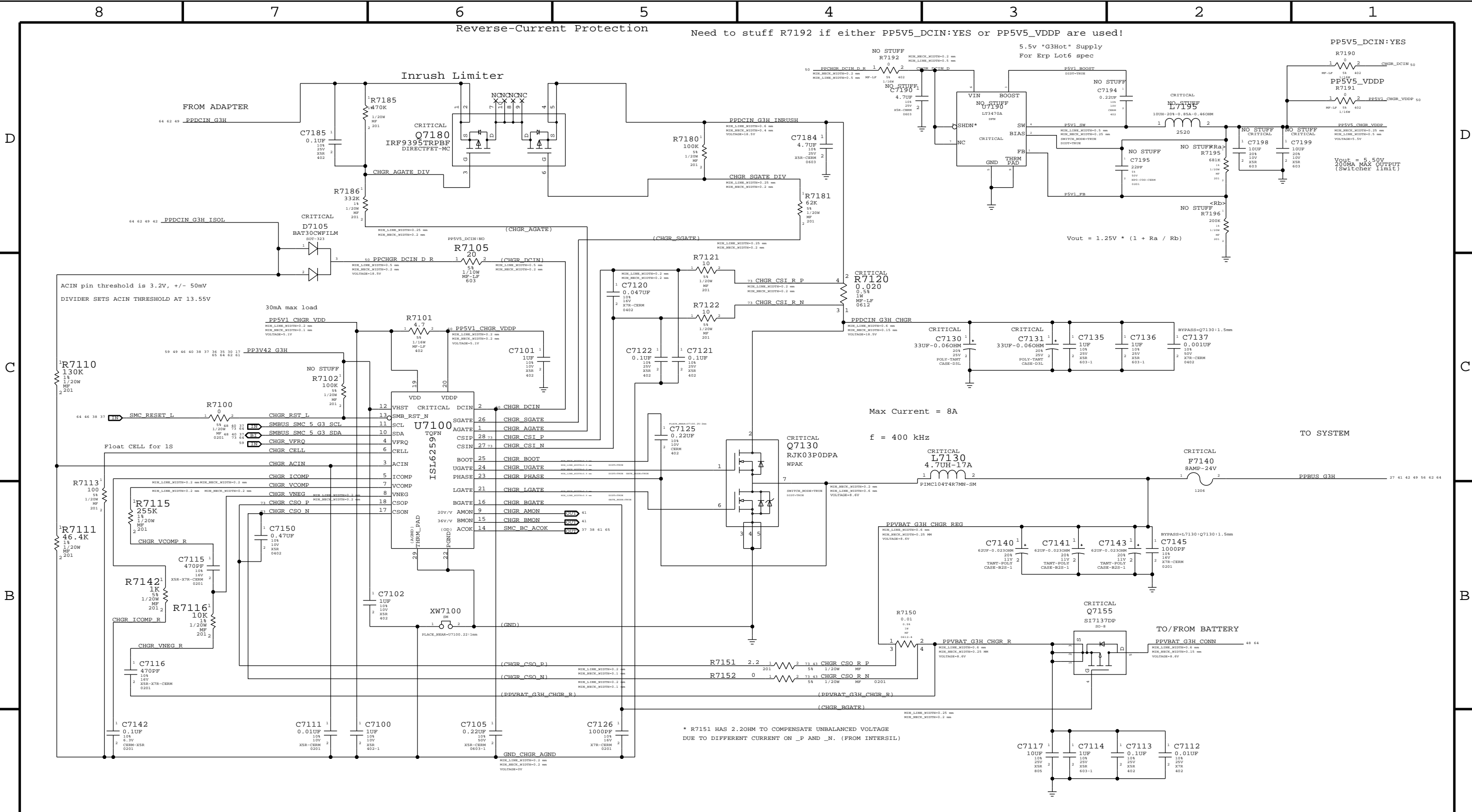
Supply needs to guarantee 3.31V delivered to SMC Vref generator



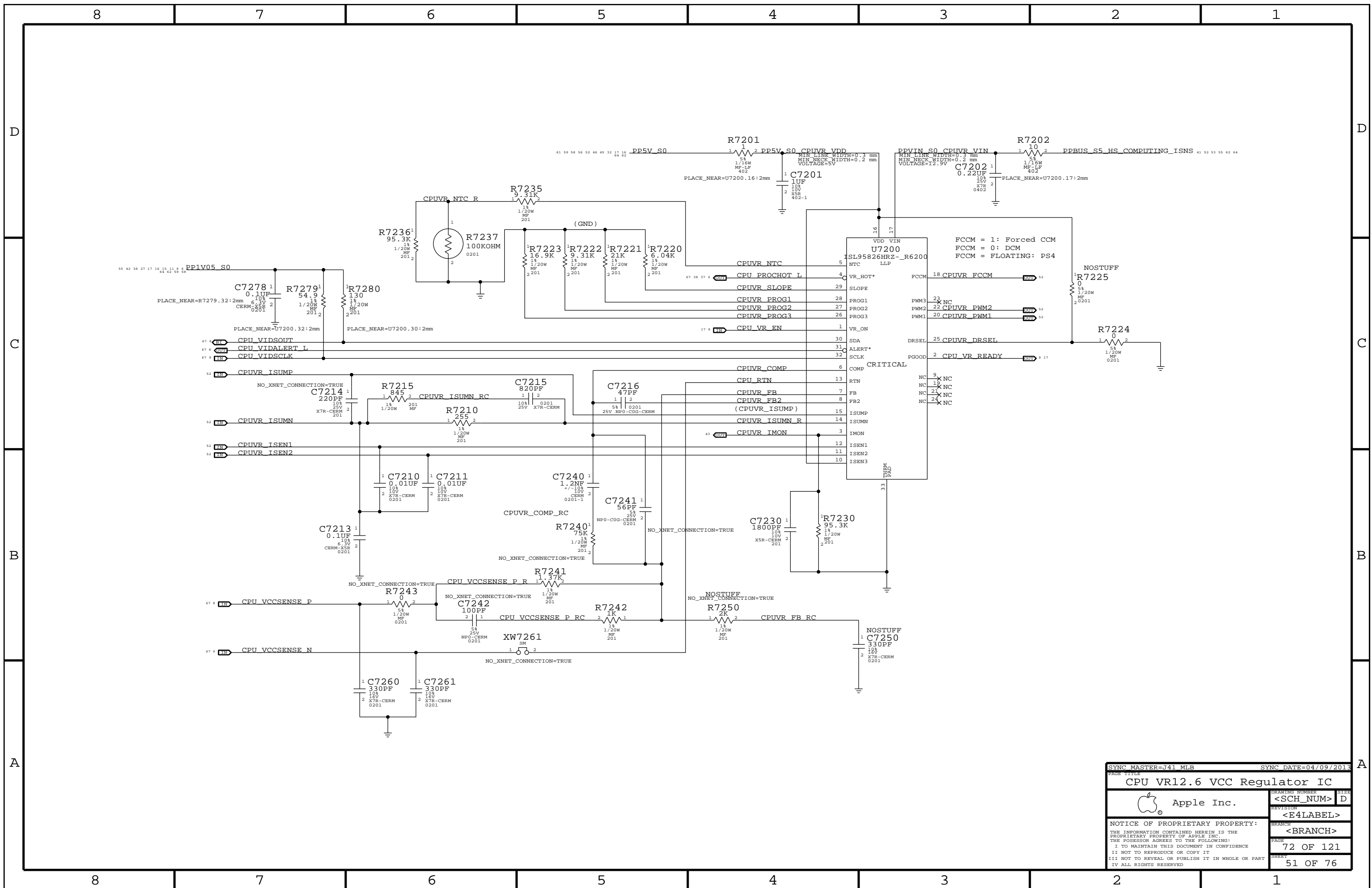
Vout = 3.425V
300mA Max Output
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

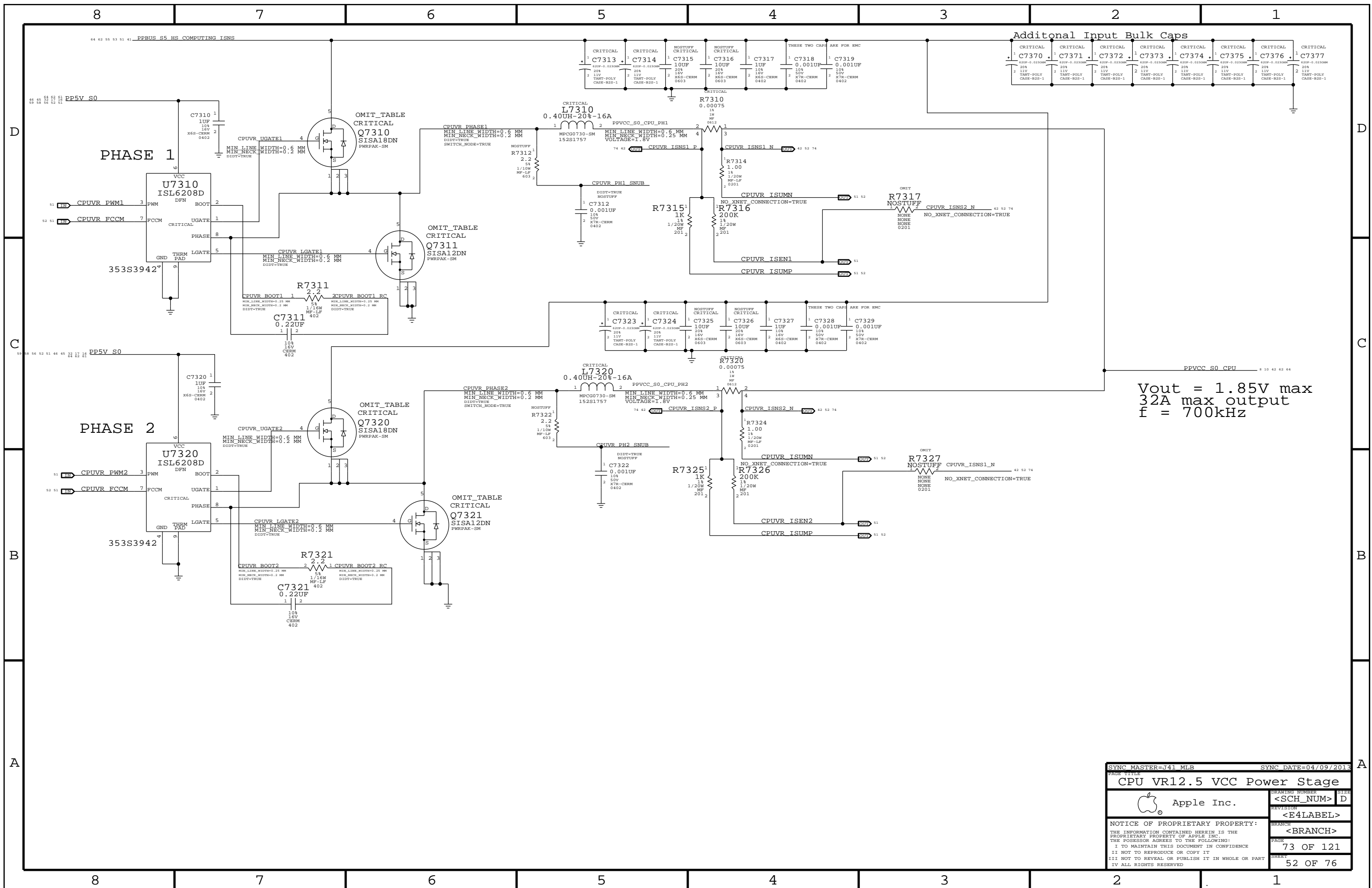
SYNC MASTER=141 MLB		SYNC DATE=02/06/2013	
PAGE TITLE DC-In & G3H Supply			
Apple Inc.		DRAWING NUMBER <SCH_NUM>	SIZE D
		REVISION <E4LABEL>	BRANCH <BRANCH>
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SYNC MASTER=J41 MLB		SYNC DATE=02/09/2013	
PAGE TITLE PBus Supply & Battery Charger			
DRAWING NUMBER <SCH_NUM>		SIZE D	
REVISION <E4LABEL>		BRANCH <BRANCH>	
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PAGE 71 OF 121		SHEET 50 OF 76	



SYNC MASTER=J41 MLB		SYNC DATE=04/09/2013	
CPU VR12.6 VCC Regulator IC			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		<E4LABEL>	
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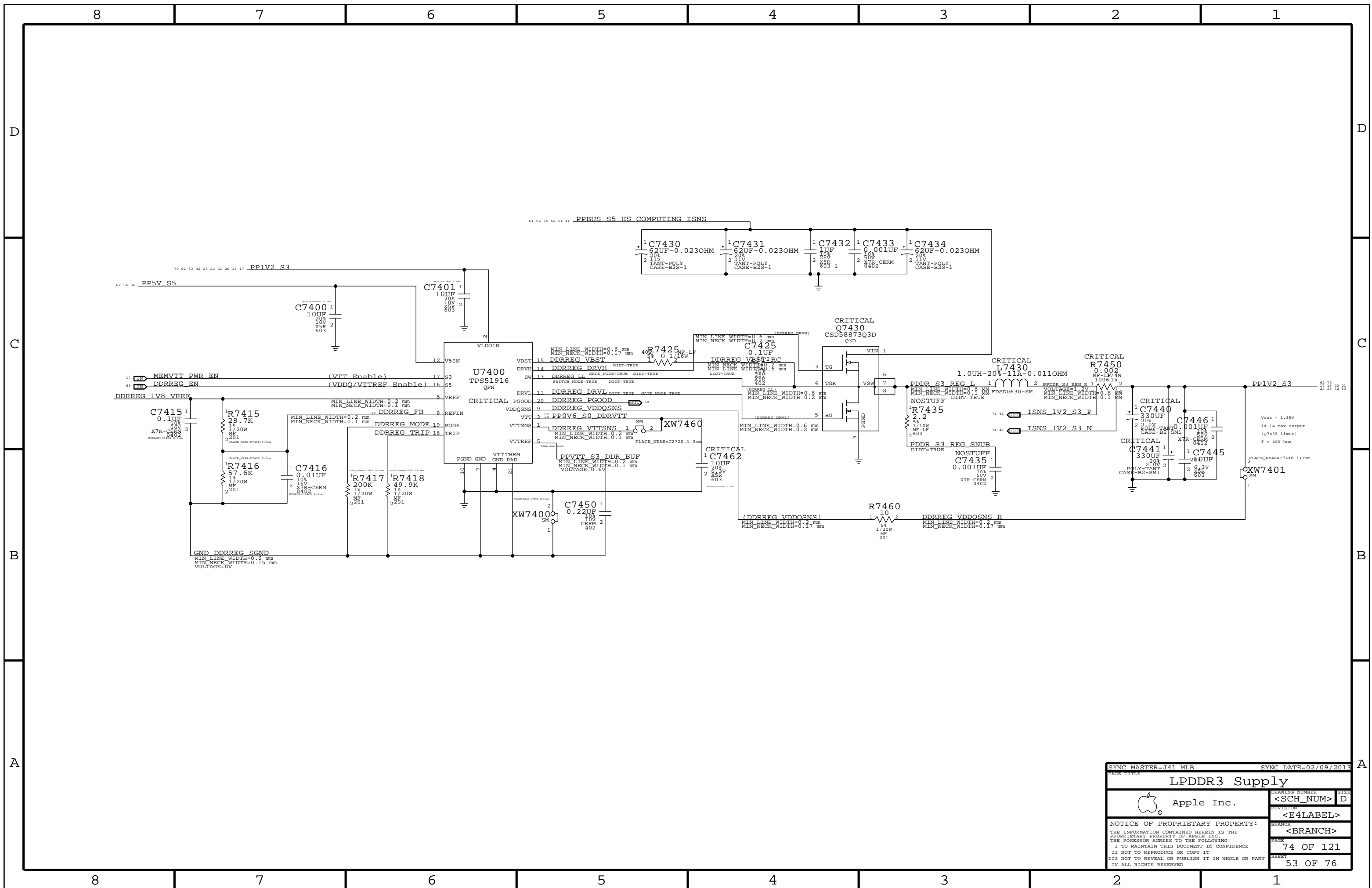


Additional Input Bulk Caps

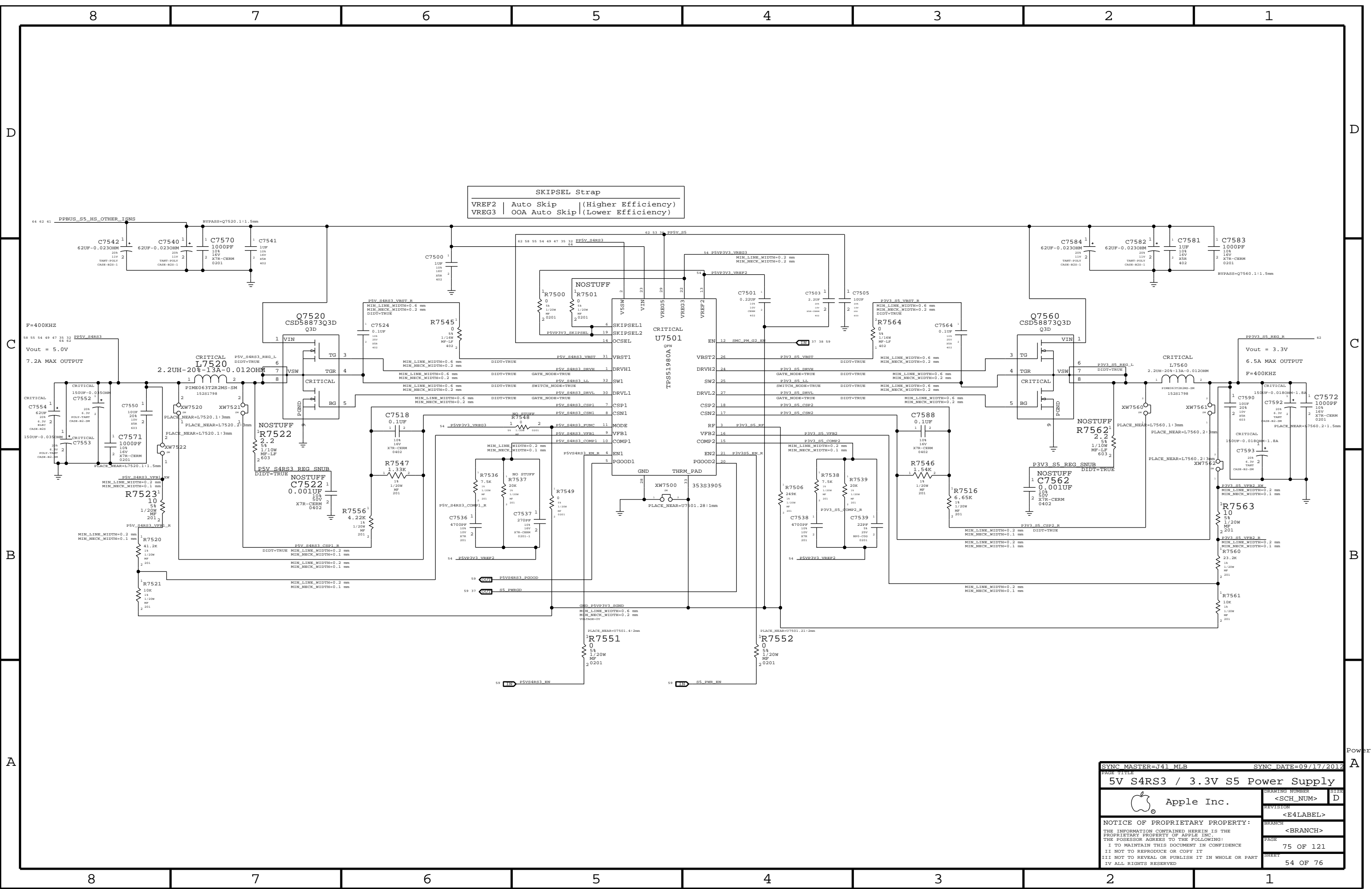
CRITICAL	CRITICAL	CRITICAL	CRITICAL	CRITICAL	CRITICAL	CRITICAL	CRITICAL
C7370	C7371	C7372	C7373	C7374	C7375	C7376	C7377
100pF-0.0230mm	100pF-0.0230mm	100pF-0.0230mm	100pF-0.0230mm	100pF-0.0230mm	100pF-0.0230mm	100pF-0.0230mm	100pF-0.0230mm
200	200	200	200	200	200	200	200
11V	11V	11V	11V	11V	11V	11V	11V
TANT-POLY	TANT-POLY	TANT-POLY	TANT-POLY	TANT-POLY	TANT-POLY	TANT-POLY	TANT-POLY
CASE-B2S-1	CASE-B2S-1	CASE-B2S-1	CASE-B2S-1	CASE-B2S-1	CASE-B2S-1	CASE-B2S-1	CASE-B2S-1

Vout = 1.85V max
 32A max output
 f = 700kHz

SYNC MASTER=J41 MLB		SYNC DATE=04/09/2013	
CPU VR12.5 VCC Power Stage			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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SYNC MASTER=J41 MLB		SYNC DATE=02/09/2013	
PAGE TITLE			
LPDDR3 Supply			
		DRAWING NUMBER	SIZE
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		PAGE	74 OF 121
		SHEET	53 OF 76

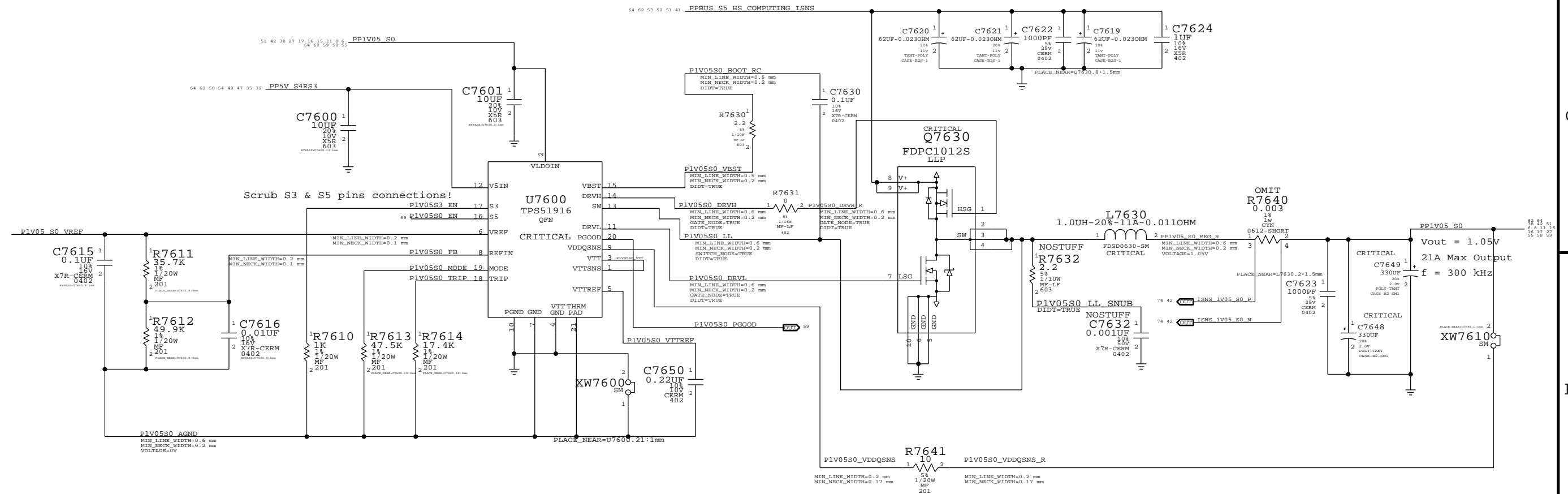


SKIPSEL Strap
 VREF2 | Auto Skip | (Higher Efficiency)
 VREG3 | OOA Auto Skip | (Lower Efficiency)

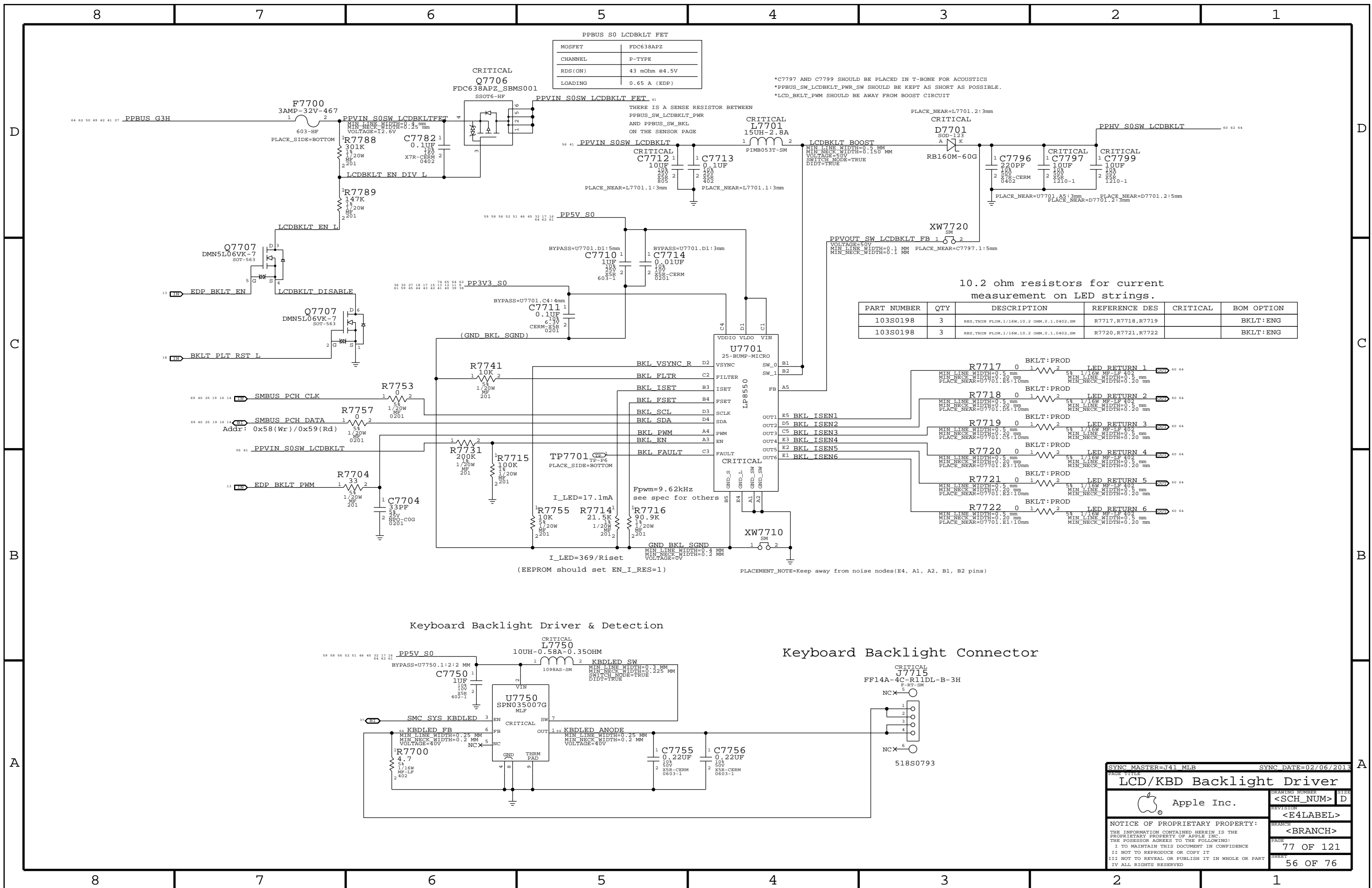
SYNC MASTER=J41 MLB		SYNC DATE=09/17/2012	
5V S4RS3 / 3.3V S5 Power Supply			
DRAWING NUMBER		SIZE	
<SCH_NUM>		D	
REVISION			
<E4LABEL>			
BRANCH			
<BRANCH>			
PAGE		75 OF 121	
SHEET		54 OF 76	

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1.05V S0 Regulator



SYNC MASTER=J41 MLB		SYNC DATE=03/28/2013	
PAGE TITLE			
1.05V S0 Power Supply			
DRAWING NUMBER		SIZE	
<SCH_NUM>		D	
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PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
 *PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
 *LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0.402, SM	R7717, R7718, R7719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0.402, SM	R7720, R7721, R7722		BKLT:ENG

Keyboard Backlight Driver & Detection

Keyboard Backlight Connector

SYNC MASTER=J41_MLB SYNC DATE=02/06/2013

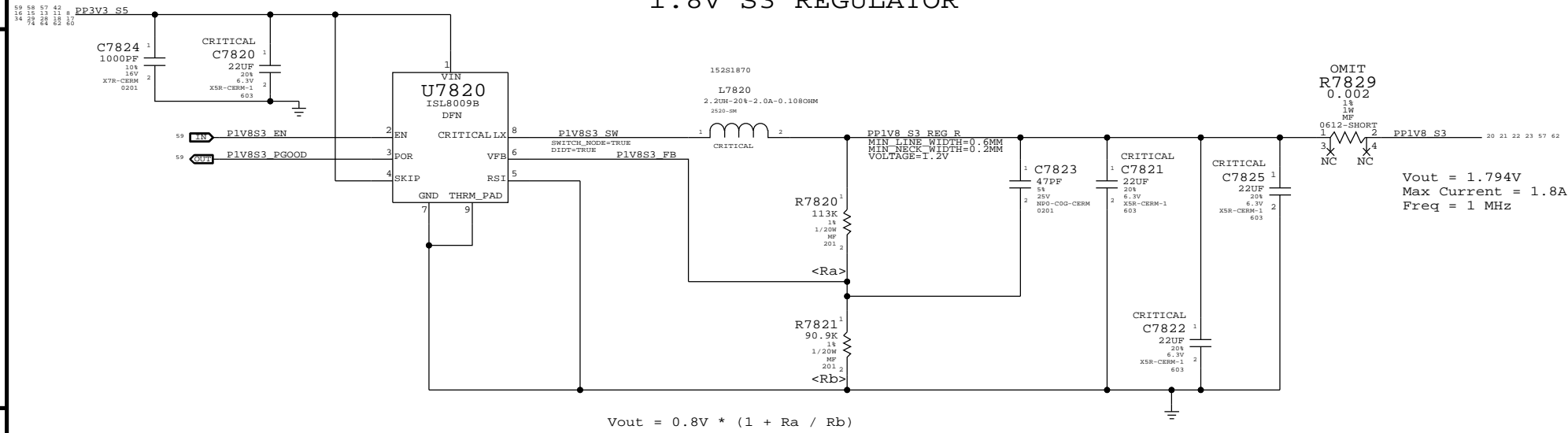
LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: <SCH_NUM> D
 REVISION: <E4LABEL>
 BRANCH: <BRANCH>
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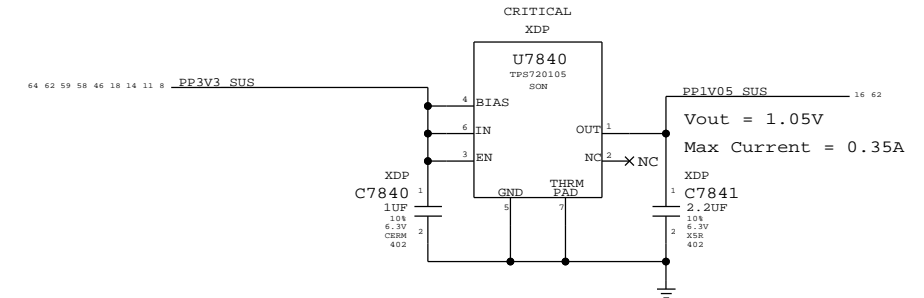
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1.8V S3 REGULATOR

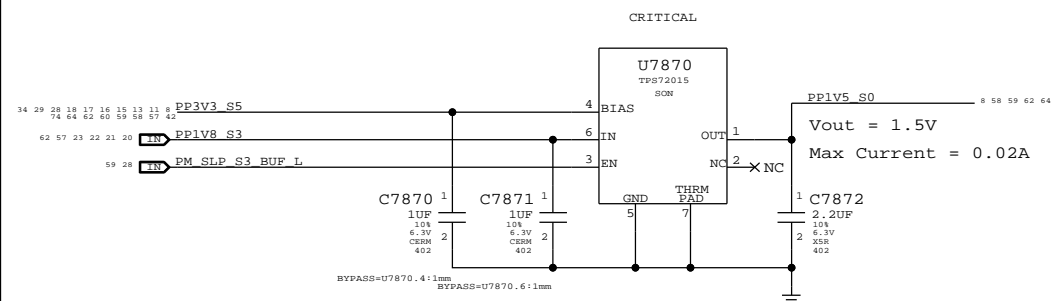


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO

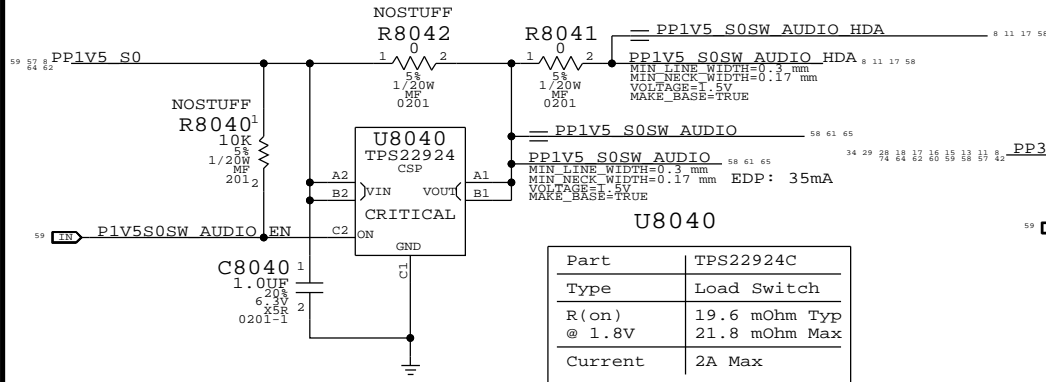


SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
Misc Power Supplies			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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1.5V S0 Audio Switch

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

3.3V SUS Switch



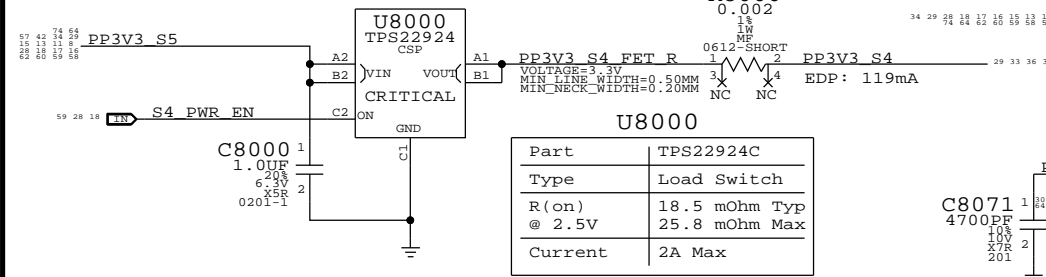
Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ
R(on) @ 2.5V	21.8 mOhm Max
Current	2A Max

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 2.5V	25.8 mOhm Max
Current	2A Max

1.05V PCH HSIO Switch

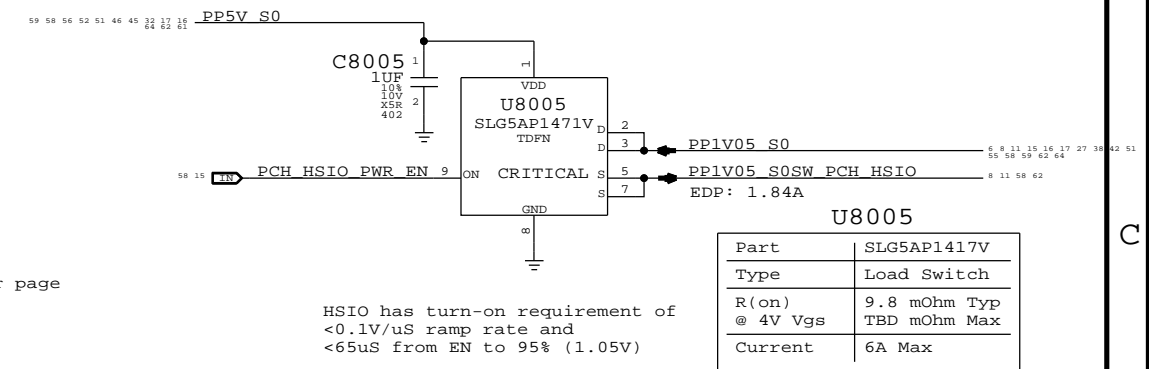
3.3V S4 Switch

3.3V SSD Switch



Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 2.5V	25.8 mOhm Max
Current	2A Max

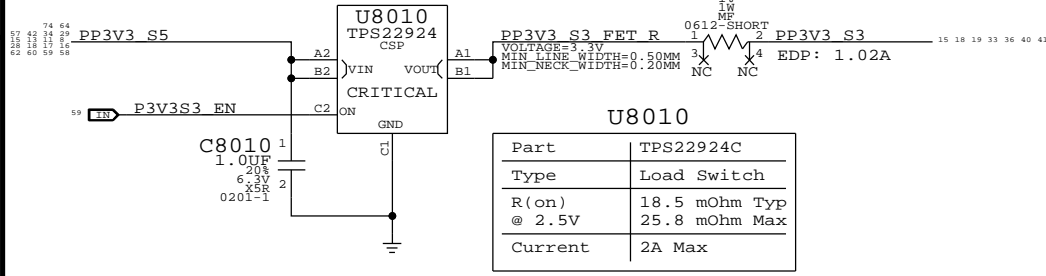
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ
R(on) @ 25C	8.5 mOhm Max
Current	5.3A Max



Part	SLG5AP1471V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ
R(on) @ 4V Vgs	TBD mOhm Max
Current	6A Max

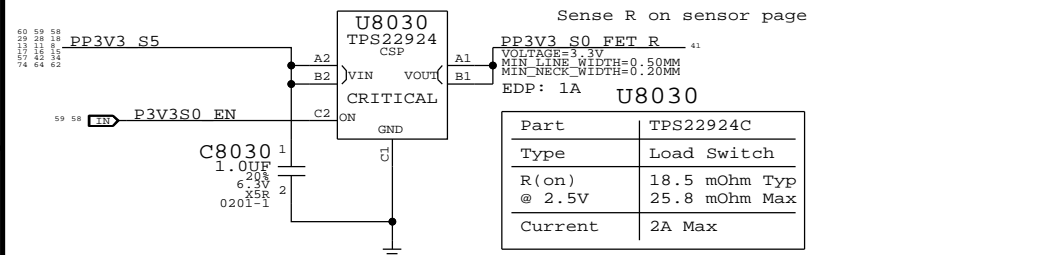
HSIO has turn-on requirement of <0.1V/uS ramp rate and <65uS from EN to 95% (1.05V)

3.3V S3 Switch



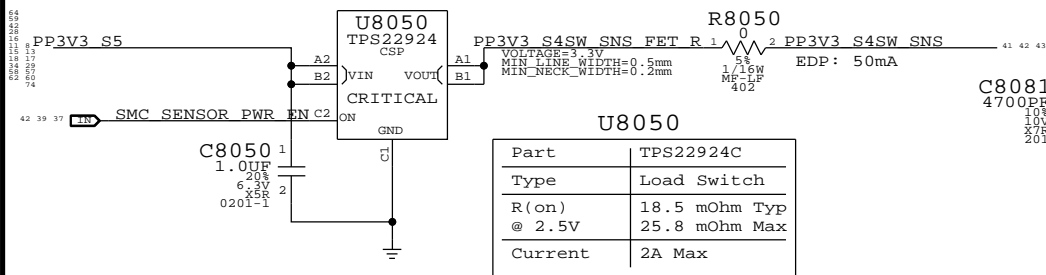
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 2.5V	25.8 mOhm Max
Current	2A Max

3.3V S0 Switch



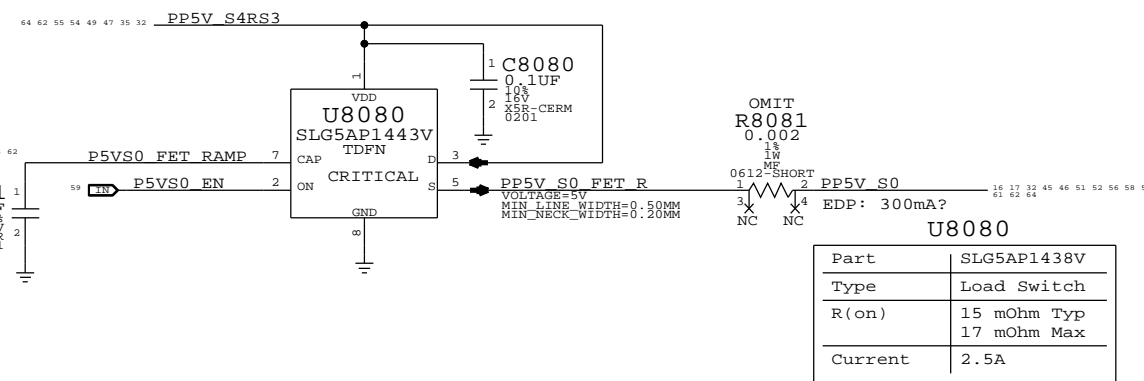
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 2.5V	25.8 mOhm Max
Current	2A Max

3.3V Sensor Switch



Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 2.5V	25.8 mOhm Max
Current	2A Max

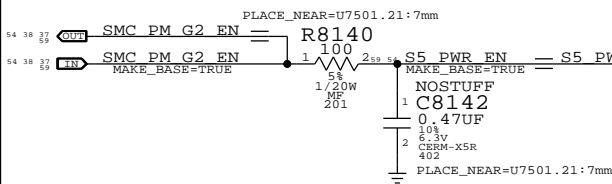
5V S0 Switch



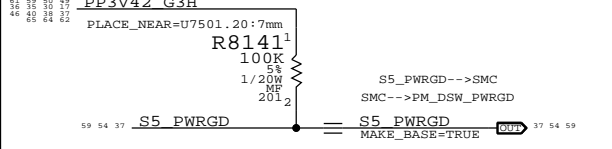
Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ
R(on)	17 mOhm Max
Current	2.5A

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
Power FETs			
Apple Inc.		DRAWING NUMBER	SIZE
<SCH_NUM>		D	
REVISION		<E4LABEL>	
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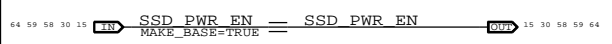
S5 Enables



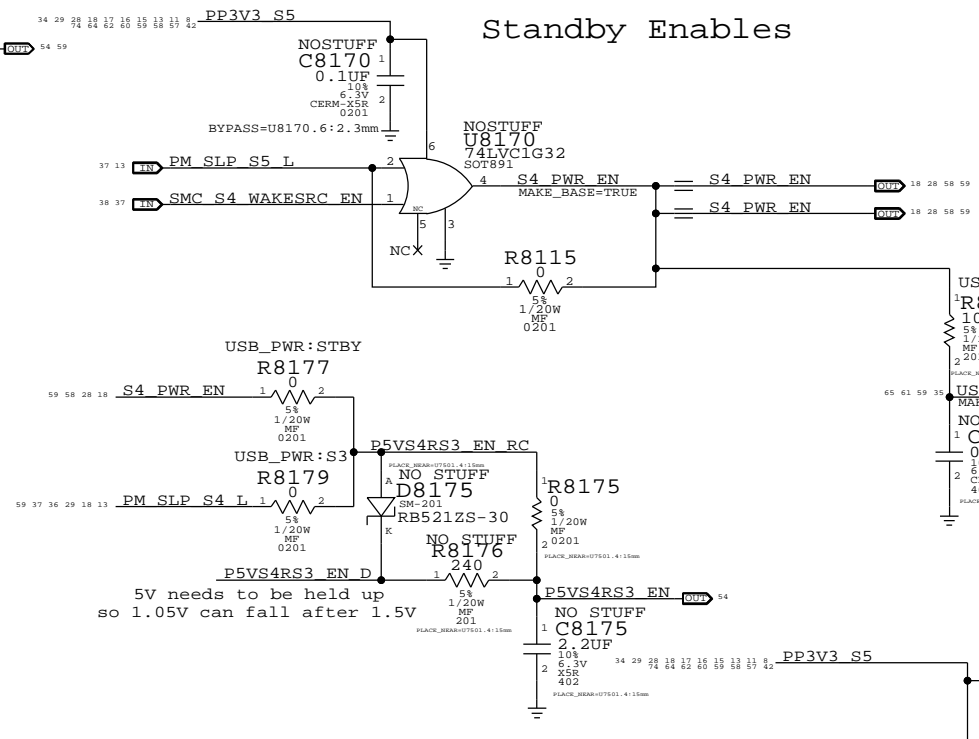
S5 Power Good



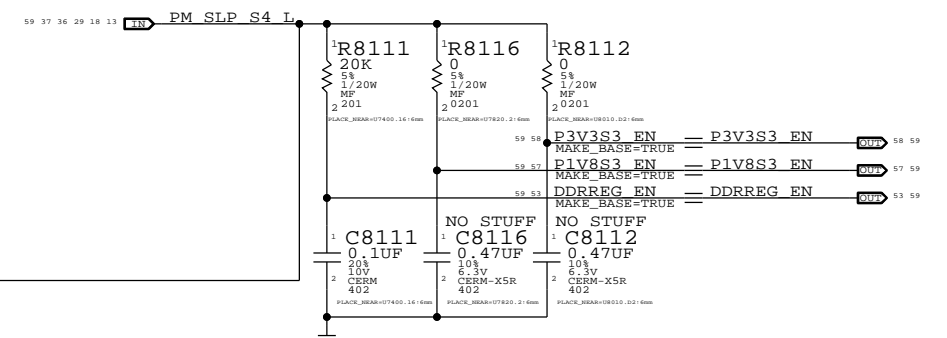
SSD Enable



Standby Enables



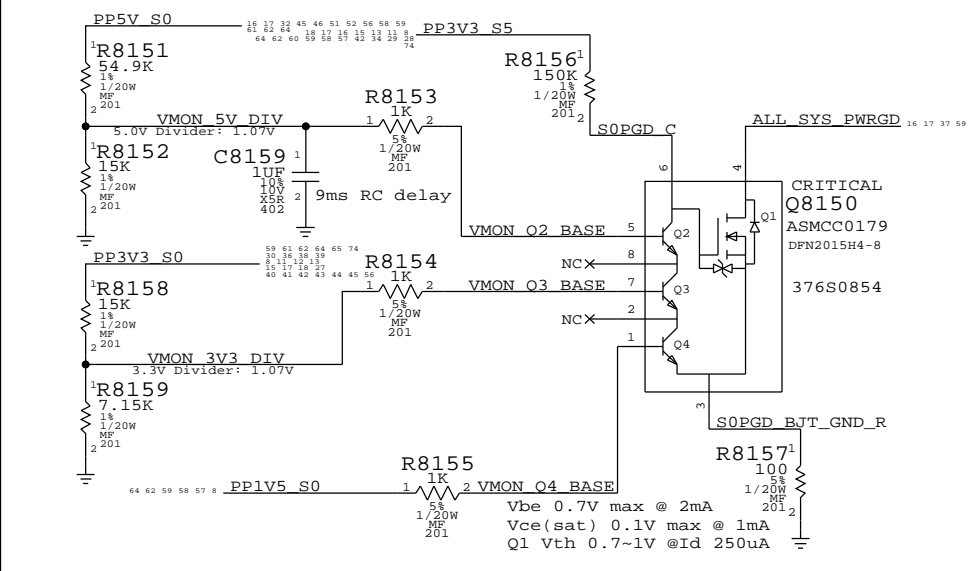
S3 Enables



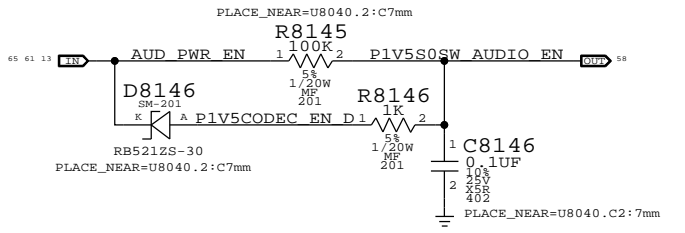
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_S2_ENABLE	SMC_S4_WAKE_SRC_EN	PM_STS_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S5_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (S3BnAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (S3Bn)	1	0	0	0	0	0	0

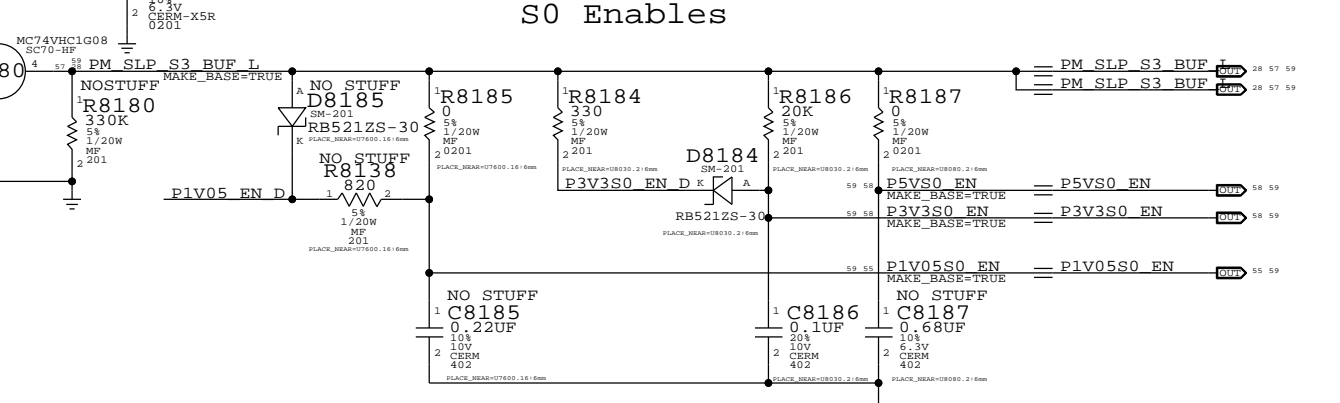
S0 Rail PGOOD (BJT Version)



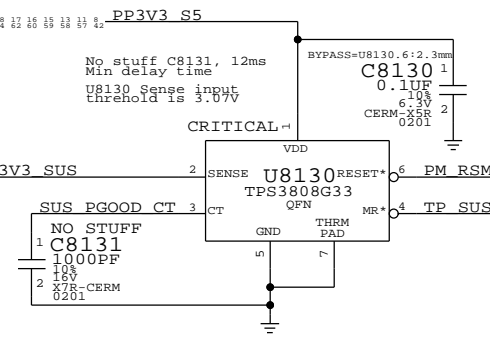
1.5V Codec Enable



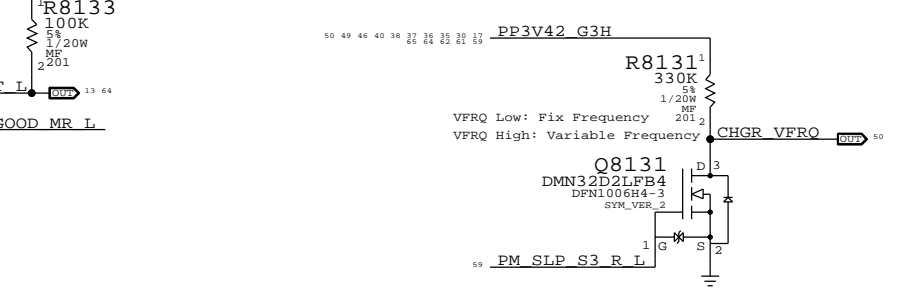
S0 Enables



3.3V SUS Detect

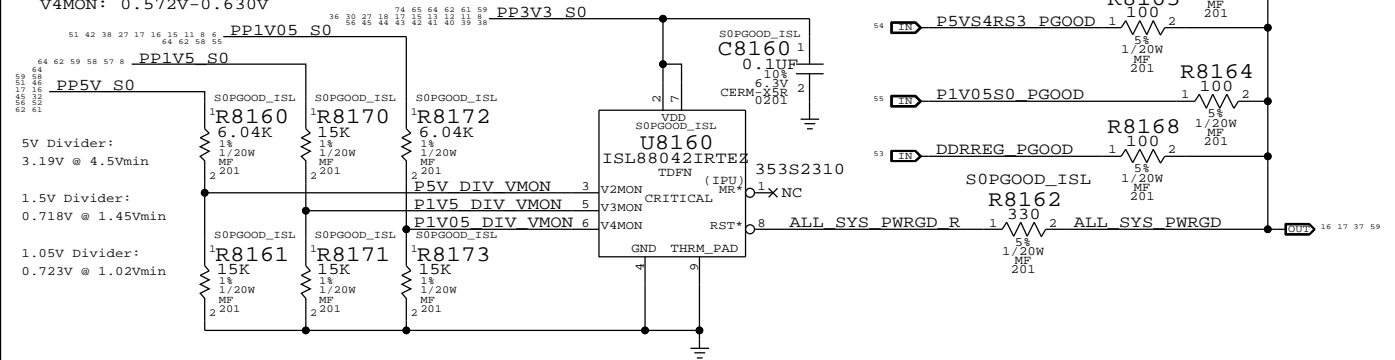


CHGR VFRQ Generation

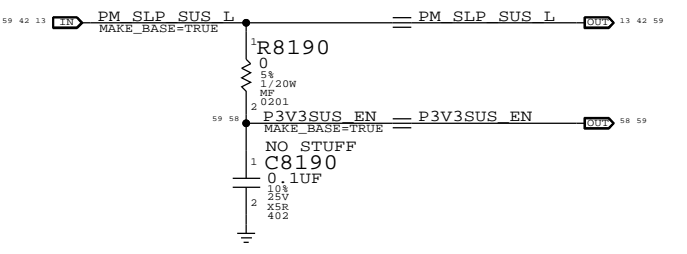


Thresholds:
 VDD: 2.734V-3.010V
 V2MON: 2.815V-3.099V
 V3MON: 0.572V-0.630V
 V4MON: 0.572V-0.630V

S0 Rail PGOOD Circuitry (ISL version used for development)



SUS Enables



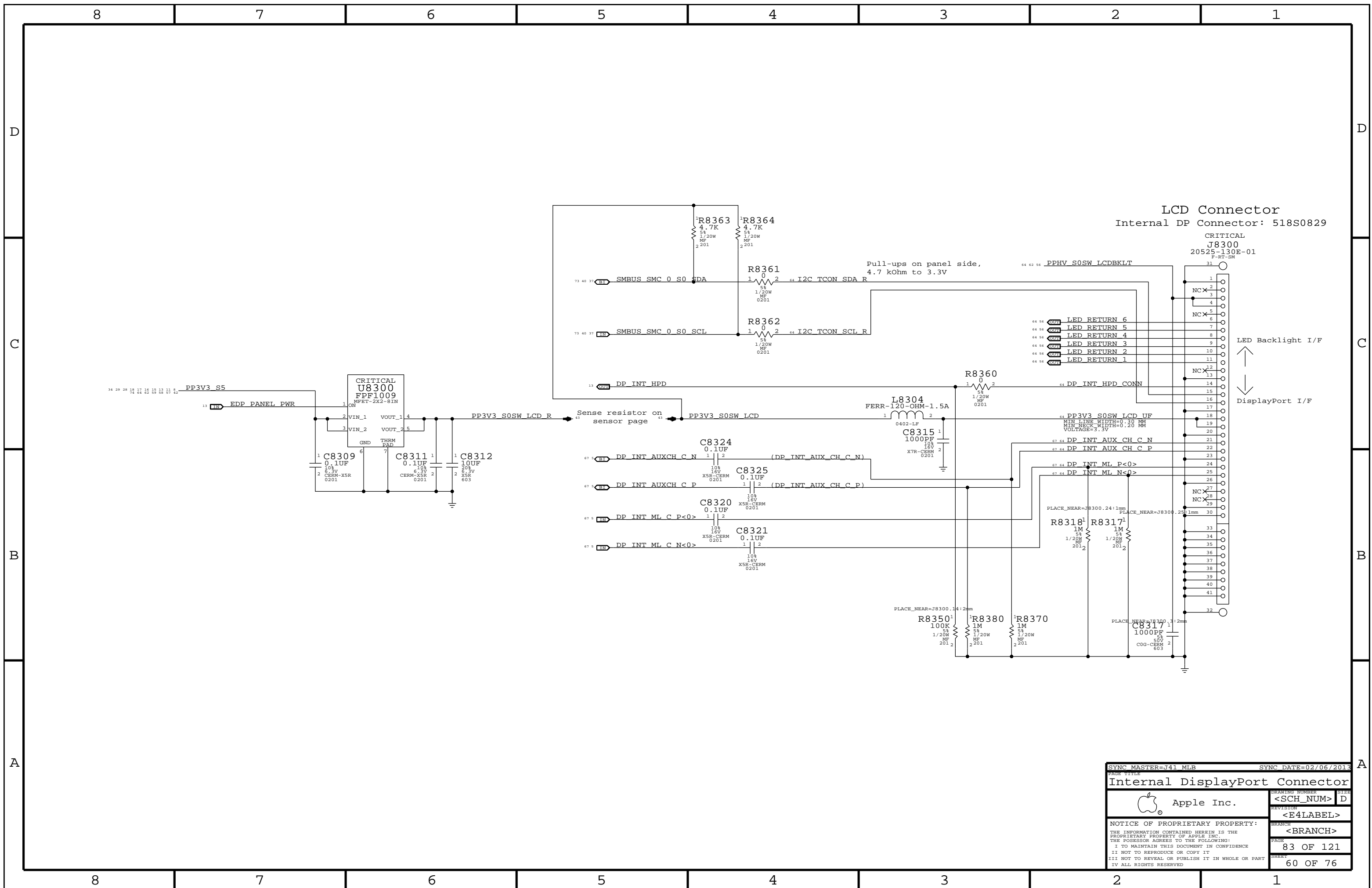
SYNC MASTER=J41 MLB SYNC DATE=02/06/2013

Power Control

Apple Inc.

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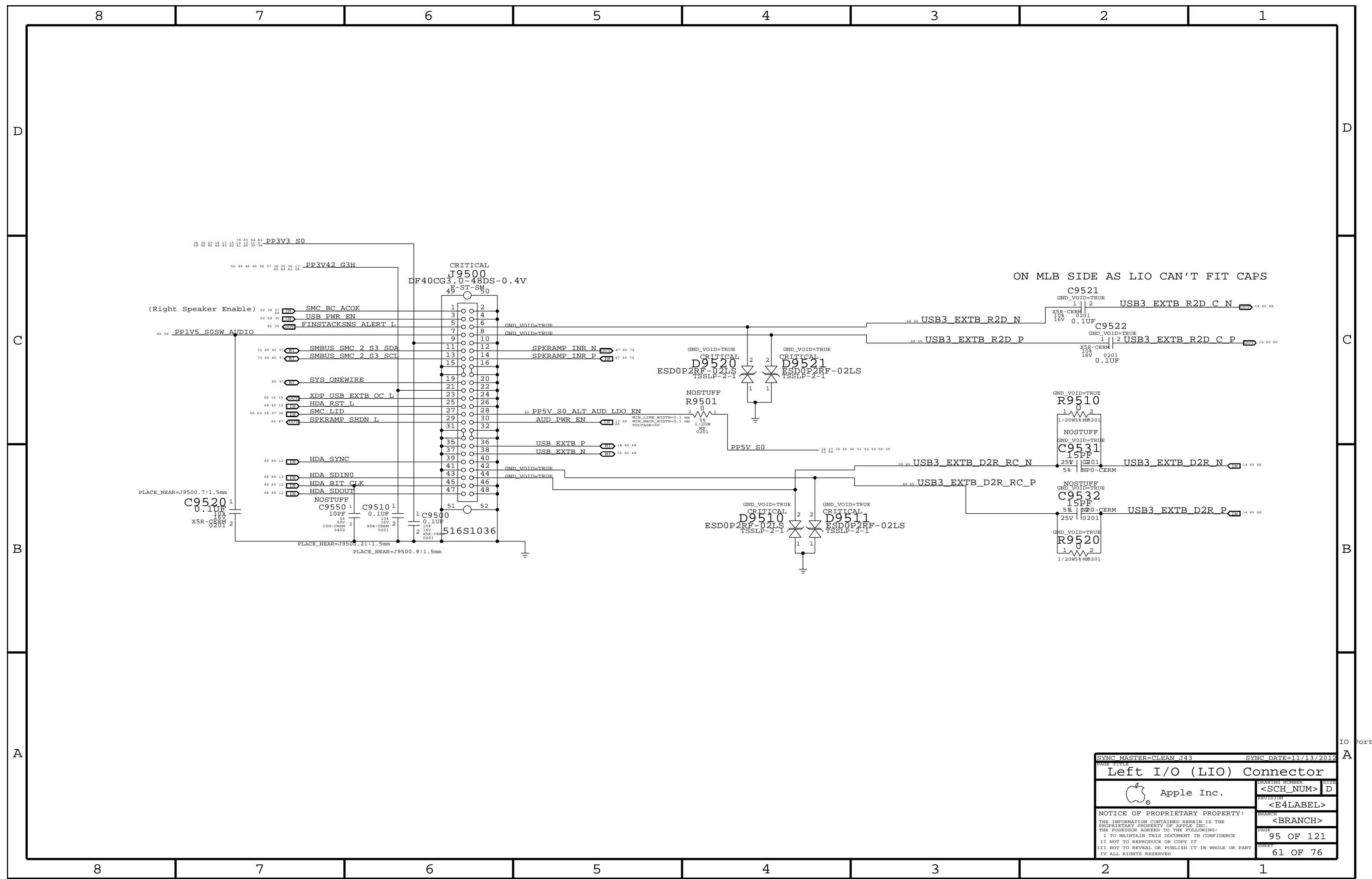


LCD Connector
Internal DP Connector: 518S0829

CRITICAL
J8300
20525-130E-01
P-RT-SM

LED Backlight I/F
↑
DisplayPort I/F
↓

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
Internal DisplayPort Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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Left I/O (LIO) Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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IO Ports
A

LPDDR3 Command/Address

Memory Bit/Byte Swizzle

Command/Address	MAKE_BASE	MEM A	MEM B
=MEM A A<5>	TRUE	MEM A CAA<0>	
=MEM A A<9>	TRUE	MEM A CAA<1>	
=MEM A A<6>	TRUE	MEM A CAA<2>	
=MEM A A<8>	TRUE	MEM A CAA<3>	
=MEM A A<7>	TRUE	MEM A CAA<4>	
=MEM A BA<2>	TRUE	MEM A CAA<5>	
MEM A CAA<6>	TRUE	MEM A CAA<6>	
=MEM A A<11>	TRUE	MEM A CAA<7>	
=MEM A A<15>	TRUE	MEM A CAA<8>	
=MEM A A<14>	TRUE	MEM A CAA<9>	
=MEM A A<13>	TRUE	MEM A CAB<0>	
=MEM A CAS L	TRUE	MEM A CAB<1>	
=MEM A WE L	TRUE	MEM A CAB<2>	
=MEM A RAS L	TRUE	MEM A CAB<3>	
=MEM A BA<0>	TRUE	MEM A CAB<4>	
=MEM A A<2>	TRUE	MEM A CAB<5>	
MEM A CAB<6>	TRUE	MEM A CAB<6>	
=MEM A A<10>	TRUE	MEM A CAB<7>	
=MEM A A<1>	TRUE	MEM A CAB<8>	
=MEM A A<0>	TRUE	MEM A CAB<9>	
MEM A ODT<0>	TRUE	MEM A ODT<0>	
TP LPDDR3 RSVD1	TRUE	TP LPDDR3 RSVD1	
TP LPDDR3 RSVD2	TRUE	TP LPDDR3 RSVD2	
=MEM B A<5>	TRUE	MEM B CAA<0>	
=MEM B A<9>	TRUE	MEM B CAA<1>	
=MEM B A<6>	TRUE	MEM B CAA<2>	
=MEM B A<8>	TRUE	MEM B CAA<3>	
=MEM B A<7>	TRUE	MEM B CAA<4>	
=MEM B BA<2>	TRUE	MEM B CAA<5>	
MEM B CAA<6>	TRUE	MEM B CAA<6>	
=MEM B A<11>	TRUE	MEM B CAA<7>	
=MEM B A<15>	TRUE	MEM B CAA<8>	
=MEM B A<14>	TRUE	MEM B CAA<9>	
=MEM B A<13>	TRUE	MEM B CAB<0>	
=MEM B CAS L	TRUE	MEM B CAB<1>	
=MEM B WE L	TRUE	MEM B CAB<2>	
=MEM B RAS L	TRUE	MEM B CAB<3>	
=MEM B BA<0>	TRUE	MEM B CAB<4>	
=MEM B A<2>	TRUE	MEM B CAB<5>	
MEM B CAB<6>	TRUE	MEM B CAB<6>	
=MEM B A<10>	TRUE	MEM B CAB<7>	
=MEM B A<1>	TRUE	MEM B CAB<8>	
=MEM B A<0>	TRUE	MEM B CAB<9>	
MEM B ODT<0>	TRUE	MEM B ODT<0>	
TP LPDDR3 RSVD3	TRUE	TP LPDDR3 RSVD3	
TP LPDDR3 RSVD4	TRUE	TP LPDDR3 RSVD4	

Command/Address	MAKE_BASE	MEM A	MEM B
=MEM A DO<0>	TRUE	MEM A DO<9>	
=MEM A DO<1>	TRUE	MEM A DO<12>	
=MEM A DO<2>	TRUE	MEM A DO<10>	
=MEM A DO<3>	TRUE	MEM A DO<11>	
=MEM A DO<4>	TRUE	MEM A DO<8>	
=MEM A DO<5>	TRUE	MEM A DO<13>	
=MEM A DO<6>	TRUE	MEM A DO<14>	
=MEM A DO<7>	TRUE	MEM A DO<15>	
=MEM A DO<8>	TRUE	MEM A DO<0>	
=MEM A DO<9>	TRUE	MEM A DO<1>	
=MEM A DO<10>	TRUE	MEM A DO<2>	
=MEM A DO<11>	TRUE	MEM A DO<7>	
=MEM A DO<12>	TRUE	MEM A DO<4>	
=MEM A DO<13>	TRUE	MEM A DO<5>	
=MEM A DO<14>	TRUE	MEM A DO<3>	
=MEM A DO<15>	TRUE	MEM A DO<6>	
=MEM A DO<16>	TRUE	MEM A DO<29>	
=MEM A DO<17>	TRUE	MEM A DO<28>	
=MEM A DO<18>	TRUE	MEM A DO<27>	
=MEM A DO<19>	TRUE	MEM A DO<31>	
=MEM A DO<20>	TRUE	MEM A DO<24>	
=MEM A DO<21>	TRUE	MEM A DO<25>	
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=MEM A DO<23>	TRUE	MEM A DO<30>	
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=MEM A DO<36>	TRUE	MEM A DO<40>	
=MEM A DO<37>	TRUE	MEM A DO<45>	
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=MEM A DO<40>	TRUE	MEM A DO<36>	
=MEM A DO<41>	TRUE	MEM A DO<37>	
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=MEM A DO<50>	TRUE	MEM A DO<48>	
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MEM A DOS P<6>	TRUE	MEM A DOS P<6>	
MEM A DOS N<6>	TRUE	MEM A DOS N<6>	
=MEM A DOS P<7>	TRUE	MEM A DOS P<7>	
=MEM A DOS N<7>	TRUE	MEM A DOS N<7>	

Command/Address	MAKE_BASE	MEM B	MEM A
=MEM B DO<0>	TRUE	MEM B DO<12>	
=MEM B DO<1>	TRUE	MEM B DO<9>	
=MEM B DO<2>	TRUE	MEM B DO<10>	
=MEM B DO<3>	TRUE	MEM B DO<11>	
=MEM B DO<4>	TRUE	MEM B DO<13>	
=MEM B DO<5>	TRUE	MEM B DO<8>	
=MEM B DO<6>	TRUE	MEM B DO<14>	
=MEM B DO<7>	TRUE	MEM B DO<15>	
=MEM B DO<8>	TRUE	MEM B DO<0>	
=MEM B DO<9>	TRUE	MEM B DO<1>	
=MEM B DO<10>	TRUE	MEM B DO<2>	
=MEM B DO<11>	TRUE	MEM B DO<7>	
=MEM B DO<12>	TRUE	MEM B DO<4>	
=MEM B DO<13>	TRUE	MEM B DO<5>	
=MEM B DO<14>	TRUE	MEM B DO<6>	
=MEM B DO<15>	TRUE	MEM B DO<3>	
=MEM B DO<16>	TRUE	MEM B DO<28>	
=MEM B DO<17>	TRUE	MEM B DO<29>	
=MEM B DO<18>	TRUE	MEM B DO<30>	
=MEM B DO<19>	TRUE	MEM B DO<27>	
=MEM B DO<20>	TRUE	MEM B DO<24>	
=MEM B DO<21>	TRUE	MEM B DO<25>	
=MEM B DO<22>	TRUE	MEM B DO<31>	
=MEM B DO<23>	TRUE	MEM B DO<26>	
=MEM B DO<24>	TRUE	MEM B DO<20>	
=MEM B DO<25>	TRUE	MEM B DO<16>	
=MEM B DO<26>	TRUE	MEM B DO<23>	
=MEM B DO<27>	TRUE	MEM B DO<22>	
=MEM B DO<28>	TRUE	MEM B DO<21>	
=MEM B DO<29>	TRUE	MEM B DO<17>	
=MEM B DO<30>	TRUE	MEM B DO<18>	
=MEM B DO<31>	TRUE	MEM B DO<19>	
=MEM B DO<32>	TRUE	MEM B DO<44>	
=MEM B DO<33>	TRUE	MEM B DO<41>	
=MEM B DO<34>	TRUE	MEM B DO<42>	
=MEM B DO<35>	TRUE	MEM B DO<43>	
=MEM B DO<36>	TRUE	MEM B DO<45>	
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=MEM B DO<38>	TRUE	MEM B DO<46>	
=MEM B DO<39>	TRUE	MEM B DO<47>	
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MEM B DO<33>	TRUE	MEM B DO<33>	
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=MEM B DO<44>	TRUE	MEM B DO<36>	
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=MEM B DOS N<2>	TRUE	MEM B DOS N<3>	
=MEM B DOS P<3>	TRUE	MEM B DOS P<2>	
=MEM B DOS N<3>	TRUE	MEM B DOS N<2>	
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=MEM B DOS N<4>	TRUE	MEM B DOS N<5>	
=MEM B DOS P<5>	TRUE	MEM B DOS P<4>	
=MEM B DOS N<5>	TRUE	MEM B DOS N<4>	
MEM B DOS P<6>	TRUE	MEM B DOS P<6>	
MEM B DOS N<6>	TRUE	MEM B DOS N<6>	

D

D

C

C

B

B

A

A

SYNC MASTER=J41 MLB SYNC DATE=08/30/2012

Signal Aliases

Apple Inc.

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Functional Test Points

NO_TEST Nets

J3501: AirPort / BT Connector

J6000: Fan Connector

Misc Voltages & Control Signals

Table with columns: FUNC_TEST, PP3V3 WLAN (Need 6 TPs), WIFI EVENT L, PCIE AP R2D N, PCIE AP R2D P, PCIE CLK100M AP N, PCIE CLK100M AP P, PCIE AP D2R P, PCIE AP D2R N, PCIE WAKE L, AP RESET CONN L, AP CLKREQ O L, USB BT CONN P, USB BT CONN N, PP3V3 S4 (Need to add 8 GND TPs)

Table with columns: FUNC_TEST, PP5V S0, FAN RT TACH, FAN RT PWM (Need to add 1 GND TP)

J4800: IPD Flex Connector

Table with columns: FUNC_TEST, SMC L1D, TPAD SPI MISO R, USB TPAD P, USB TPAD N, TPAD SPI CLK R, TPAD WAKE L, TPAD SPI MOSI R, PP3V3 S4 IPD, TPAD SPI CS R L, TPAD SPI IF EN CONN, TPAD SPI INT S4 WAKE L CONN, PP5V S4 IPD, TPAD USB IF EN CONN, SMBUS SMC 3 SDA, SMBUS SMC 3 SCL, SMC LSOC RST L, PP3V42 G3H, SMC ONOFF L (Need to add 5 GND TPs)

J7000: DC-In Connector

Table with columns: FUNC_TEST, PPDICIN G3H (Need 4 TPs), PP5V S4RS3 (Need 3 TPs) (Need to add 5 GND TPs)

J6404: Speaker Connector

Table with columns: FUNC_TEST, SPKRAMP ROUT P, SPKRAMP ROUT N (Need to add 3 GND TPs)

J6950: Battery Connector

Table with columns: FUNC_TEST, PPVBAT G3H CONN (Need 4 TPs), SMBUS SMC 5 G3 SCL, SMBUS SMC 5 G3 SDA, SYS DETECT L (Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

Table with columns: FUNC_TEST, PPHV S0SW LCDBKLT (Need 2 TPs), LED RETURN 6, LED RETURN 5, LED RETURN 4, LED RETURN 3, LED RETURN 2, LED RETURN 1, DP INT HPD CONN, I2C TCON SDA R, I2C TCON SCL R, PP3V3 S0SW LCD UF (Need 2 TPs), DP INT AUX CH C N, DP INT AUX CH C P, DP INT ML P<0>, DP INT ML N<0> (Need to add 5 GND TPs)

J7715: KB BKLT Connector

Table with columns: FUNC_TEST, KBDLED ANODE, KBDLED FB (Need to add 2 GND TPs)

J1800: XDP Connector (Only a subset are needed for FCT HVM test fixture)

Table with columns: FUNC_TEST, XDP CPU TCK, XDP PCH TCK, XDP CPU TDI, XDP CPU TDO, XDP CPU PCH TRST L, XDP CPU TMS, XDP PCH TMS, XDP PCH TDI, XDP PCH TDO, XDP CPU PREQ L, XDP CPU PRDY L, XDP CPU VCCST PWRGD, PM RSMRST L, XDP SYS PWROK, PM SYSRST L, CPU CFG<3>, PP1V05 S0 (Need to add 2 GND TPs)

J3700: SSD Connector

Table with columns: FUNC_TEST, PP3V3 S0SW SSD FLT (Need 5 TPs), PCIE SSD R2D N<3..0>, PCIE SSD R2D P<3..0>, PP3V3 S0, SSD RESET CONN L, SSD CLKREQ CONN L, SMC OOB1 R2D CONN L, SMC OOB1 D2R CONN L, SSD PCIE SEL L, SSD DEVSPLP, SSD PWRFAIL WARN L, SSD PWR EN, PCIE SSD D2R N<3..0>, PCIE SSD D2R P<3..0>, PCIE CLK100M SSD N, PCIE CLK100M SSD P (Need to add 6 GND TPs)

J4002: Camera Connector

Table with columns: FUNC_TEST, MIPI CLK CONN N, MIPI CLK CONN P, CAM SENSOR WAKE L CONN, MIPI DATA CONN N, MIPI DATA CONN P, SMBUS SMC 1 S0 SDA, SMBUS SMC 1 S0 SCL, I2C CAM SCK, I2C CAM SDA, PP5V S3RS0 ALSCAM F (Need 1BD TPs) (Need to add 1BD GND TPs)

J6100: LPC+SPI Connector

Table with columns: FUNC_TEST, PP3V42 G3H, PP5V S0, LPC CLK24M LPCPLUS, LPC AD<3..0>, SPI ALT MOSI, XDP LPCPLUS GPIO, LPCPLUS RESET L, SMC TDO, TP SMC TRST L, TP SMC MD1, SMC TX L, SPI ALT MISO, LPC FRAME L, SPIROM USE MLB, PM CLKRUN L, SPI ALT CLK, SPI ALT CS L, LPC SERIRQ, LPC PWRDWN L, SMC TDI, SMC TCK, SMC RESET L, SMC ROMBOOT, SMC RX L, SMC TMS (Need to add 6 GND TPs)

Unused nets with offpage (Nets with offpages not used on this project)

Table with columns: HDD PWR EN, WOL EN, BT PWRST L, HDMITBTMUX FLAG L, FW PWR EN, ENET MEDIA SENSE, LCD PSR EN, LCD IRO L, ODD PWR EN L, ENET LOW PWR, AUD IP PERIPHERAL DET, AUD I2C INT L, AUD IPHS SWITCH EN

Table with columns: NO_TEST MAKE_BASE, NC PCIE CLK100M SDP, NC PCIE CLK100M SDN, NC PCIE CLK100M FWP, NC PCIE CLK100M FWN, NC PCIE FW D2RP, NC PCIE FW D2RN, NC PCIE FW R2D CP, NC PCIE FW R2D CN, NC USB IRP, NC USB IRN, NC USB CAMERAP, NC USB CAMERAN, NC USB SDP, NC USB SDN, DP INT ML C P<3..1>, DP INT ML C N<3..1>, NC HDA SDIN1, NC PCI PME L, NC CLINK CLK, NC CLINK DATA, NC CLINK RESET L

Table with columns: NC SMC SYS LED, NC IR RX OUT RC, NC USB SMCN, NC SMC GFX OVERTEMP, NC SMC GFX THROTTLE L, NC SMC FAN 1 CTL, NC SMC FAN 1 TACH, NC SMC FAN 5 CTL, NC ENET ASF GPIO, NC SMC MPM5 LED PWR, NC SMC MPM5 LED CHG, NC SMC T25 EN L, NC SMC DP HPD L, NC SMBUS SMC 4 ASF SCL, NC SMBUS SMC 4 ASF SDA, NC BDV BKL PWM

Table with columns: TBT B R2D C P<1..0>, TBT B R2D C N<1..0>, TBT B D2R P<1..0>, TBT B D2R N<1..0>, NC TBT B LSTX, NC DP TBTBP ML CP<3..1:2>, NC DP TBTBP ML CN<3..1:2>, NC DP TBTBP AUXCH CP, NC DP TBTBP AUXCH CN, TP DP TBTSRC ML CP<3>, TP DP TBTSRC ML CN<3>, TP DP TBTSRC ML CP<2>, TP DP TBTSRC ML CN<2>, NC DP TBTSRC ML CP<1>, NC DP TBTSRC ML CN<1>, TP DP TBTSRC ML CP<0>, TP DP TBTSRC ML CN<0>, NC DP TBTSRC AUXCH CP, NC DP TBTSRC AUXCH CN

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Functional Test Points

SD Card Aliases

J9500: LIO Connector		MAKE_BASE	
FUNC_TEST			
TRUE PP3V42 G3H	17 20 25 26 37 38 40 46 49 50	68 65 34 14 USB3 SD D2R P	== TRUE USB3 SD D2R P 14 34 65 68
TRUE PP3V3 S0	8 11 12 13 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 38	68 65 34 14 USB3 SD D2R N	== TRUE USB3 SD D2R N 14 34 65 68
TRUE PP1V5 S0SW AUDIO	58 61	68 65 34 14 USB3 SD R2D C P	== TRUE USB3 SD R2D C P 14 34 65 68
TRUE SYS ONEWIRE	37 61	68 65 34 14 USB3 SD R2D C N	== TRUE USB3 SD R2D C N 14 34 65 68
TRUE SMC BC ACOK	37 38 50 61		
TRUE USB PWR EN	35 59 61	65 39 37 34 15 PP3V3 S0SW SD	== PP3V3 S0SW SD 15 34 37 39 65
TRUE SMBUS SMC 2 S3 SDA	37 40 61 73		(MAKE_BASE=TRUE on page 45)
TRUE SMBUS SMC 2 S3 SCL	37 40 61 73		
TRUE SPKRAMP SHDN L	47 61		
TRUE FINSTACKSNS ALERT L	39 61		
TRUE SPKRAMP INR N	47 61 74		
TRUE SPKRAMP INR P	47 61 74		
TRUE USB EXTB N	14 61 68		
TRUE USB EXTB P	14 61 68		
TRUE PP5V S0 ALT AUD LDO EN	61		
TRUE SMC LID	36 37 38 61 64		
TRUE HDA SDOUT	12 61 69		
TRUE HDA BIT CLK	12 61 69		
TRUE HDA SDINO	12 61 69		
TRUE XDP USB EXTB OC L	14 16 61		
TRUE HDA RST L	12 61 69		
TRUE HDA SYNC	12 61 69		
TRUE USB3 EXTB D2R RC P	61 65 68		
TRUE USB3 EXTB D2R RC N	61 65 68		
TRUE USB3 EXTB R2D P	61 65 68		
TRUE USB3 EXTB R2D N	61 65 68		
TRUE AUD PWR EN	13 59 61		

(Need to add 5 GND TPs)

Bead Probes

68 61 14	USB3 EXTB D2R N	1	BEAD-PROBE	BPA511
68 61 14	USB3 EXTB D2R P	1	BEAD-PROBE	BPA510
68 65 61	USB3 EXTB D2R RC N	1	BEAD-PROBE	BPA520
68 65 61	USB3 EXTB D2R RC P	1	BEAD-PROBE	BPA521
68 61 14	USB3 EXTB R2D C N	1	BEAD-PROBE	BPA513
68 61 14	USB3 EXTB R2D C P	1	BEAD-PROBE	BPA512
68 65 61	USB3 EXTB R2D N	1	BEAD-PROBE	BPA523
68 65 61	USB3 EXTB R2D P	1	BEAD-PROBE	BPA522

SYNC MASTER=J41 MLB		SYNC DATE=09/13/2012	
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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS		BOARD AREAS			BOARD UNITS (MIL. OF MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM		NO_TYPE, BGA, MEM_TERM			MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3, ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIe Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

Note: DisplayPort tables are on Page 113

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
CPU_PECT	CPU_45S	CPU_COMP	CPU_PECT	6 38
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_ITP	XDP_DBRESET L	6 16 17
	CPU_45S	CPU_ITP	XDP_CPU_PRDY L	6 16 64
	CPU_45S	CPU_ITP	XDP_CPU_PREQ L	6 16 64
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
CPU_CATEREER_I	CPU_45S	CPU_ITP	CPU_CFG<11..0>	6 16 64
CPU_CATEREER_I	CPU_45S	CPU_AGTL	CPU_CATEREER_I	6 37
CPU_CATEREER_I	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	6 37 38 51
CPU_CATEREER_I	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6
CPU_CATEREER_I	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THERMTRIP_I	CPU_45S	CPU_SMIL	PM_THERMTRIP_L	15 38
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLKP	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLKN	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M_P	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M_N	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPXDP_CLK100M_P	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPXDP_CLK100M_N	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
XDP_CPU_CLK100M_P	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
XDP_CPU_CLK100M_N	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_CPU_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 64
XDP_CPU_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 64
XDP_CPU_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 64
XDP_CPU_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 64
XDP_CPUPCH_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 13 16 64
XDP_BPM_L<1..0>	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
XDP_BPM_L<7..2>	CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
XDP_OBSDATA_B<3..0>	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	6 16
CPU_CFG<15..12>	CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
XDP_CPURST_L	CPU_45S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE_P	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	6 51
CPU_VCCSENSE_N	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	6 51
CPU_VCCIOSENSE_P	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE_N	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE_P	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE_N	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VDDO_SENSE_P	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P	
CPU_VDDO_SENSE_N	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N	
CPU_AXG_VALSENSE_P	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_AXG_VALSENSE_N	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VCC_VALSENSE_P	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VCC_VALSENSE_N	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_VIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	6 51
CPU_VIDSCCLK	CPU_45S	CPU_COMP	CPU_VIDSCCLK	6 51
CPU_VIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	6 51
PCIE_SSD_R2D_C_P<3..0>	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_SSD_R2D_C_N<3..0>	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
PCIE_SSD_R2D_P<3..0>	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 64
PCIE_SSD_R2D_N<3..0>	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 64
PCIE_SSD_D2R_C_P<3..0>	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	12 30 64
PCIE_SSD_D2R_C_N<3..0>	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	12 30 64
PCIE_SSD_D2R_P<3..0>	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 64
PCIE_SSD_D2R_N<3..0>	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 64
PCIE_CLK100M_SSD_P	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 64
PCIE_CLK100M_SSD_N	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 64
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML N<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML C P<3..0>	5 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML C N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML0 AUXCH P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML0 AUXCH N	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML0 AUXCH C P	13 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML0 AUXCH C N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML1 ML P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML1 ML N<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML1 ML C P<3..0>	5 18 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBT_ML1 ML C N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML1 AUXCH P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML1 AUXCH N	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML1 AUXCH C P	13 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBT_ML1 AUXCH C N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML P<3..0>	60 64
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML N<3..0>	60 64
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML C P<3..0>	6 60 64
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML C N<3..0>	6 60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 60
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 60

PCIe SSD

DP

SYNC MASTER=CONSTRAINTS SYNC DATE=09/25/2012

CPU Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX	USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX	USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX	USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX	USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2RX	USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2TX	USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHER	USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_RX	*	USB3_2OTHER	USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME
	PHYSICAL	SPACING	
PCH_SATA_ICOMP	SATA_ICOMP		PCH_SATAICOMP
USB_HUB1_UP	USB_80D	USB	USB_HUB1_UP_P
USB_HUB1_UP	USB_80D	USB	USB_HUB1_UP_N
USB_BT	USB_80D	USB	USB_BT_P
USB_BT	USB_80D	USB	USB_BT_N
USB_BT	USB_80D	USB	USB_BT_CONN_P
USB_BT	USB_80D	USB	USB_BT_CONN_N
USB_BT	USB_80D	USB	USB_BT_WAKE_P
USB_BT	USB_80D	USB	USB_BT_WAKE_N
USB_TPAD	USB_80D	USB	USB_TPAD_P
USB_TPAD	USB_80D	USB	USB_TPAD_N
USB_TPAD	USB_80D	USB	USB_TPAD_CONN_P
USB_TPAD	USB_80D	USB	USB_TPAD_CONN_N
USB_TPAD_M	USB_80D	USB	TPAD_SPI_MOSI_USB_P
USB_TPAD_M	USB_80D	USB	TPAD_SPI_MISO_USB_N
USB_SDCARD	USB_80D	USB	USB_TPAD_M_P
USB_SDCARD	USB_80D	USB	USB_TPAD_M_N
USB_SDCARD	USB_80D	USB	USB_SDCARD_P
USB_SDCARD	USB_80D	USB	USB_SDCARD_N
SPI_45S	SPI		TPAD_SPI_MOSI
SPI_45S	SPI		TPAD_SPI_MISO
SPI_45S	SPI		TPAD_SPI_CLK
USB_EXT_A	USB_80D	USB	USB_EXT_A_P
USB_EXT_A	USB_80D	USB	USB_EXT_A_N
UART_45S	UART		SMC_DEBUGPRT_TX_L
UART_45S	UART		SMC_DEBUGPRT_RX_L
USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_P
USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_N
USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_F_P
USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_F_N
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_P
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_N
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_P
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_N
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_D2R_F_P
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_D2R_F_N
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_F_P
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_F_N
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_P
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_N
USB_EXT_B	USB_80D	USB	USB_EXT_B_P
USB_EXT_B	USB_80D	USB	USB_EXT_B_N
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_P
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_N
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_RC_P
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_RC_N
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_P
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_N
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_C_P
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_C_N
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_P
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_N
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_P
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_N
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_D2R_C_P
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_D2R_C_N
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N
PCH_USB_RBBIAS	PCH_USB_RBBIAS		PCH_USB_RBBIAS
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCIE_CLK100M_PCH_P
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCIE_CLK100M_PCH_N
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCH_CLK96M_DOT_P
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCH_CLK96M_DOT_N
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCH_CLK100M_SATA_P
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCH_CLK100M_SATA_N
PCH_DIFCLK_UNUSED	CLK_PCFE_80D	CLK_PCFE	PCH_CLK14P3M_REFCLK

USB Hucopyb nets

TP SPI nets

USB EXT_A nets (Right USB port)

USB EXT_B nets (Left USB port)

SYNC_MASTER=CLEAN_J43 SYNC_DATE=11/13/2012

PCH Constraints 1

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DRAWING NUMBER: <SCH_NUM> D
 REVISION: <E4LABEL>
 BRANCH: <BRANCH>
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?	DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?	DP_2OTHERHS	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?	DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	MIN_LENGTH	MAX_LENGTH
	PHYSICAL	SPACING			
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	14	37 46 64
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME L	14	37 46 64
LPC_45S	LPC_45S	LPC	LPCPLUS RESET L	18	46 64
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17	37
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	17	37
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17	46 64
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	17	37
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS PCH CLK	14	16 19 25 40 56
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS PCH DATA	14	16 19 25 40 56
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14	40
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14	40
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	11	32 37 40 43 44 64
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	11	32 37 40 43 44 64
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	12	61 65
HDA_45S	HDA_45S	HDA	HDA BIT CLK R	12	61 65
HDA_SYNC	HDA_45S	HDA	HDA SYNC	12	61 65
HDA_45S	HDA_45S	HDA	HDA SYNC R	12	61 65
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12	61 65
HDA_45S	HDA_45S	HDA	HDA_RST_L	12	61 65
HDA_SDINO	HDA_45S	HDA	HDA_SDINO	12	61 65
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12	61 65
HDA_45S	HDA_45S	HDA	HDA_SDOUT R	12	61 65
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13	38
CLK_SLOW_45S	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	37	38
SPT_CLK	SPT_45S	SPT	SPI_CLK_R	14	46
SPT_45S	SPT_45S	SPT	SPI_CLK	46	46
SPT_45S	SPT_45S	SPT	SPI_MOST_R	14	46
SPT_45S	SPT_45S	SPT	SPI_MOST	46	46
SPT_45S	SPT_45S	SPT	SPI_MISO	14	46
SPT_45S	SPT_45S	SPT	SPI_MISO_R	46	46
SPT_45S	SPT_45S	SPT	SPI_CS0_R_L	14	46
SPT_45S	SPT_45S	SPT	SPI_CS0_L	46	46
SPT_45S	SPT_45S	SPT	SPI_SMC_CLK	37	46
SPT_45S	SPT_45S	SPT	SPI_SMC_MOST	37	46
SPT_45S	SPT_45S	SPT	SPI_SMC_MISO	37	46
SPT_45S	SPT_45S	SPT	SPI_SMC_CS_L	37	46
SPT_45S	SPT_45S	SPT	SPI_MLB_CLK	46	46
SPT_45S	SPT_45S	SPT	SPI_MLB_MOST	46	46
SPT_45S	SPT_45S	SPT	SPI_MLB_MISO	46	46
SPT_45S	SPT_45S	SPT	SPI_MLB_CS_L	46	46
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D P	29	64
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D N	29	64
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C P	14	29
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C N	14	29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R P	14	29 64
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R N	14	29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M AP P	12	29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M AP N	12	29 64
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D P<3..0>	25	25
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D N<3..0>	25	25
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C P<3..0>	14	25
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C N<3..0>	14	25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R P<3..0>	14	25
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R N<3..0>	14	25
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C P<3..0>	25	25
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C N<3..0>	25	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M TBT P	12	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M TBT N	12	25
CLK_PCIE_80D	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M P		
CLK_PCIE_80D	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M N		
XDP_TDI	BCH_45S	BCH_ITP	XDP_PCH_TDI	12	16 64
XDP_TDO	BCH_45S	BCH_ITP	XDP_PCH_TDO	12	16 64
XDP_TMS	BCH_45S	BCH_ITP	XDP_PCH_TMS	12	16 64
XDP_TCK	BCH_45S	BCH_ITP	XDP_PCH_TCK	12	16 64
PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D P	31	32
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D N	31	32
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D C P	14	32
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D C N	14	32
PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R P	14	32
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R N	14	32
PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R C P	31	32
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R C N	31	32
PCIE_CLK100M_CAMERA	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12	32
PCIE_CLK100M_CAMERA	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12	32
CLK_PCIE_80D	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31	32
CLK_PCIE_80D	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31	32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	MIN_LENGTH	MAX_LENGTH
	PHYSICAL	SPACING			
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1		
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17	32
CLK_25M_45S	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31	32
CLK_25M_45S	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32	32
CLK_25M_45S	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32	32
CLK_25M_45S	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32	32
CLK_25M_45S	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31	32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17	25
CLK_25M_45S	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17	17
CLK_25M_45S	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17	17
CLK_25M_45S	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	17	17
CLK_25M_45S	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	14	17
CLK_25M_45S	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	34	34

SYNC MASTER=J41_MLB SYNC DATE=12/14/2012

PCH Constraints 2	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK N<1>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A CS L<1..0>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM A CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM A CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM A CAB<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM A CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM A DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK N<1>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B CS L<1..0>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM B CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM B CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM B CAB<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM B CAB<9..0>
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM B DQ<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS P<7>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS N<7>
		MEM_PWR	PP1V2 S3
		MEM_PWR	PP0V6 S3 MEM VREFCA A
		MEM_PWR	PP0V6 S3 MEM VREFDO A
		MEM_PWR	PP0V6 S3 MEM VREFCA B
		MEM_PWR	PP0V6 S3 MEM VREFDO B

SYNC MASTER=CONSTRAINTS SYNC DATE=09/25/2012

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Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX	TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX	TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX	TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX	TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
TBT_A_R2D	TBTDE_80D	TBTDE_TX	TBT A R2D C P<1..0>
TBT_A_R2D	TBTDE_80D	TBTDE_TX	TBT A R2D C N<1..0>
TBT_A_R2D	TBTDE_80D	TBTDE_TX	TBT A R2D P<1..0>
TBT_A_R2D	TBTDE_80D	TBTDE_TX	TBT A R2D N<1..0>
DP_TBTPA_ML1	DP_80D	DP_TX	DP TBTPA ML C P<1>
DP_TBTPA_ML1	DP_80D	DP_TX	DP TBTPA ML C N<1>
DP_TBTPA_ML3	DP_80D	DP_TX	DP TBTPA ML C P<3>
DP_TBTPA_ML3	DP_80D	DP_TX	DP TBTPA ML C N<3>
	DP_80D	DP_TX	DP TBTPA ML P<3..1:2>
	DP_80D	DP_TX	DP TBTPA ML N<3..1:2>
	DP_80D	DP_TX	DP A LSX ML P<1>
	DP_80D	DP_TX	DP A LSX ML N<1>
	TBTDE_80D	TBTDE_RX	TBT A D2R C P<1..0>
	TBTDE_80D	TBTDE_RX	TBT A D2R C N<1..0>
TBT_A_D2R1	TBTDE_80D	TBTDE_RX	TBT A D2R P<1>
TBT_A_D2R1	TBTDE_80D	TBTDE_RX	TBT A D2R N<1>
TBT_A_D2R0	TBTDE_80D	TBTDE_RX	TBT A D2R P<0>
TBT_A_D2R0	TBTDE_80D	TBTDE_RX	TBT A D2R N<0>
TBT_A_AUXCH	DP_80D	DP_AUX	DP TBTPA AUXCH C P
TBT_A_AUXCH	DP_80D	DP_AUX	DP TBTPA AUXCH C N
	DP_80D	DP_AUX	DP TBTPA AUXCH P
	DP_80D	DP_AUX	DP TBTPA AUXCH N
	DP_80D	DP_AUX	DP A AUXCH DDC P
	DP_80D	DP_AUX	DP A AUXCH DDC N
	TBTDE_80D	TBTDE_RX	TBT A D2R1 AUXDDC P
	TBTDE_80D	TBTDE_RX	TBT A D2R1 AUXDDC N
TBT_B_R2D	TBTDE_80D	TBTDE_TX	TBT B R2D C P<1..0>
TBT_B_R2D	TBTDE_80D	TBTDE_TX	TBT B R2D C N<1..0>
	TBTDE_80D	TBTDE_TX	TBT B R2D P<1..0>
	TBTDE_80D	TBTDE_TX	TBT B R2D N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	NC DP TBTPB ML CP<3..1:2>
DP_TBTPB_ML	DP_80D	DP_TX	NC DP TBTPB ML CN<3..1:2>
	DP_80D	DP_TX	DP TBTPB ML P<3..1:2>
	DP_80D	DP_TX	DP TBTPB ML N<3..1:2>
	DP_80D	DP_TX	DP B LSX ML P<1>
	DP_80D	DP_TX	DP B LSX ML N<1>
	TBTDE_80D	TBTDE_RX	TBT B D2R C P<1..0>
	TBTDE_80D	TBTDE_RX	TBT B D2R C N<1..0>
TBT_B_D2R	TBTDE_80D	TBTDE_RX	TBT B D2R P<1..0>
TBT_B_D2R	TBTDE_80D	TBTDE_RX	TBT B D2R N<1..0>
	DP_80D	DP_AUX	NC DP TBTPB AUXCH CP
	DP_80D	DP_AUX	NC DP TBTPB AUXCH CN
	DP_80D	DP_AUX	DP TBTPB AUXCH P
	DP_80D	DP_AUX	DP TBTPB AUXCH N
	DP_80D	DP_AUX	DP B AUXCH DDC P
	DP_80D	DP_AUX	DP B AUXCH DDC N
	TBTDE_80D	TBTDE_RX	TBT B D2R1 AUXDDC P
	TBTDE_80D	TBTDE_RX	TBT B D2R1 AUXDDC N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	DP_80D	DP_TX	DP TBTSRC ML C P<3..0>
	DP_80D	DP_TX	DP TBTSRC ML C N<3..0>
	DP_80D	DP_AUX	DP TBTSRC AUXCH C P
	DP_80D	DP_AUX	DP TBTSRC AUXCH C N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS L

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=CONSTRAINTS		SYNC DATE=09/25/2012	
Thunderbolt Constraints			
Apple Inc.		DRAWING NUMBER	SIZE
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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?	MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?	MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?	MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2X_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2X_DIELECTRIC	?	S2_DQS2OWNDATA	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CTRL	*	=2X_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CTRL2CTRL	*	=2X_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_2OTHERMEM	*	=4X_DIELECTRIC	?	S2_2OTHERMEM	TOP,BOTTOM	=6X_DIELECTRIC	?
S2MEM_2PWR	*	=2X_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2GND	*	=2X_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2OTHER	*	=6X_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1>
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DO<7..0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DO<15..8>
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN N
		S2_MEM_PWR	PP1V35 CAM
		S2_MEM_PWR	PP0V675 CAM VREF
		S2_MEM_PWR	PP0V675 MEM CAM VREFCA
		S2_MEM_PWR	PP0V675 MEM CAM VREFDO

SYNC MASTER=J41 MLB SYNC DATE=01/30/2013

Camera Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	37 40 60
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	37 40 60
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 64 69
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 64 69
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	37 40 61 65
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	37 40 61 65
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	36 37 40 44 64
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	36 37 40 44 64
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	37 40 48 50 64
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	37 40 48 50 64

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_P	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	50
	2TO1_DIFFPAIR		CHGR_CSI_R_P	50
	2TO1_DIFFPAIR		CHGR_CSI_R_N	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	50
	2TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	2TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

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SMC Constraints			
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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SENSE_1T01_P2MM	*	=1T01_DIFFPAIR	0.200 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR
THERM_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SPKR_DIFFPAIR	*	=1T01_DIFFPAIR	0.300 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 P 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 N 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R P 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R N 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 P 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 N 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS P 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS N 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	MLBBOT THMSNS D3 P 44
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	MLBBOT THMSNS D3 N 44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	TBDTHMSNS D2 P 44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	TBDTHMSNS D2 N 44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THMSNS D2 P 44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THMSNS D2 N 44
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS N 44
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS P 44
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 P 42 52
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 N 42 52
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISNS2 P 42 52
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISNS2 N 42 52
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 P R 42 43
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 N R 42 43
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISUM R P 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISUM R N 42
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS CPUDDR P 42
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS CPUDDR N 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3S5 N 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3S5 P 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3 S0 P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3 S0 N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS CAMERA P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS CAMERA N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3 S0 N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3 S0 P 41
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS 1V05 S0 P 42 55
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS 1V05 S0 N 42 55
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS BMON GAIN P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS BMON GAIN N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING N 41 43
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING P 41 43
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V2 S3 N 41 53
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V2 S3 P 41 53
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS PANEL N 43
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS PANEL P 43
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS GAIN N 43 44
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS GAIN P 43 44
AUD DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR P 47 61 65
AUD DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR N 47 61 65
	1T01_DIFFPAIR	AUDIO	MAX98300 R P 47
	1T01_DIFFPAIR	AUDIO	MAX98300 R N 47
SPKR OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT P 47 64
SPKR OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT N 47 64
	SB_POWER		PP3V3 S5 57 58 59 60 62 64 65 66 68 69 70 71 72 73 74 75 76 77 78
	SB_POWER		PP3V3 S0 59 60 62 64 65 66 68 69 70 71 72 73 74 75 76 77 78
	GND		GND
	GND		GND

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE		

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE			
	PHYSICAL	SPACING		
SDDATA	SD_45SE		SDCONN DATA<0..3>	33 34
SDCLK	SD_45SE		SDCONN CLK	33 34
	SD_45SE		SDCONN WP	33 34
	SD_45SE		SDCONN CMD	33 34
	SD_45SE		SDCONN DETECT L	33 34
	SD_45SE	SPT	SD SPI CLK	34
	SD_45SE	SPT	SD SPI CS L	34
	SD_45SE	SPT	SD SPI MOSI	34
	SD_45SE	SPT	SD SPI MISO	34
CLK_25M_45s			SDCLK CLK 25M X1	
CLK_25M_45s			SDCLK CLK25M X2 R	34 69

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<RDAR://COMPONENT/508937> J43 HW EE SCHEMATIC | PROTO 1
<RDAR://COMPONENT/508941> J43 HW EE SCHEMATIC | EVT
<RDAR://COMPONENT/508945> J43 HW EE SCHEMATIC | DVT

Kismet:

afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

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<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
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<rdar://component/497590> MobileMac HW | Investigation
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