1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2681 MLB-S

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0045286995	ENGINEERING RELEASED	2023-06-27

LAST_MODIFICATION=Tue Jun 27 02:19:00 2023

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114	243	SECDIS: SAK	T585_REF_SECDIS_H14X_0.9.0	
115	245	AUDIO JACK CODEC	T585_REF_CODEC_CARLOW_1.6.0	
116	246	AUDIO AMPLIFIERS (1/2)	T585_REF_SPKRAMP_SN012776_3.8.0	
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-08242	1	SCHEM,MLB-S,X2681	SCH	CRITICAL	SCH
820-02918	1	PCBF,MLB-S,X2681	PCB	CRITICAL	PCB

CHECKPLUS RULE CONFIGURATIONS	
CHECK VOLTAGE IC - LEVELS	?
PCB TESTPOINTS ALLOWED	YES
CHECK FATAL PACK_OPTION	YES
CHECK RESISTOR VOLTAGE	NO

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DRAWING TITLE: SCHEM,MLB-S,X2681

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	SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
SOC_H15C:5,6,8,10,12,14,16,19,20,23,25,27,29,31,33,35,37,39,41-43	T585	REF_SOC_H15S	5,6,8,10,12,14,16,19,20,21,22,23,25,27,29,31,33,35,37,41-42	0.89.0	S	2023_03_29_05:11:19
	T585	REF_SE_JUNO	50	0.1.2	S	2023_02_19_15:59:17
	T585	REF_DEADBATTERY_SAK	51	0.20.9	S	2023_03_21_11:13:53
	T585	REF_CHARGER_MANDOLA_MP	52,53	0.0.12	S	2022_10_24_15:28:45
	T585	REF_MAGSAFE_ACE3	54,55,56	0.4.3	S	2023_04_06_16:03:32
ICEMAN_HP:57,58,60	T585	REF_VR_ICEMAN_HP	57,58,60	0.33.8	S	2022_10_24_15:25:58
CHAPEL:74,76-84,404	T585	REF_PMU_CHAPEL_H15	74,76-84,404	0.42.0	S	2023_04_04_14:26:56
SPITFIRE:93-99	T585	REF_VR_SPITFIRE_EKARA_H15S	93-99	0.28.9	S	2023_04_07_12:52:21
	T585	REF_VR_5V_SN621371	122	0.13.0	S	2022_10_24_15:24:44
	T585	REF_IMU_SOVEREIGN	144	0.16.0	S	2022_10_24_15:24:24
	T585	REF_USBC_VR_LT8642_1	158	0.11.0	S	2022_10_24_15:24:33
	T585	REF_USBC_VR_TPS62180	168	0.9.0	S	2022_10_24_15:24:12
USBC:150-157,159,160,162-164,166-167,169	T585	REF_USBC_LFKA_3PRT_ACE3	150-157,159,160,162-164,166-167,169	0.45.0	S	2023_03_29_05:35:29
HDMI_COBRA:175-179	T585	REF_HDMI_COBRA	175-179	0.61.0	S	2023_03_05_22:15:34
SDCARD_GL9755:195-198	T585	REF_SDCARD_GL9755_V2	195-198	0.13.0	S	2022_10_24_15:26:10
REF_WIRELESS_WILLAMETTE:200-201	T585	REF_WIRELESS_WILLAMETTE	200,201	0.34.0	S	2023_02_28_19:33:16
REF_STORAGE_S5E_MARK2 220-229	T585	REF_STORAGE_S5E_MARK2	220-224	0.26.0	S	2022_10_24_15:24:58
	T585	REF_PANELPWR_2D	237	0.9.0	S	2022_10_24_15:23:49
REF_BLC_LUXE:238	T585	REF_BLC_LUXE	238	0.36.0	S	2022_10_24_15:26:31
	T585	REF_SECDIS_LAS_H14X	242	0.3.0	S	2022_10_24_15:26:52
	T585	REF_SECDIS_H14X	243	0.9.0	S	2022_10_24_15:29:18
	T585	REF_CODEC_CARLOW	245	1.6.0	S	2022_10_24_15:28:11
	T585	REF_SPKRAMP_SN012776	246,247	3.8.0	S	2022_10_24_15:29:29
	T585	REF_BLC_BEN_KBD_ONLY	250	0.8.0	S	2022_10_24_15:29:40
	T585	REF_KBD_34PIN	251	0.7.0	S	2022_10_24_15:26:41
	T585	REF_TPAD_IF_PKG_LARGE	253	0.13.0	H	2023_02_28_18:17:32
	J514.MBESTAWROS	MLB_S	135-140	3.0.3	S	2023_06_06_12:20:54

X2406/X2681 overwrite LIST 04/03/2023

CSA51: REF_DEADBATTERY_SAK
Added Voltage property for PP1V8_AON_DEADBATTERY_R

CSA51: REF_DEADBATTERY_SAK
Added R5179, C5173, U5172, C5172 circuit per rdar://107959550
Change should be in ref design release 0.20.10

CSA52/53: REF_CHARGER_MANDOLA_28V
MUTIPLE BOM related updates

CSA94: REF_VR_SPITFIRE_EKARA_H15S
L9411 APN overwritten (s only) per rdar://103076975
OMIT table for PMU inductors to use 152S01837 as primary rdar://104334933

CSA152: REF_USBC_LFKA_3PRT_ACE3
Added ATC0_ROM_ONLY:YES/NO BOM option for manual override for rdar://105021838 (EVTs: Switch to shared ROM for ATC0 and ATC1)

CSA153: REF_USBC_LFKA_3PRT_ACE3
Remove PPF300 and floating net UPC01_REQUEST_DFU

CSA156: REF_USBC_LFKA_3PRT_ACE3
UP690 overwrite APN 353S4037

CSA250: REF_BLC_BEN_KBD_ONLY
LT000, CT050-CT057 add CRITICAL PROPERTY per rdar://105738392

SYNC_MASTER= SYNC_DATE=05/20/2022

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MAGSAFE BOSS

BS0450
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS0451
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L USBC BOSS

BS04F0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

R USBC BOSS

BS04G0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04G1
2.7X1.8R-1.4ID-1.7H-SM

ANTENNA BOSS

BS04L0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04L1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

DISP, CAM BOSS

BS04P0 860-01924
BOSS-3.2OD1.4D-1.7H-SM

BS04P1 860-01924
BOSS-3.2OD1.4D-1.7H-SM

TRACKPAD BOSS

860-01805
BS04T0
3.4OD1.75ID-2.01H-SM

860-01805
BS04T1
3.4OD1.75ID-2.01H-SM

BKLT BOSS

BS04P2 860-01924
BOSS-3.2OD1.4D-1.7H-SM

BS04P3 860-01924
BOSS-3.2OD1.4D-1.7H-SM

LAS BOSS

BS04R0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04R1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

AUDIO JACK BOSS

BS04R4
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04R5
2.7X1.8R-1.4ID-1.7H-SM
860-01714

TOUCHID BOSS

BS04T2 860-01936
2.7X1.8R-1.34H-SM

BS04T3 860-01936
2.7X1.8R-1.34H-SM

STIFFERNER

APN in BOM TABLE

806-38241
ST0416
STIFFENER-MLB-LOWER-TOP-X2465
SM

806-38241
ST0417
STIFFENER-MLB-LOWER-TOP-X2465
SM

ICEMAN SHIELD FENCE

OMIT_TABLE
SH0478
SM
FENCE-MLB-BTM-NAND-X940

VIPER SHIELD FENCE

OMIT_TABLE
SH0476
SM
FENCE-MLB-BTM-NAND-X940

OMIT_TABLE
SH0477
SM
FENCE-TITAN-RIDGE-X940

TOP-SIDE BUMPERS

860-01819 (was 860-01209) (was 860-01742)

860-01819
BM0400
2.8OD1.2ID-1.703H-SM

BM0402
2.8OD1.2ID-1.703H-SM

BM0403
2.8OD1.2ID-1.703H-SM

BM0404
2.8OD1.2ID-1.703H-SM

BM0405
2.8OD1.2ID-1.703H-SM

BM0406
2.8OD1.2ID-1.703H-SM

BM0407
2.8OD1.2ID-1.703H-SM

BM0408
2.8OD1.2ID-1.703H-SM

BM0410
2.8OD1.2ID-1.703H-SM

BM0413
2.8OD1.2ID-1.703H-SM

BOTTOM-SIDE BUMPERS

was 860-01208
was 860-01741

860-01820
BM0430
2.8OD1.2ID-3.416H-SM

860-01820
BM0434
2.8OD1.2ID-3.416H-SM

860-01820
BM0435
2.8OD1.2ID-3.416H-SM

860-01820
BM0436
2.8OD1.2ID-3.416H-SM

SHIELD FRAMES

OMIT_TABLE
SH0470
SM
FENCE-TITAN-RIDGE-X940

OMIT_TABLE
SH0471
SM
FENCE-MLB-BTM-NAND-X940

OMIT_TABLE
SH0472
SM
FENCE-TITAN-RIDGE-X940

OMIT_TABLE
SH0473
SM
FENCE-MLB-BTM-NAND-X940

OMIT_TABLE
SH0474
SM
FENCE-TITAN-RIDGE-X940

OMIT_TABLE
SH0475
SM
FENCE-MLB-BTM-NAND-X940

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-35724	1	SHIELD,FENCE,BRIDGE,RT,UPDATE,X2465	SH0470	CRITICAL	
806-34681	1	SHIELD,FENCE,BRIDGE,LEFT,X2465	SH0471	CRITICAL	
806-37360	1	SHIELD,FENCE,SPITFIRE,RIGHT,BOT,X2674	SH0472	CRITICAL	
806-37359	1	SHIELD,FENCE,SPITFIRE,LEFT,BOT,X2674	SH0473	CRITICAL	
806-34684	1	SHIELD,FENCE,RIGHT,X2465	SH0474	CRITICAL	
806-34685	1	SHIELD,FENCE,MAVERICK,X2465	SH0475	CRITICAL	
806-37298	1	SHIELD,FENCE,SPITFIRE,LEFT,TOP,S,X2674	SH0476	CRITICAL	
806-37299	1	SHIELD,FENCE,SPITFIRE,RIGHT,TOP,S,X2674	SH0477	CRITICAL	
806-39104	1	SHIELD,FENCE,ICEMAN,X2674	SH0478	CRITICAL	
806-29576	1	STIFFENER,CORNER,LT,UP,MLB,X1930	ST0410	CRITICAL	
806-29575	1	STIFFENER,CORNER,RT,UP,MLB,X1930	ST0411	CRITICAL	
806-29574	1	STIFFENER,LEFT,MID,MLB,,X1930	ST0412	CRITICAL	
806-29573	1	STIFFENER,RT,MID,MLB,X1930	ST0413	CRITICAL	
806-29572	2	STIFFENER,MLB,CORNER,LOWER,X1930	ST0414,ST0415	CRITICAL	
806-37805	1	STFNR,FCS,67SS-167CU-67SS,C,STDOFF,X2294	STFNR	CRITICAL	STFNR
810-20145	1	STIFFENER,MLB,TOP,L5230,X2674	ST0418	CRITICAL	NOSTUFF

ANTENNA CLIPS

860-01841
CL0400
BOSS-2.9X4.7-2.1H-SM

PLATED SLOTS NEAR SOC

Shield CAN Alignment Slots 8X
- 998-04440 (1.2mm X 0.4mm)

SH0445 SH0446 SH0447 SH0448
SH0449 SH0450 SH0451 SH0452
SH0453 SH0454 SH0455 SH0456
SH0457 SH0458 SH0459 SH0460
SH0461 SH0462
TH-NSP
SL-1.2X0.4-1.5X0.7

POGO 870-12170

870-12170
PG0400 PG0401 PG0402 PG0403
PG0404 PG0405 PG0406 PG0407
PG0408 PG0409 PG0410 PG0411
POGO-2.3OD-4.33H-SM
SM

STIFFERNER

806-29576
OMIT_TABLE
ST0410
STIFFENER-MLB-LC-X1930
SM

806-29575
OMIT_TABLE
ST0411
STIFFENER-MLB-LC-X1930
SM

806-29574
OMIT_TABLE
ST0412
STIFFENER-MLB-LC-X1930
SM

806-29573
OMIT_TABLE
ST0413
STIFFENER-MLB-LC-X1930
SM

806-29572
OMIT_TABLE
ST0414
STIFFENER-MLB-LC-X1930
SM

806-29572
OMIT_TABLE
ST0415
STIFFENER-MLB-LC-X1930
SM

806-29573
OMIT_TABLE
ST0418
STIFFENER-MLB-LC-X1930
SM

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=X2481_* SYNC_DATE=09/02/2020

PAGE TITLE
PD PARTS

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 4 OF 700
SHEET 3 OF 156

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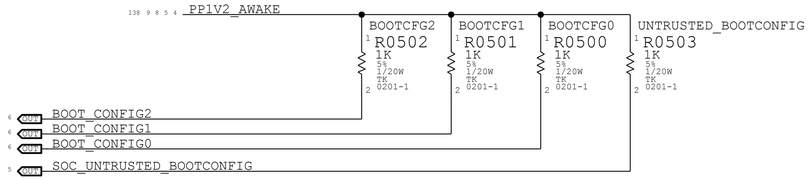
BOOT CONFIG

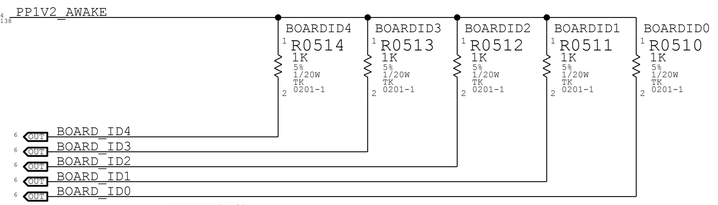


BOOT_CONFIGFG[2:0]	MODE
000	RESERVED
001	RESERVED
010	QUADSPI NOR (24MHZ) BACKUP
011	RESERVED
100	SPI1 NOR (6MHZ) BRING-UP
101	SPI1 NOR (12MHZ) MFG/SIVAL
POR ---> 110	QUADSPI NOR (40MHZ) PROD
111	SPI1 NOR (40MHZ) LEGACY PROD

SW READ FLOW

1. SET GPIO AS INPUT
2. ENABLE IPD
3. WAIT 100 MILLISECONDS
4. READ VALUES
5. DISABLE GPIOS

BOARD ID

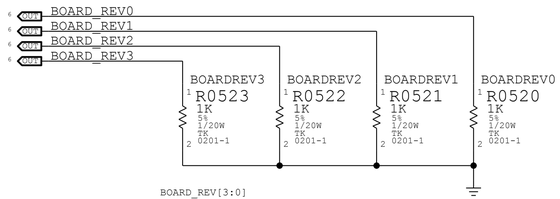


BOARD_ID[4:0]	
00000	Unassigned
00001	Unassigned
00010	Unassigned
00011	Unassigned
00100	X2881
00101	X1711
00110	X2682
00111	X1711
01000	Unassigned
01001	Unassigned
01010	Unassigned
01011	Unassigned
01100	Unassigned
01101	Unassigned
01110	Unassigned
01111	Unassigned

HW READ FLOW

- HARDWARE SAMPLED BEFORE AP TAKEN OUT OF RESET
- SEE CHIPPADS INTEGRATION SPEC, SECTION 2.4.7

BOARD REV



BOARD_REV[3:0]	
0000	0x0
0001	0x1
0010	0x2
0011	0x3
0100	0x4
0101	0x5
0110	0x6
0111	0x7
1000	0x8
1001	0x9
1010	0xA
1011	0xB
1100	0xC
1101	0xD
1110	0xE
1111	0xF

SW READ FLOW

- SAMPLED IN IBOOT ONCE AP IS RUNNING

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: CONFIG STRAPS

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 5 OF 700
SHEET: 4 OF 156

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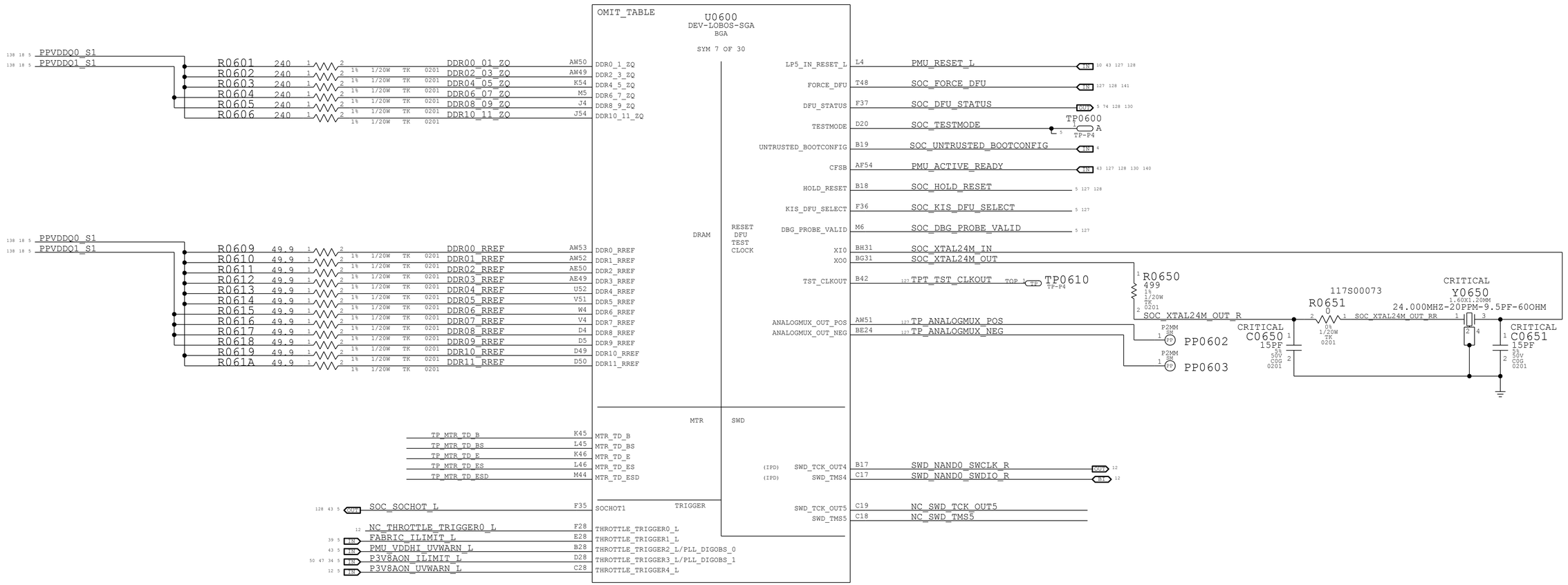

PAGE TITLE
SOC: RESETS, CLOCKS, SWD

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DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 6 OF 700
SHEET 5 OF 156

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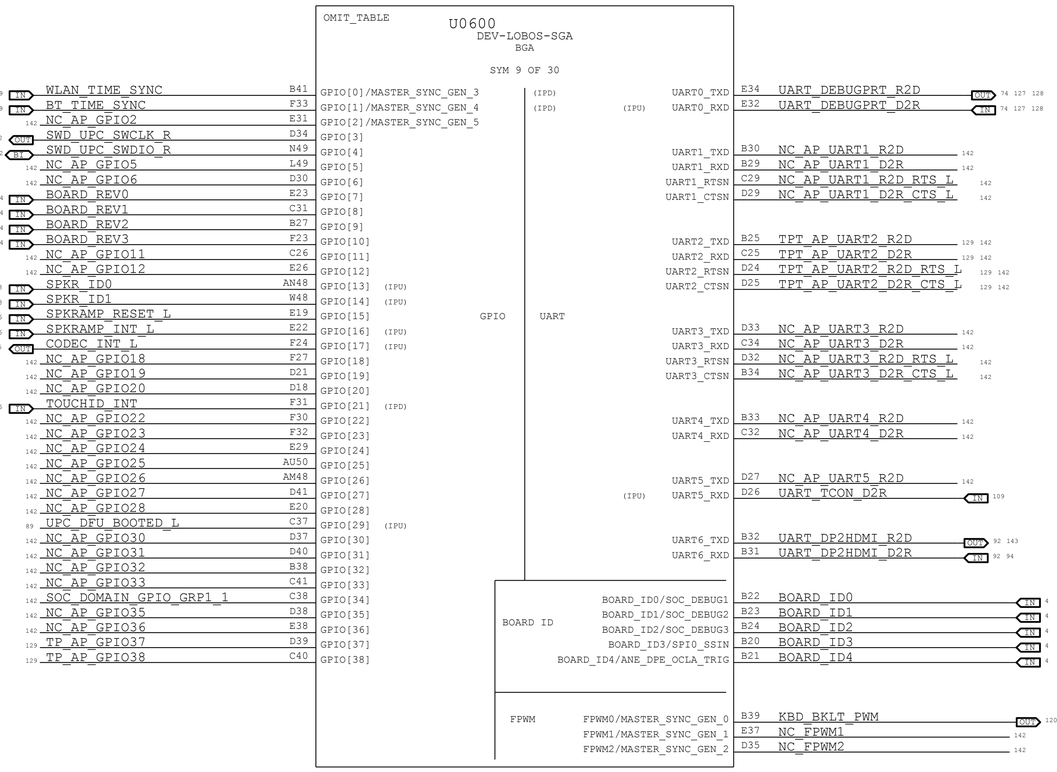

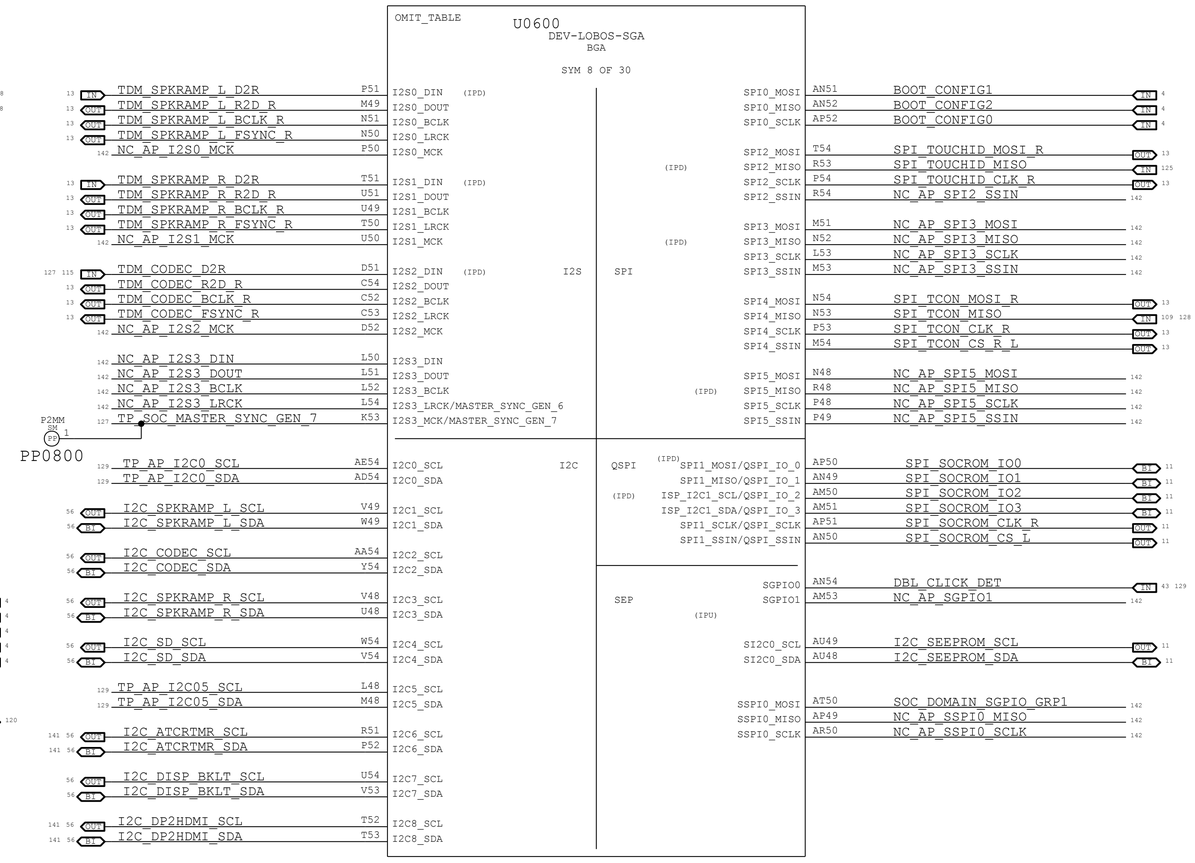

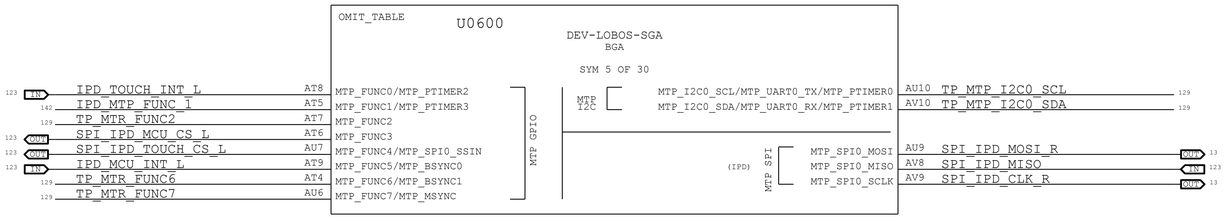

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GPIO, I2C, I2S, SPI, UART

Apple Inc.

DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 8 OF 700
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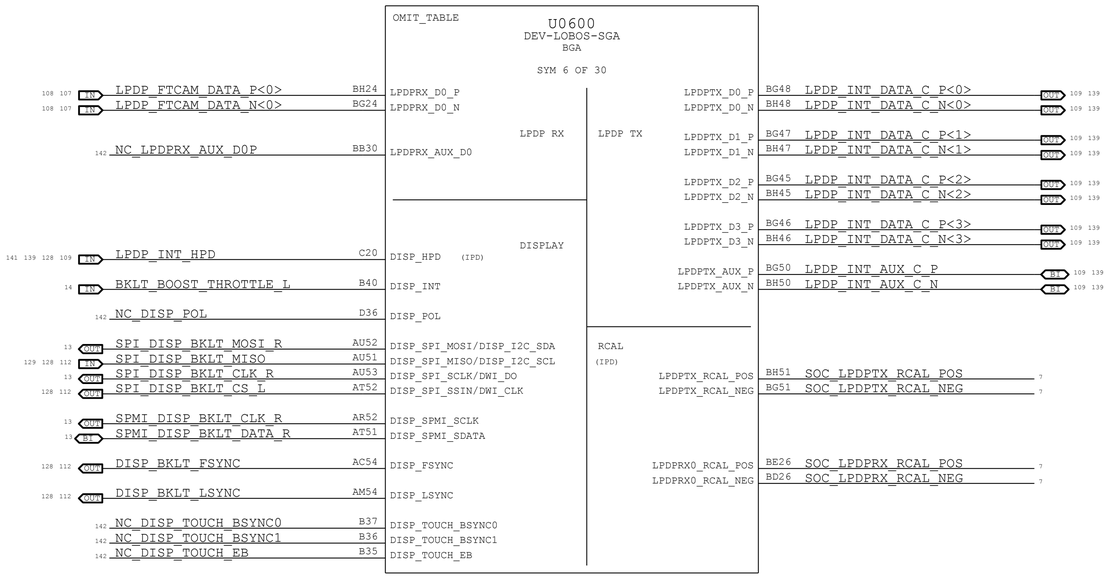

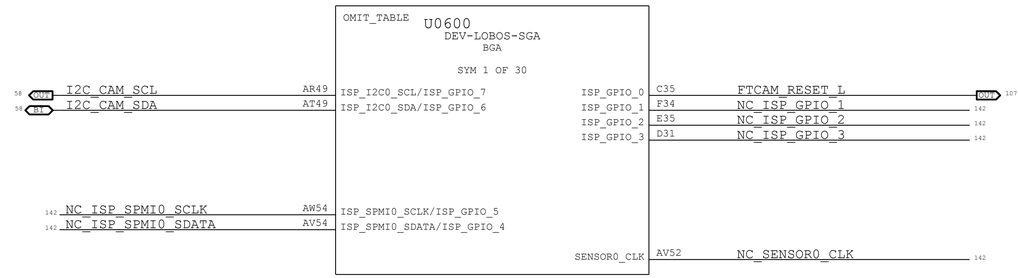

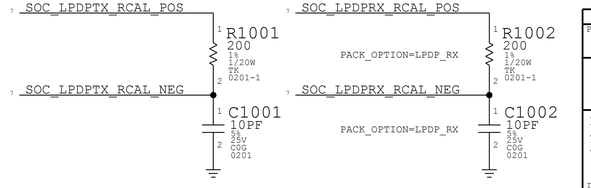

PAGE TITLE
SOC: LPDP, ISP, MIPI

Apple Inc.

DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 10 OF 700
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OMIT_TABLE
U0600
DEV-LOBOS-SGA
BGA
SYM 3 OF 30
PCIE_NAND0_R2D_C_P<0> BD36 ST_PCIE_TX0_P
PCIE_NAND0_R2D_C_N<0> BC36 ST_PCIE_TX0_N
PCIE_NAND0_D2R_P<0> BH36 ST_PCIE_RX0_P
PCIE_NAND0_D2R_N<0> BG36 ST_PCIE_RX0_N
PCIE_CLK100M_NAND0_0_1_P BH29 ST_PCIE_REF_CLK0_P
PCIE_CLK100M_NAND0_0_1_N BG29 ST_PCIE_REF_CLK0_N
NAND0_CLKREQ0_L AP54 ST_PCIE_CLKREQ0_L
ST0 PCIE PORT 0
PCIE_NAND0_R2D_C_P<1> BC35 ST_PCIE_TX1_P
PCIE_NAND0_R2D_C_N<1> BB35 ST_PCIE_TX1_N
PCIE_NAND0_D2R_P<1> BG35 ST_PCIE_RX1_P
PCIE_NAND0_D2R_N<1> BF35 ST_PCIE_RX1_N
NC_PCIE_CLK100M_NAND0_1P BH28 ST_PCIE_REF_CLK1_P
NC_PCIE_CLK100M_NAND0_1N BG28 ST_PCIE_REF_CLK1_N
NAND0_CLKREQ1_L AT53 ST_PCIE_CLKREQ1_L
ST0 PCIE PORT 1
PCIE_NAND0_R2D_C_P<2> BD34 ST_PCIE_TX2_P
PCIE_NAND0_R2D_C_N<2> BC34 ST_PCIE_TX2_N
PCIE_NAND0_D2R_P<2> BH34 ST_PCIE_RX2_P
PCIE_NAND0_D2R_N<2> BG34 ST_PCIE_RX2_N
PCIE_CLK100M_NAND0_2_3_P BH27 ST_PCIE_REF_CLK2_P
PCIE_CLK100M_NAND0_2_3_N BG27 ST_PCIE_REF_CLK2_N
NAND0_CLKREQ2_L AT54 ST_PCIE_CLKREQ2_L
ST0 PCIE PORT 2
PCIE_NAND0_R2D_C_P<3> BC33 ST_PCIE_TX3_P
PCIE_NAND0_R2D_C_N<3> BB33 ST_PCIE_TX3_N
PCIE_NAND0_D2R_P<3> BG33 ST_PCIE_RX3_P
PCIE_NAND0_D2R_N<3> BF33 ST_PCIE_RX3_N
NC_PCIE_CLK100M_NAND0_3P BH26 ST_PCIE_REF_CLK3_P
NC_PCIE_CLK100M_NAND0_3N BG26 ST_PCIE_REF_CLK3_N
NAND0_CLKREQ3_L AU54 ST_PCIE_CLKREQ3_L
ST0 PCIE PORT 3
NAND0_PCIE_RESET_L AP53 ST_PCIE_PERST_L
SOC_ST0_PCIE_RCAL_POS BH42 ST_PCIE_RCAL_POS
SOC_ST0_PCIE_RCAL_NEG BG42 ST_PCIE_RCAL_NEG
RCAL
NAND_SYS_CLK0 AL48 NAND0_CLK24M_R
NAND_SYS_CLK1 AL49 NC_NAND1_CLK24M_R
SSD_BFH AL54 NAND_BFH
SSD_RESET0_L AR54 SOC_DOMAIN_HGPIO_GRP0_0
SSD_RESET1_L AN53 SOC_DOMAIN_HGPIO_GRP0_1
NAND SUPPORT
OMIT_TABLE
U0600
DEV-LOBOS-SGA
BGA
SYM 2 OF 30
PCIE_WLBT_R2D_C_P BD40 GP_PCIE_TX0_P
PCIE_WLBT_R2D_C_N BC40 GP_PCIE_TX0_N
PCIE_WLBT_D2R_P BH40 GP_PCIE_RX0_P
PCIE_WLBT_D2R_N BG40 GP_PCIE_RX0_N
PCIE_CLK100M_WLBT_P BE31 GP_PCIE_REF_CLK0_P
PCIE_CLK100M_WLBT_N BD31 GP_PCIE_REF_CLK0_N
WLBT_CLKREQ_L F26 GP_PCIE_CLKREQ0_L
WLBT_RESET_L D23 GP_PCIE_PERST0_L
GP PCIE PORT 0
PCIE_SD_UHS2_R2D_C_P BC39 GP_PCIE_TX1_P
PCIE_SD_UHS2_R2D_C_N BB39 GP_PCIE_TX1_N
PCIE_SD_UHS2_D2R_P BG39 GP_PCIE_RX1_P
PCIE_SD_UHS2_D2R_N BF39 GP_PCIE_RX1_N
PCIE_CLK100M_SD_UHS2_P BE30 GP_PCIE_REF_CLK1_P
PCIE_CLK100M_SD_UHS2_N BD30 GP_PCIE_REF_CLK1_N
SD_UHS2_CLKREQ_L B26 GP_PCIE_CLKREQ1_L
SD_UHS2_RESET_L C22 GP_PCIE_PERST1_L
GP PCIE PORT 1
SOC_GP_PCIE_RCAL_POS BH43 GP_PCIE_RCAL_POS
SOC_GP_PCIE_RCAL_NEG BG43 GP_PCIE_RCAL_NEG
GP RCAL
GP_PCIE_TX2_P BD38 NC_GP_PCIE_TX2_P
GP_PCIE_TX2_N BC38 NC_GP_PCIE_TX2_N
GP_PCIE_RX2_P BH38 NC_GP_PCIE_RX2_P
GP_PCIE_RX2_N BG38 NC_GP_PCIE_RX2_N
GP_PCIE_REF_CLK2_P BE29 NC_GP_PCIE_REF_CLK2_P
GP_PCIE_REF_CLK2_N BD29 NC_GP_PCIE_REF_CLK2_N
GP_PCIE_CLKREQ2_L C23 NC_GP_PCIE_CLKREQ2_L
GP_PCIE_PERST2_L D22 NC_GP_PCIE_PERST2_L
GP PCIE PORT 2
GP_PCIE_TX3_P BC37 NC_GP_PCIE_TX3_P
GP_PCIE_TX3_N BB37 NC_GP_PCIE_TX3_N
GP_PCIE_RX3_P BG37 NC_GP_PCIE_RX3_P
GP_PCIE_RX3_N BF37 NC_GP_PCIE_RX3_N
GP_PCIE_REF_CLK3_P BE28 NC_GP_PCIE_REF_CLK3_P
GP_PCIE_REF_CLK3_N BD28 NC_GP_PCIE_REF_CLK3_N
GP_PCIE_CLKREQ3_L F25 NC_GP_PCIE_CLKREQ3_L
GP_PCIE_PERST3_L E25 NC_GP_PCIE_PERST3_L
GP PCIE PORT 3
PP1V2_AWAKE
R1210 30K NAND0_CLKREQ0_L
R1211 30K NAND0_CLKREQ1_L
R1212 30K NAND0_CLKREQ2_L
R1213 30K NAND0_CLKREQ3_L
1% 1/20W TK 0201
R1218 30K WLBT_CLKREQ_L
R1219 30K SD_UHS2_CLKREQ_L
PACK_OPTION=SDCARD
R1222 47K NAND0_PCIE_RESET_L
R1224 47K WLBT_RESET_L
R1225 47K SD_UHS2_RESET_L
5% 1/20W TK 0201
PACK_OPTION=SDCARD
SOC_ST0_PCIE_RCAL_POS
SOC_ST0_PCIE_RCAL_NEG
R1200 200 1% 1/20W TK 0201-1
C1200 10PF ±5% 25V C0G 0201
SOC_GP_PCIE_RCAL_POS
SOC_GP_PCIE_RCAL_NEG
R1202 200 1% 1/20W TK 0201-1
C1202 10PF ±5% 25V C0G 0201
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: PCIE
Apple Inc.
DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 12 OF 700
SHEET 8 OF 156
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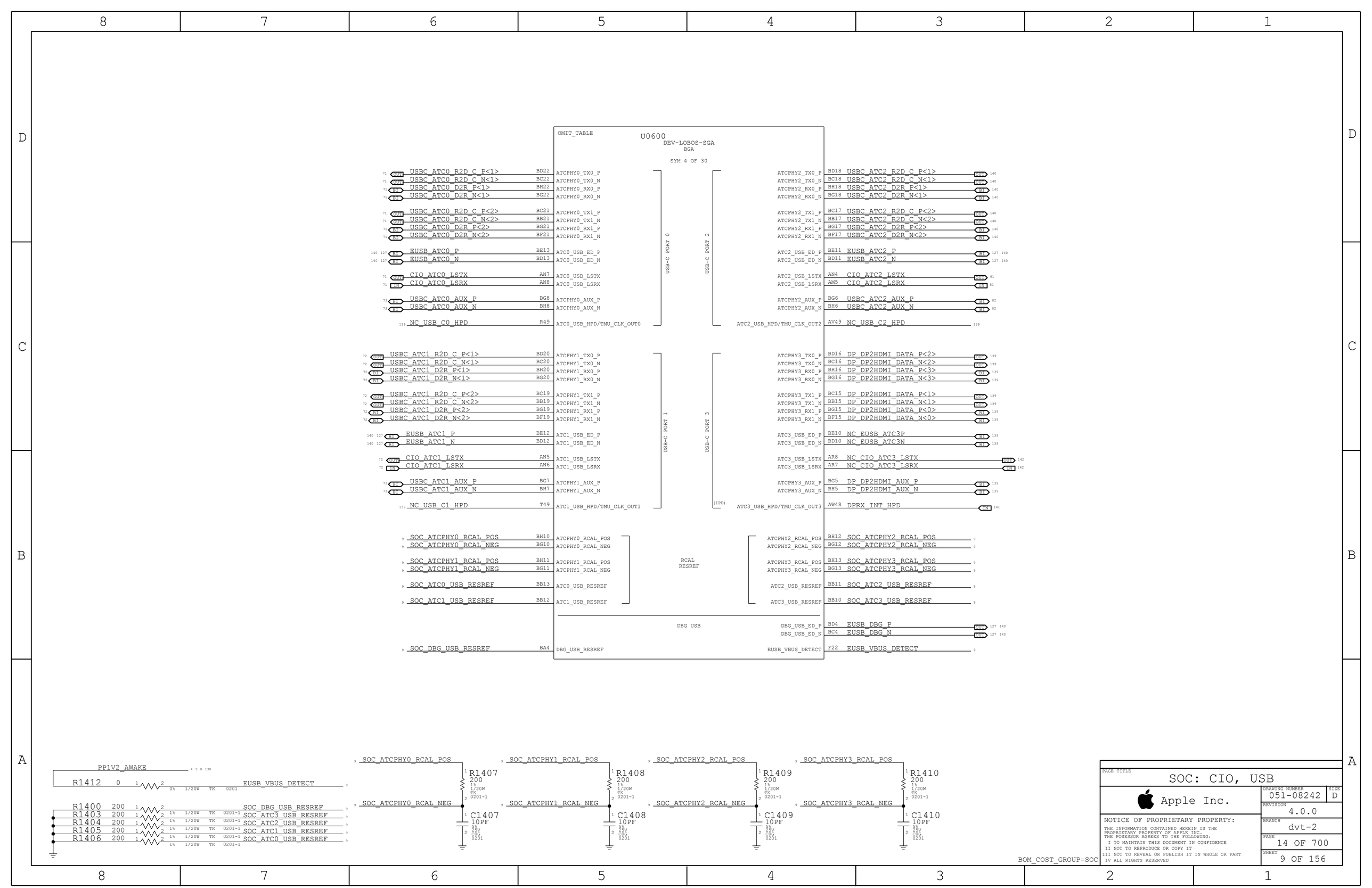

PAGE TITLE: SOC: CIO, USB

Apple Inc.

DRAWING NUMBER: 051-08242 | SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 14 OF 700
SHEET: 9 OF 156

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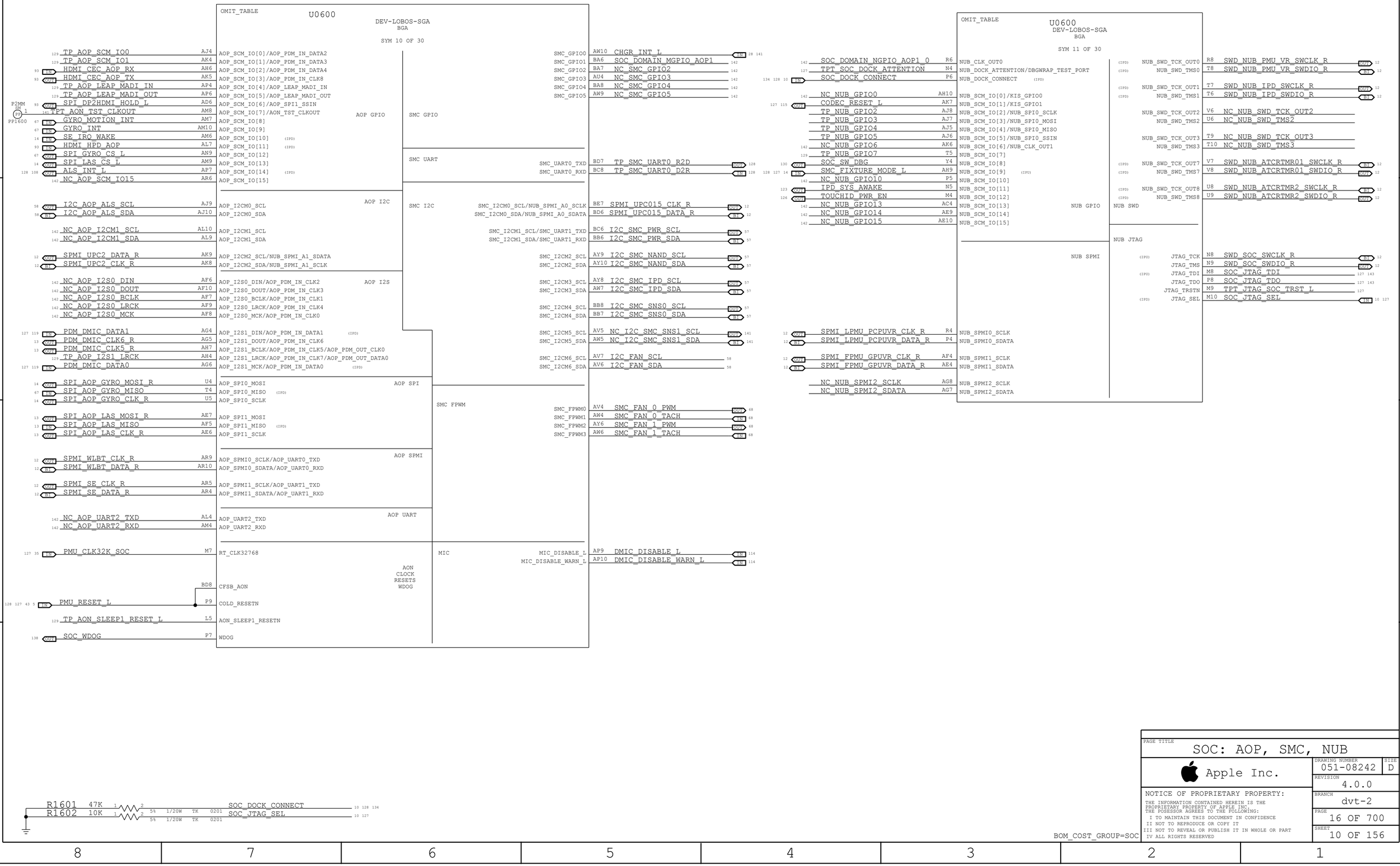

PAGE TITLE: SOC: AOP, SMC, NUB

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 16 OF 700
SHEET: 10 OF 156

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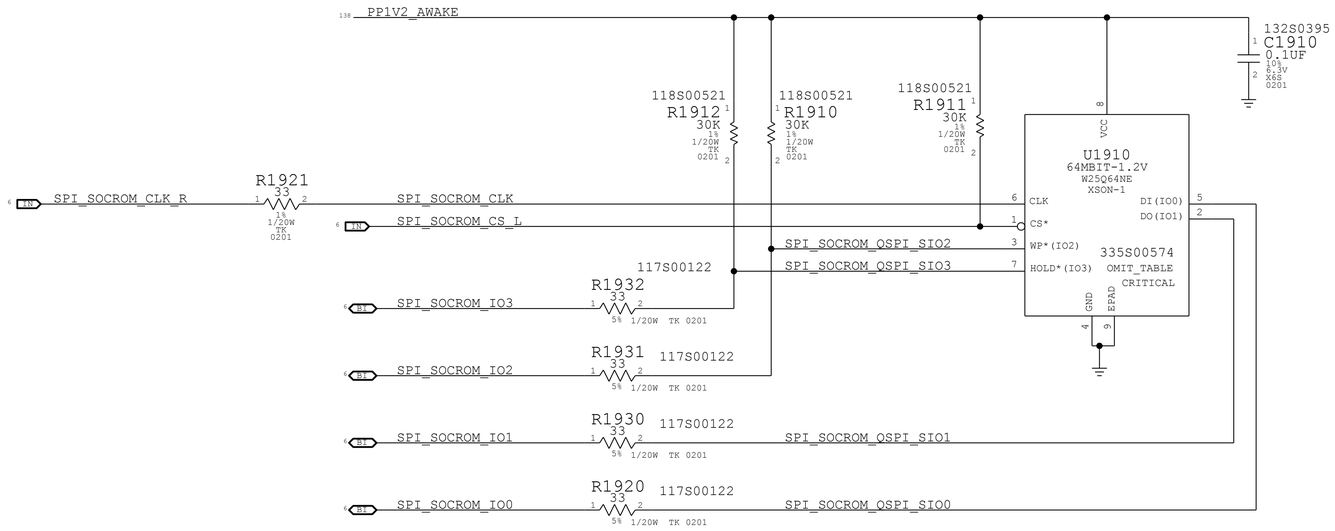
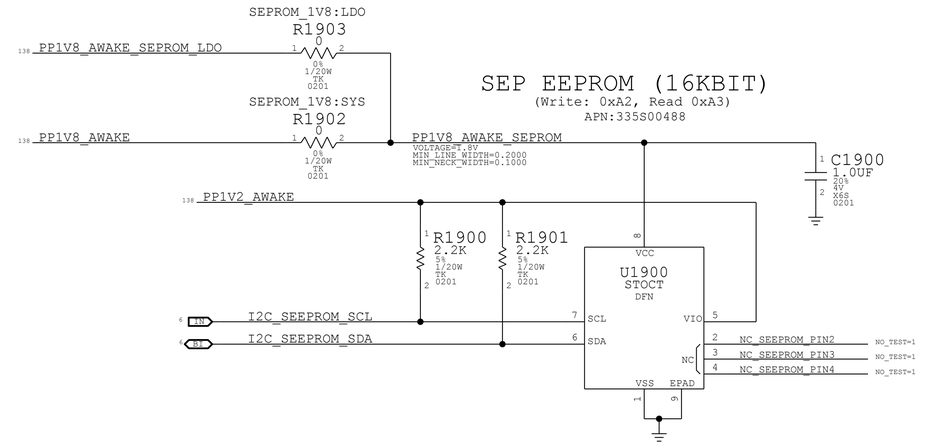
SPI NOR (1.2V 64MBIT)



SEP EEPROM (16KBIT)

(Write: 0xA2, Read 0xA3)

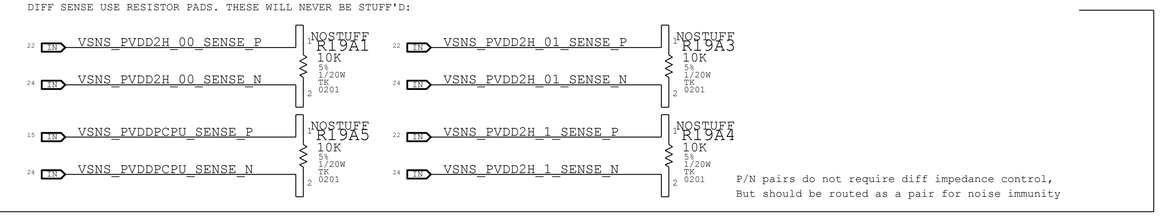
APN:335S00488

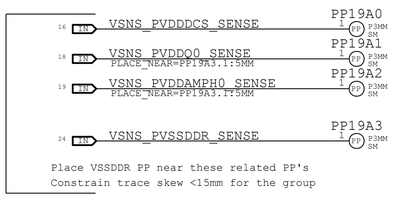


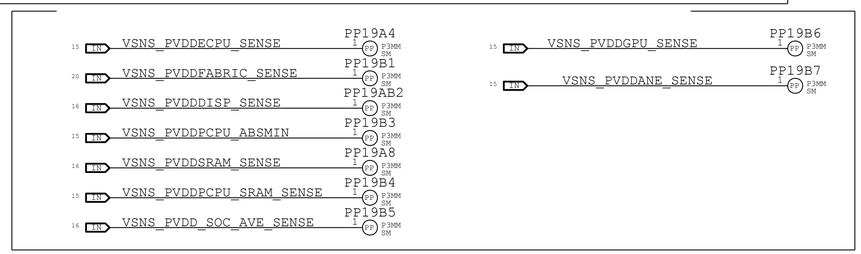
VDD/VSS SENSE BREAKOUT PADS

All SOC/DRAM VSNS traces to attempt to be 50ohm SE-impedance
45ohm SE-impedance will work but may impact measurement accuracy

DIFF SENSE USE RESISTOR PADS. THESE WILL NEVER BE STUFF'D:







BOM_COST_GROUP=SOC

PAGE TITLE: SOC: QSPI ROM, SEP ROM, VSNS

Apple Inc.

DRAWING NUMBER: 051-08242 | SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

PAGE: 19 OF 700

SHEET: 11 OF 156

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SPMI SERIES TERMINATION

IN	SPMI_LPMU_PCPUVR_CLK_R	R2008	20	SPMI_LPMU_PCPUVR_CLK	R2021	49.9	SPMI_LPMU_CLK	OUT	43
					R2022	49.9	SPMI_PCPUVR_CLK	OUT	47
BI	SPMI_LPMU_PCPUVR_DATA_R	R2009	20	SPMI_LPMU_PCPUVR_DATA	R2023	49.9	SPMI_LPMU_DATA	BI	43
					R2024	49.9	SPMI_PCPUVR_DATA	BI	47
IN	SPMI_FPMU_GPUVR_CLK_R	R2014	20	SPMI_FPMU_GPUVR_CLK	R2010	49.9	SPMI_FPMU_CLK	OUT	39
					R2011	49.9	SPMI_GPUVR_CLK	OUT	50
BI	SPMI_FPMU_GPUVR_DATA_R	R2015	20	SPMI_FPMU_GPUVR_DATA	R2012	49.9	SPMI_FPMU_DATA	BI	39
					R2013	49.9	SPMI_GPUVR_DATA	BI	50
IN	SPMI_WLBT_CLK_R				R2068	20	SPMI_WLBT_CLK	OUT	99
BI	SPMI_WLBT_DATA_R				R2069	20	SPMI_WLBT_DATA	BI	99
IN	SPMI_SE_CLK_R				R2000	20	SPMI_SE_CLK	BI	25
BI	SPMI_SE_DATA_R				R2001	20	SPMI_SE_DATA	OUT	25
IN	SPMI_UPC015_CLK_R	R2070	20	SPMI_UPC015_CLK	R2071	33	SPMI_UPC0_CLK	OUT	89
					R2072	33	SPMI_UPC1_CLK	OUT	89
					R2073	33	SPMI_UPC5_CLK	OUT	89
BI	SPMI_UPC015_DATA_R	R2074	20	SPMI_UPC015_DATA	R2075	33	SPMI_UPC0_DATA	BI	89
					R2076	33	SPMI_UPC1_DATA	BI	89
					R2077	33	SPMI_UPC5_DATA	BI	89
IN	SPMI_UPC2_CLK_R	R2078	20	SPMI_UPC2_CLK_R2			SPMI_UPC2_CLK	OUT	89
					R2016	20			
BI	SPMI_UPC2_DATA_R	R2079	20	SPMI_UPC2_DATA_R2			SPMI_UPC2_DATA	BI	89
					R2017	20			

SWD SERIES TERMINATION

IN	SWD_NAND0_SWCLK_R	R2032	15	SWD_NAND0_SWCLK	R2082	49.9	SWD_NAND0_S5E0_S5E1_SWCLK	OUT	139
					R2083	49.9	SWD_NAND0_S5E2_S5E3_SWCLK	OUT	139
BI	SWD_NAND0_SWDIO_R	R2033	15	SWD_NAND0_SWDIO	R2084	49.9	SWD_NAND0_S5E0_S5E1_SWDIO	BI	139
					R2085	49.9	SWD_NAND0_S5E2_S5E3_SWDIO	BI	139
IN	SWD_NUB_PMU_VR_SWCLK_R	R2036	15	SWD_NUB_PMU_VR_SWCLK	R2040	49.9	SWD_LPMU_SWCLK	OUT	43
					R2042	49.9	SWD_FPMU_SWCLK	OUT	39
					R2030	49.9	SWD_PCPUVR_SWCLK	OUT	47
					R2090	49.9	SWD_GPUVR_SWCLK	OUT	50
BI	SWD_NUB_PMU_VR_SWDIO_R	R2037	15	SWD_NUB_PMU_VR_SWDIO	R2041	49.9	SWD_LPMU_SWDIO	BI	43
					R2043	49.9	SWD_FPMU_SWDIO	BI	39
					R2031	49.9	SWD_PCPUVR_SWDIO	BI	47
					R2092	49.9	SWD_GPUVR_SWDIO	BI	50
OUT	SWD_NUB_IPD_SWCLK_R				R2065	49.9	SWD_NUB_IPD_SWCLK	BI	140
BI	SWD_NUB_IPD_SWDIO_R				R2066	49.9	SWD_NUB_IPD_SWDIO	BI	140
OUT	SWD_NUB_ATCRTMR01_SWCLK_R				R2061	49.9	SWD_NUB_ATCRTMR01_SWCLK	BI	141
BI	SWD_NUB_ATCRTMR01_SWDIO_R				R2062	49.9	SWD_NUB_ATCRTMR01_SWDIO	BI	141
OUT	SWD_NUB_ATCRTMR2_SWCLK_R				R2063	49.9	SWD_NUB_ATCRTMR2_SWCLK	BI	141
BI	SWD_NUB_ATCRTMR2_SWDIO_R				R2064	49.9	SWD_NUB_ATCRTMR2_SWDIO	BI	141
OUT	SWD_SOC_SWCLK_R				R2038	0	SWD_SOC_SWCLK	IN	74 127 128
BI	SWD_SOC_SWDIO_R				R2039	0	SWD_SOC_SWDIO	BI	74 127 128

IN	SWD_UPC_SWCLK_R	R2050	20	SWD_UPC_SWCLK	R2046	49.9	SWD_UPC_SWCLK015	R2051	20	SWD_UPC_SWCLK0	MAKE_BASE=TRUE	SWD_UPC_SWCLK0	OUT	75 140
								R2052	20	SWD_UPC_SWCLK1	MAKE_BASE=TRUE	SWD_UPC_SWCLK1	OUT	76
								R2053	49.9	SWD_UPC_SWCLK5	MAKE_BASE=TRUE	SWD_UPC_SWCLK5	OUT	30 31
					R2060	20	SWD_UPC_SWCLK2				MAKE_BASE=TRUE	SWD_UPC_SWCLK2	OUT	84 140
BI	SWD_UPC_SWDIO_R	R2054	20	SWD_UPC_SWDIO	R2055	49.9	SWD_UPC_SWDIO015	R2047	20	SWD_UPC_SWDIO0	MAKE_BASE=TRUE	SWD_UPC_SWDIO0	BI	75 140
								R2049	20	SWD_UPC_SWDIO1	MAKE_BASE=TRUE	SWD_UPC_SWDIO1	BI	76
								R2056	49.9	SWD_UPC_SWDIO5	MAKE_BASE=TRUE	SWD_UPC_SWDIO5	BI	30 31
					R2048	20	SWD_UPC_SWDIO2				MAKE_BASE=TRUE	SWD_UPC_SWDIO2	BI	84 140

OUT	P3V8AON_UVWARN_L	R2026	430	PMU_VDDMAIN_UVWARN_L	IN	43
		R2027	0	PCPUVR_VDDMAIN_UVWARN_L	IN	47
		R2028	680	GPUVR_VDDMAIN_UVWARN_L	IN	50

NC_THROTTLE_TRIGGER0_L = NC_THROTTLE_TRIGGER0_L (MAKE_BASE=TRUE)

NAND PCIE CLK BRANCH RESISTORS

IN	PCIE_CLK100M_NAND0_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_1_P	OUT 101 106
			PCIE_CLK100M_NAND0_0_1_P	OUT 102
IN	PCIE_CLK100M_NAND0_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_1_N	OUT 101 106
			PCIE_CLK100M_NAND0_0_1_N	OUT 102
IN	PCIE_CLK100M_NAND0_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_3_P	OUT 103 106
			PCIE_CLK100M_NAND0_2_3_P	OUT 104
IN	PCIE_CLK100M_NAND0_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_3_N	OUT 103 106
			PCIE_CLK100M_NAND0_2_3_N	OUT 104

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: SHARED SUPPORT 1

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

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SHEET: 12 OF 156

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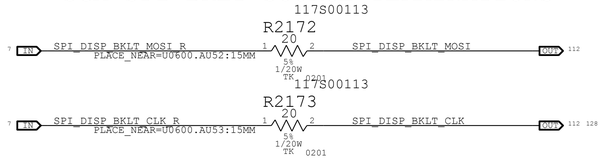
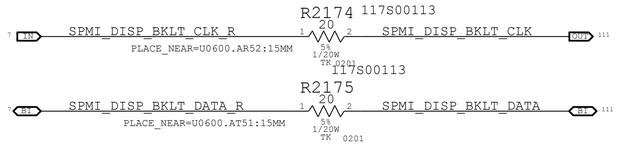
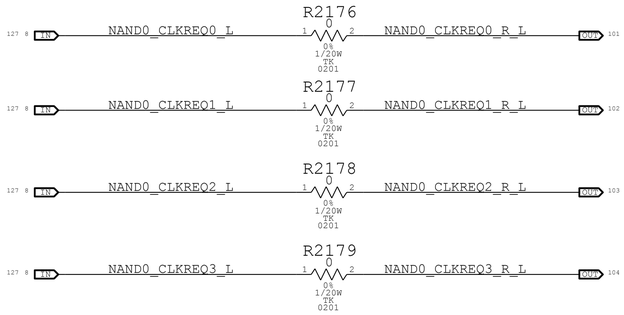
SGA SPI BKLT SOURCE TERMINATIONS



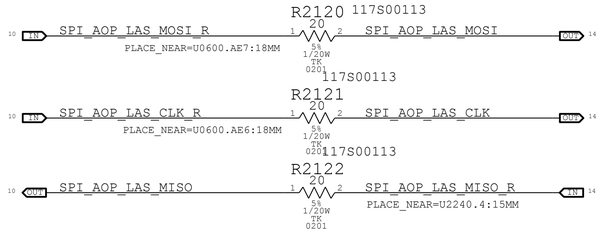
LUXE SPMI SOURCE TERMINATIONS



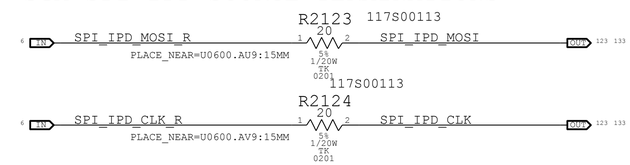
NAND CLKREQ SERIES RESISTORS



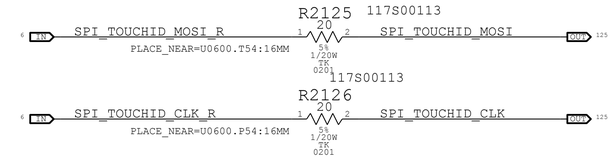
SGA SPI SENSOR SOURCE TERMINATIONS



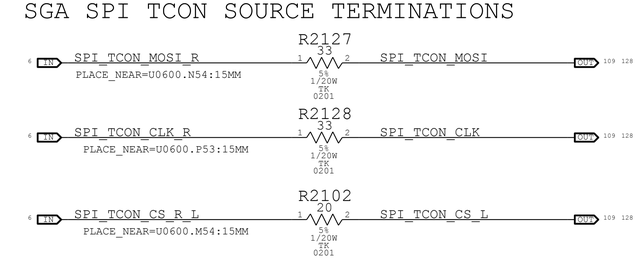
SGA SPI IPD SOURCE TERMINATIONS



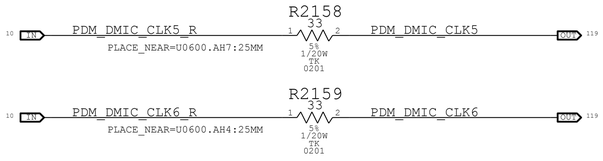
SGA SPI TOUCHID SOURCE TERMINATIONS



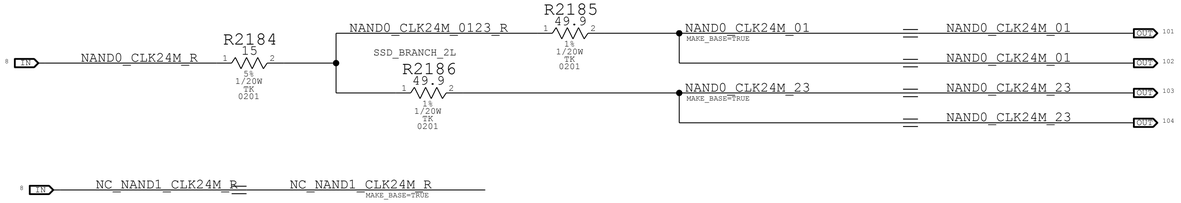
SGA SPI TCON SOURCE TERMINATIONS



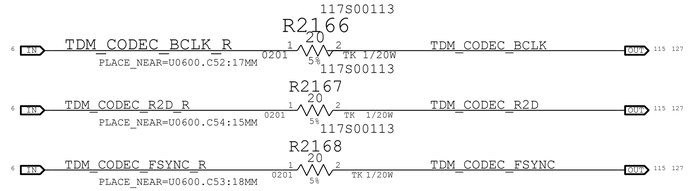
DMIC CLK SOURCE TERMINATIONS



SSD 24M CLOCK TERMINATIONS



SGA TDM SOURCE TERMINATIONS



BOM_COST_GROUP=SOC

PAGE TITLE: SOC: SHARED SUPPORT 2

Apple Inc.

DRAWING NUMBER: 051-08242 | SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 21 OF 700
SHEET: 13 OF 156

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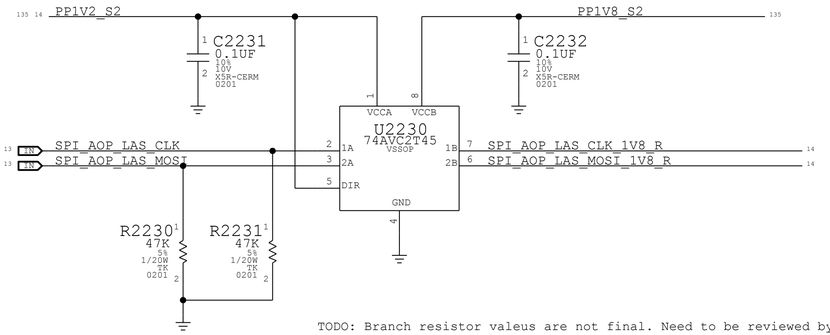
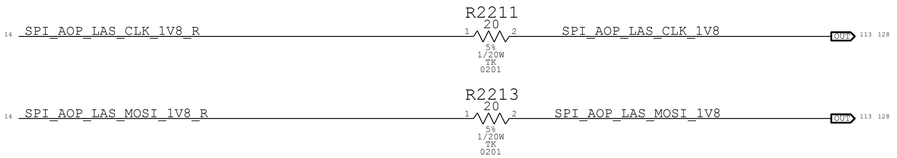
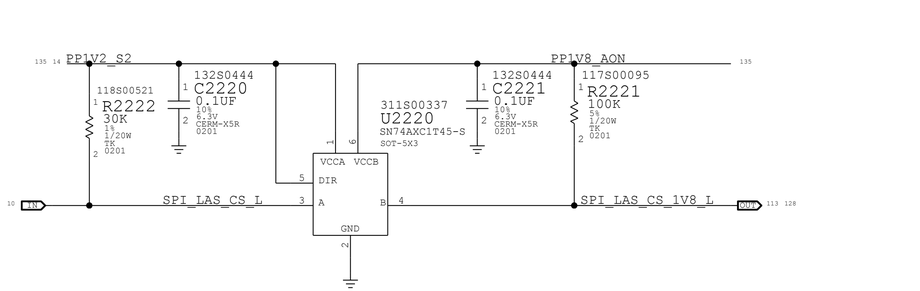
SPI AOP Sensor LS and Branch Resistors

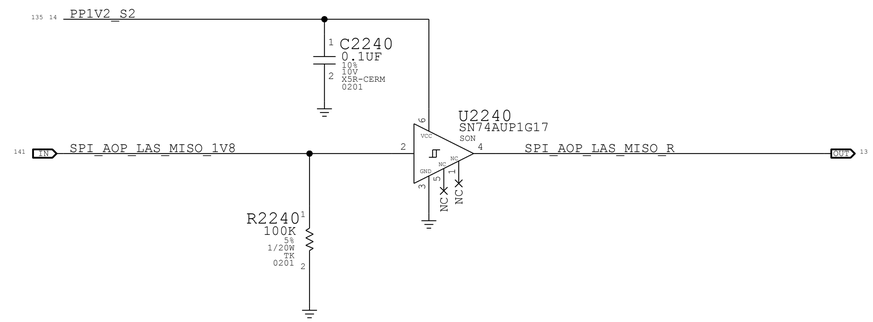


TODO: Branch resistor valeus are not final. Need to be reviewed by SI once routed

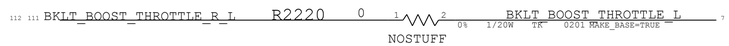




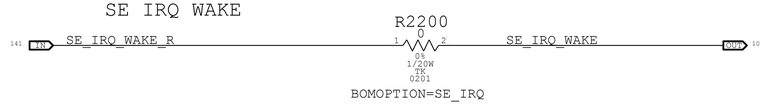
SPI LEVEL TRANSLATION

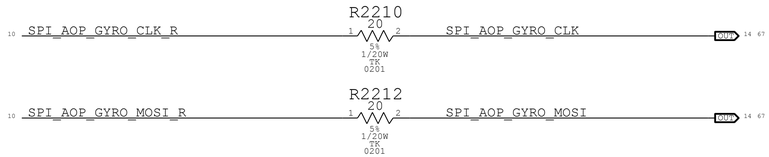


DISPLAY BACKLIGHT



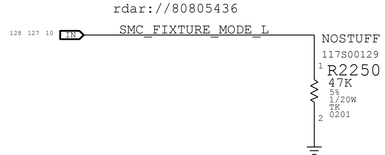
SE IRQ WAKE





rdar://86287477

rdar://80805436



BOM_COST_GROUP=SOC

PAGE TITLE
PROJECT SUPPORT (2/2)

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DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 22 OF 700
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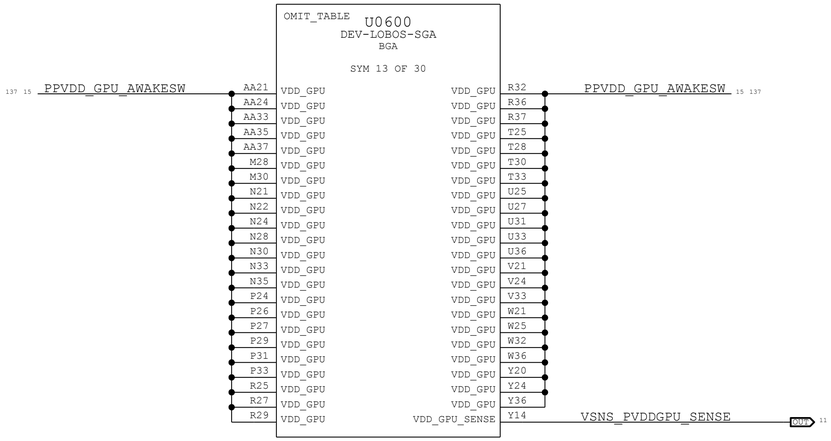

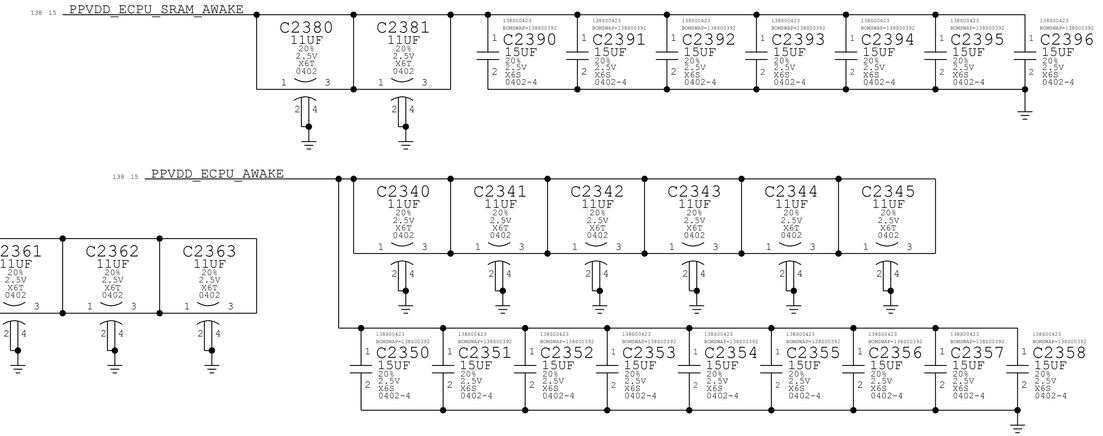

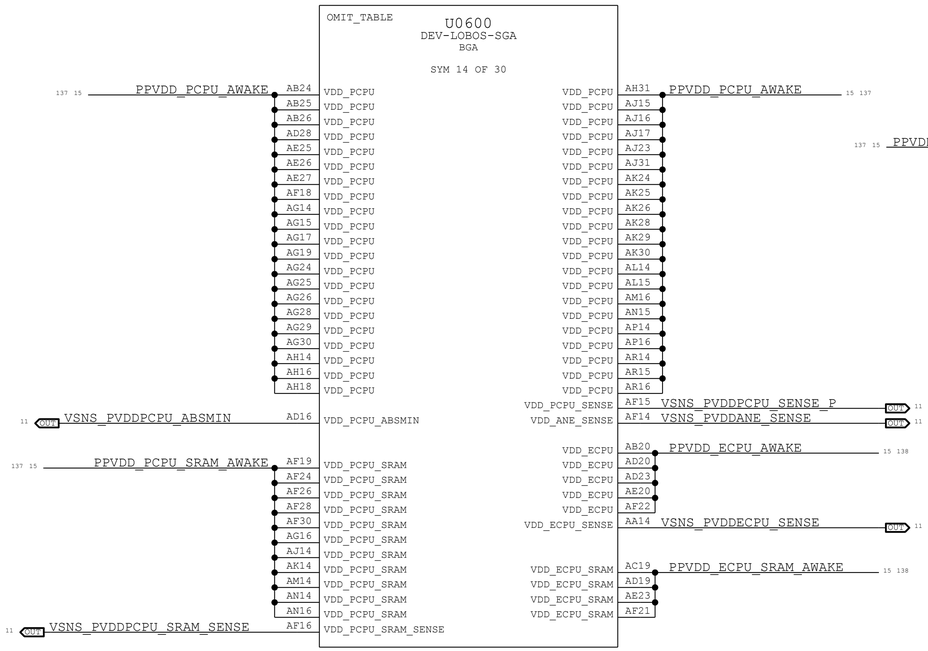

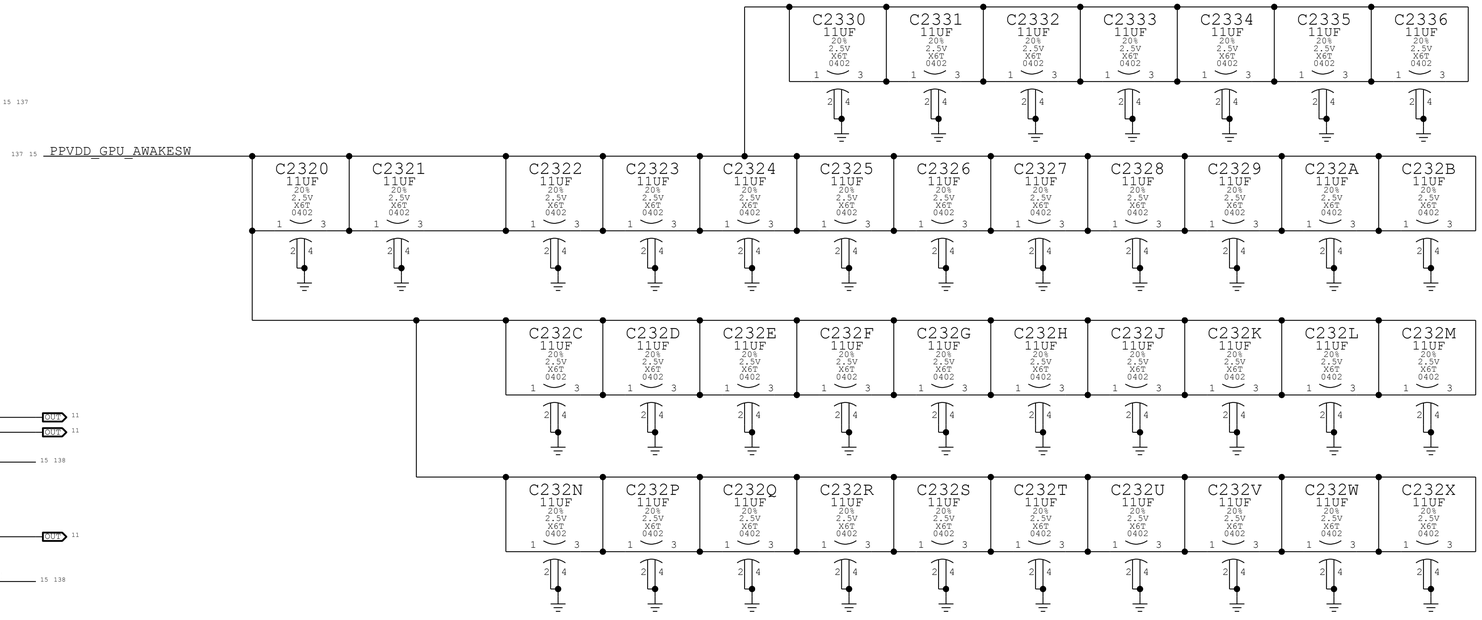

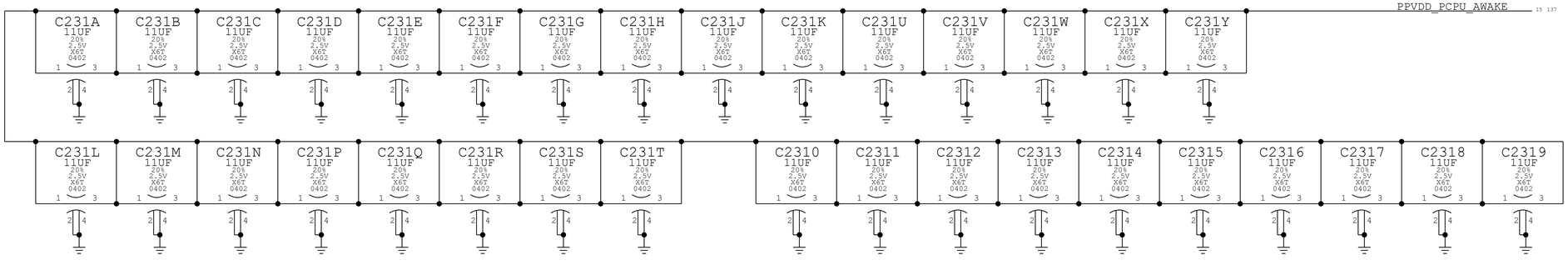

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (CPU, GPU)

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 23 OF 700
SHEET 15 OF 156

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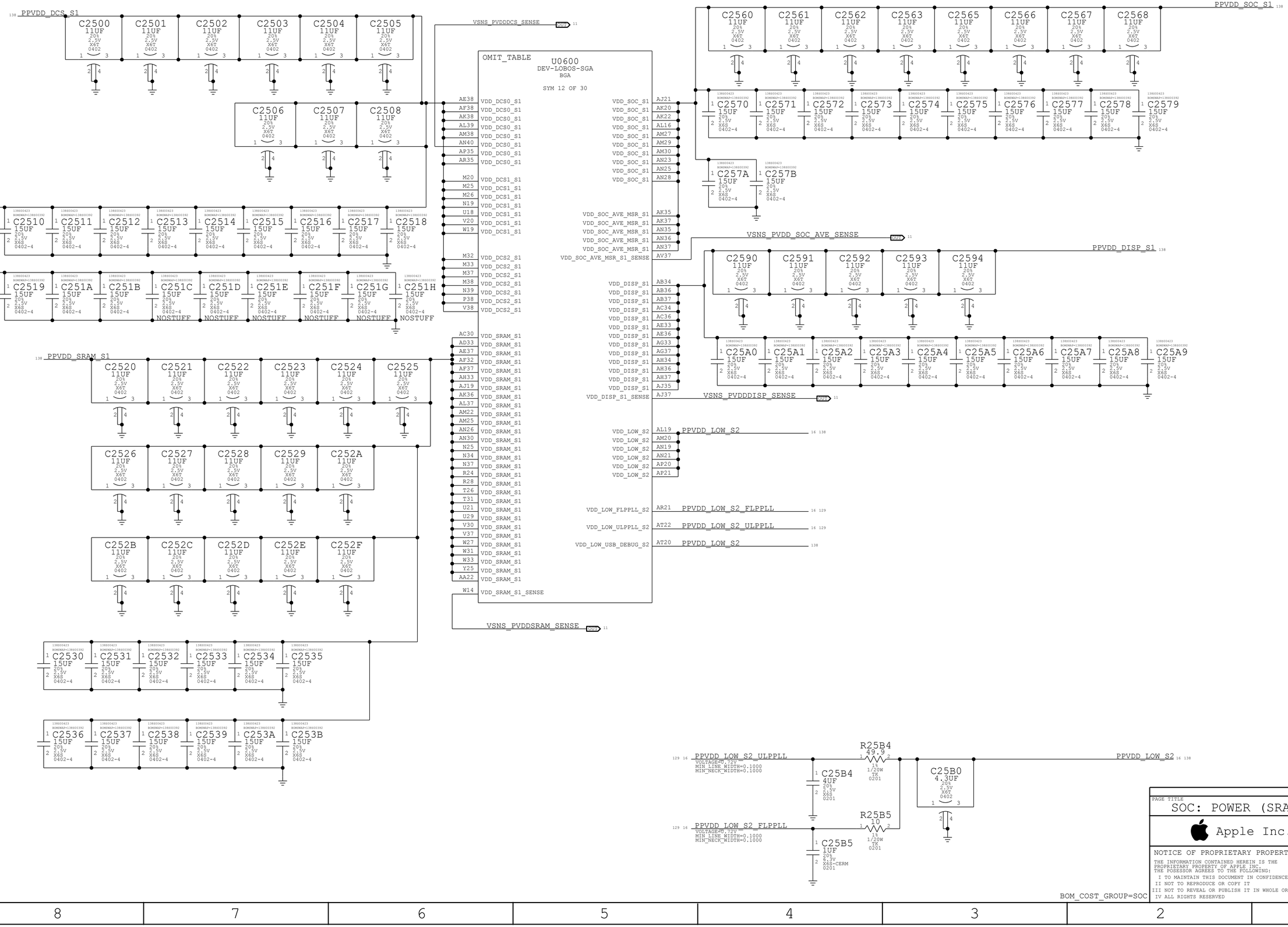

PAGE TITLE	SOC: POWER (SRAM, DISP, DCS)
	Apple Inc.
DRAWING NUMBER	051-08242
SIZE	D
REVISION	4.0.0
BRANCH	dvt-2
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SHEET	16 OF 156

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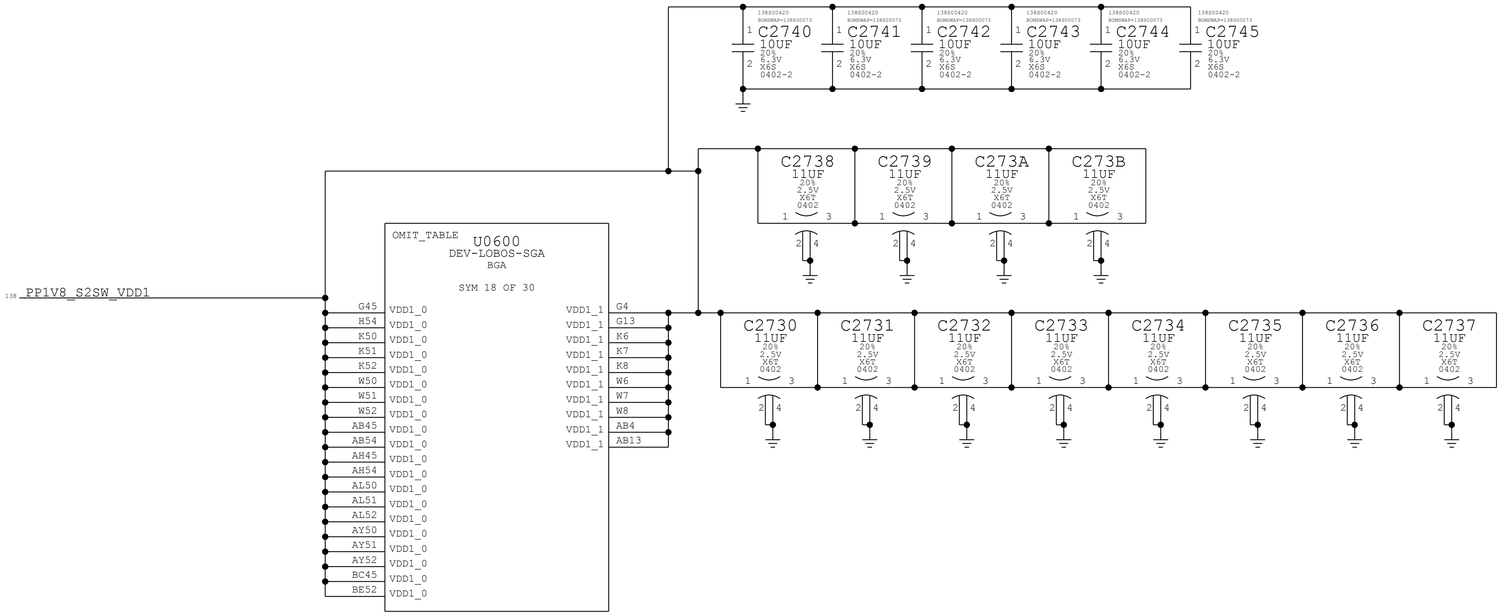

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD1)

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DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
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SHEET 17 OF 156

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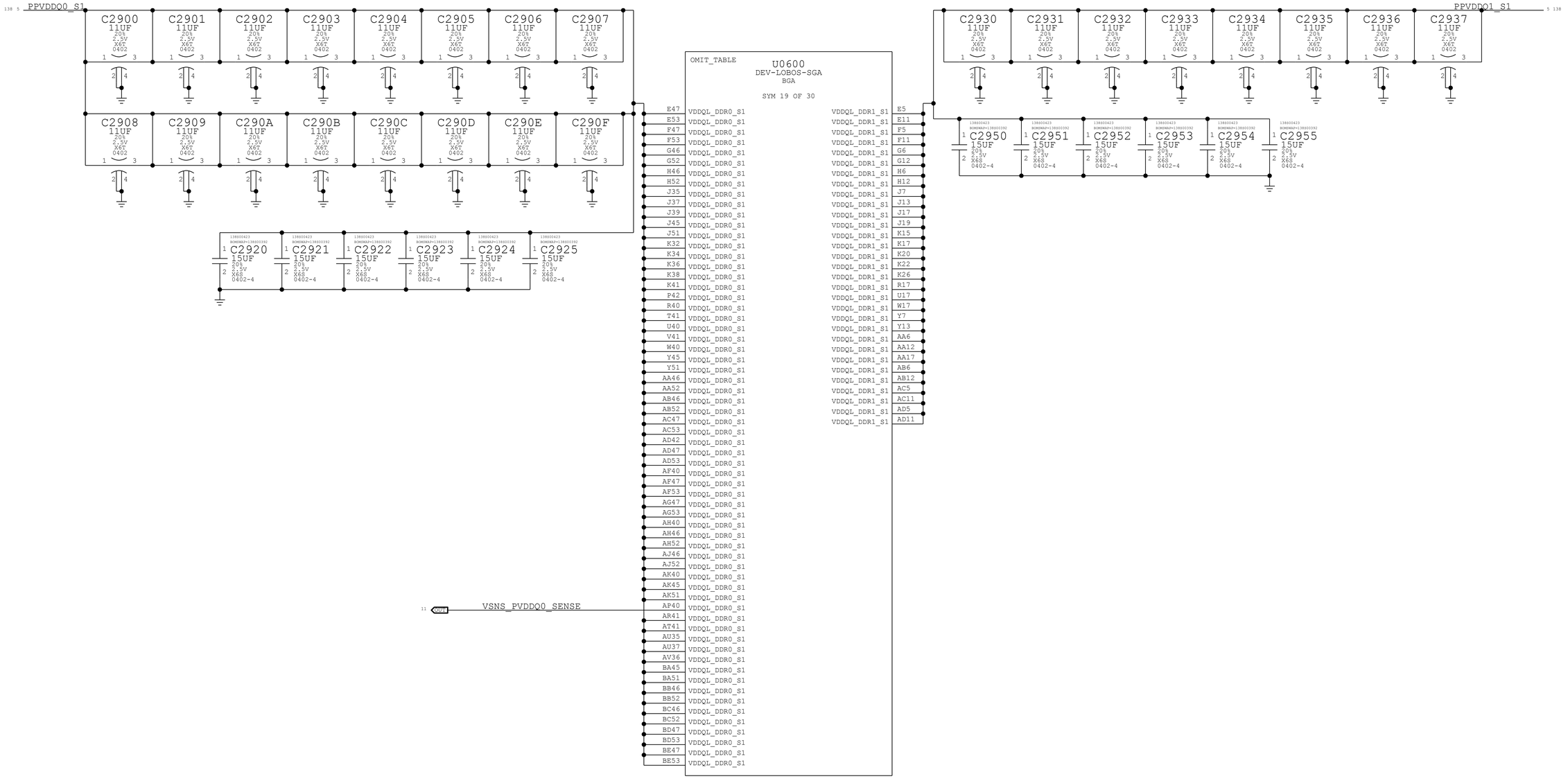

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDDQ)

Apple Inc.

DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 29 OF 700
SHEET 18 OF 156

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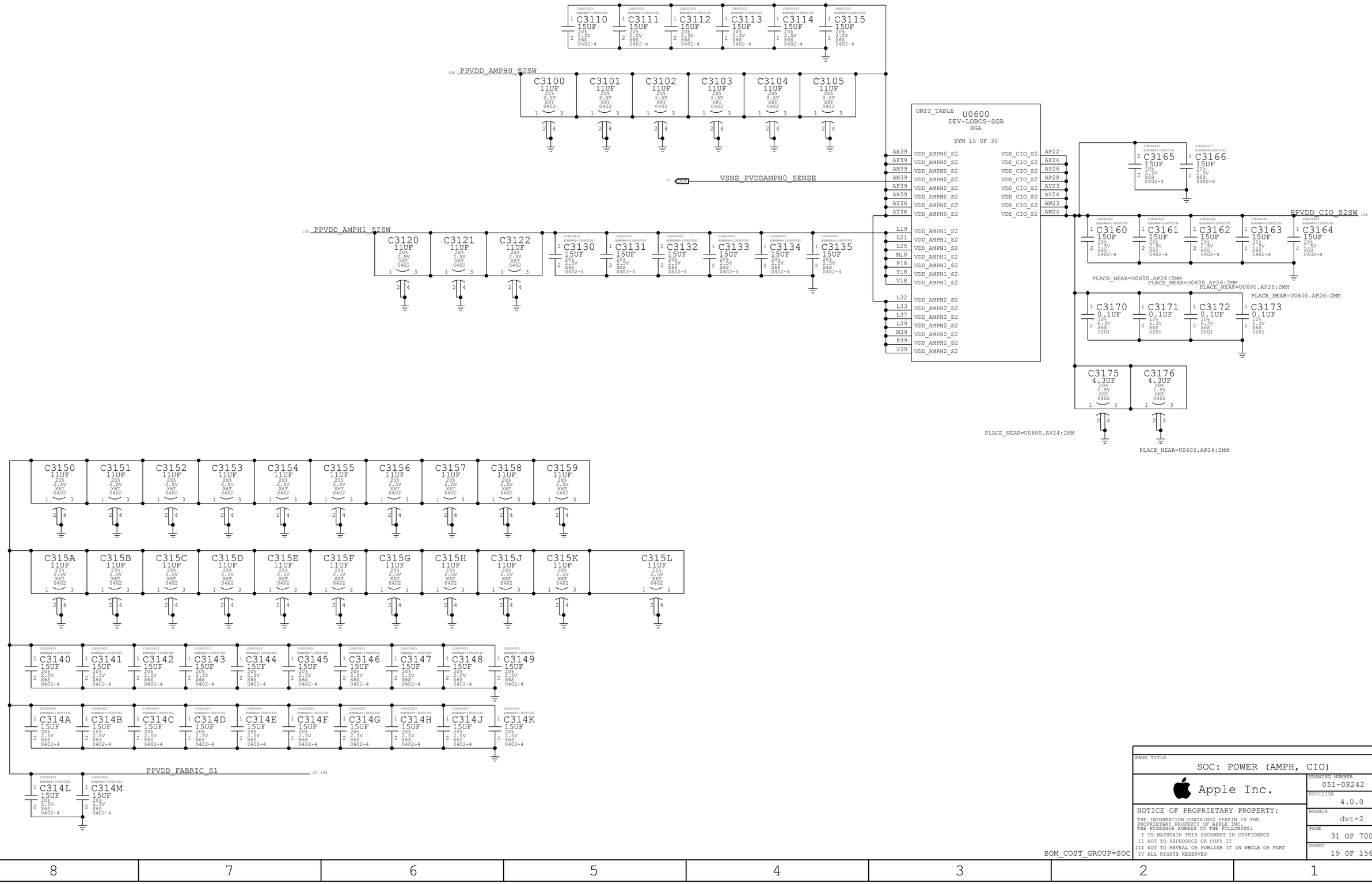

BOM_COST_GROUP=SOC

PAGE TITLE

SOC: POWER (AMPH, CIO)

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D

REVISION 4.0.0

BRANCH dvt-2

PAGE 31 OF 700

SHEET 19 OF 156

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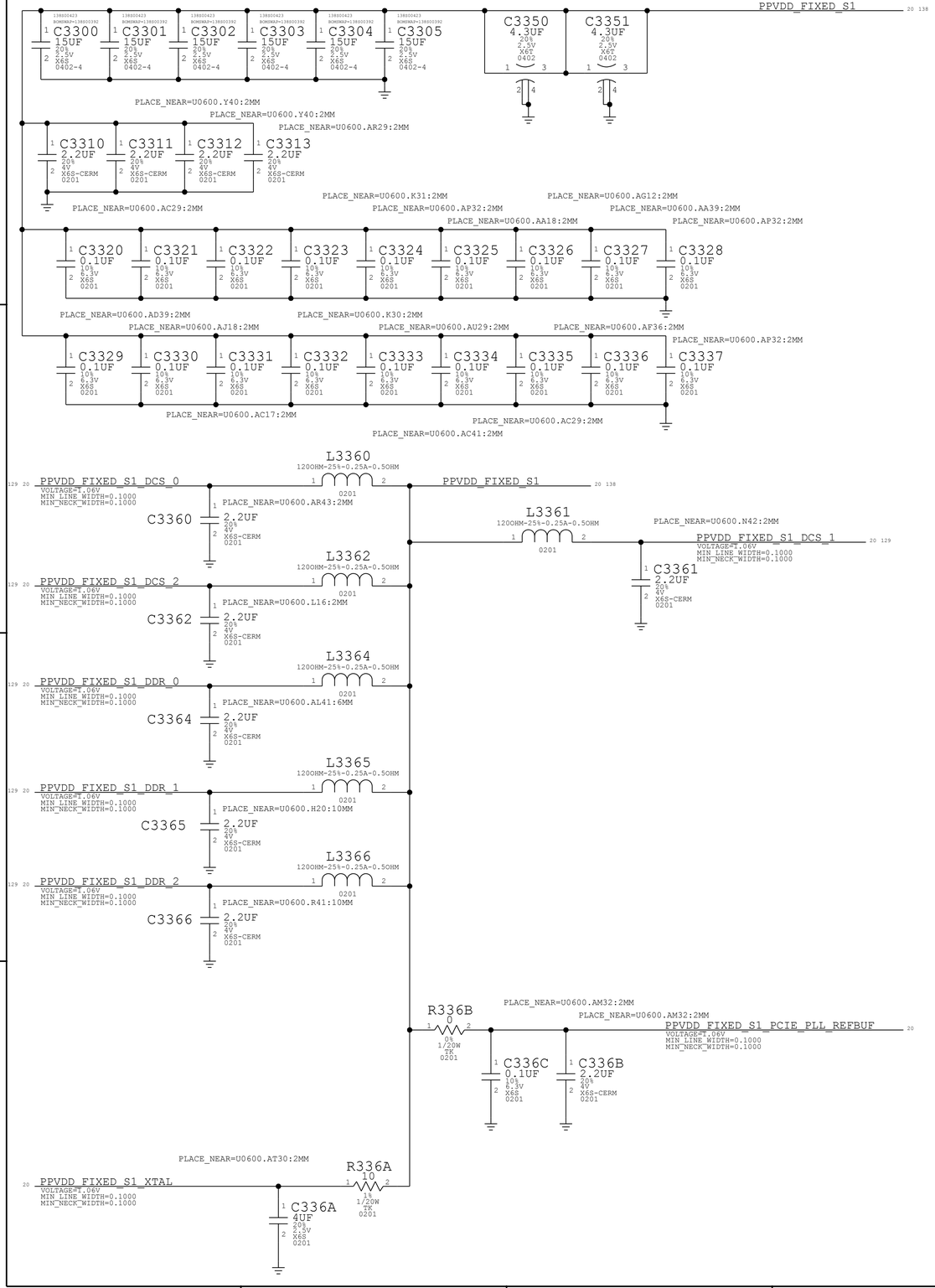

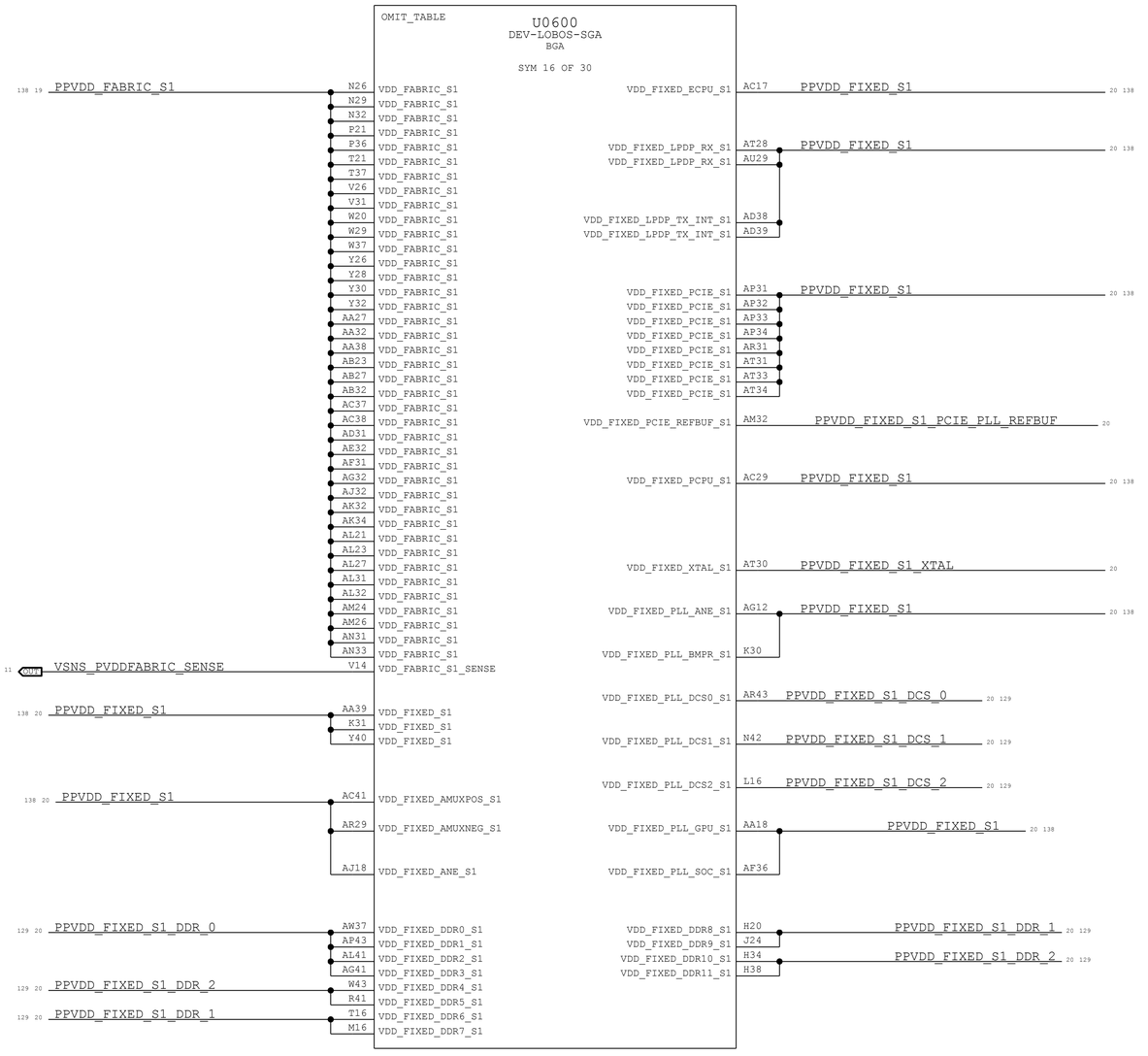

TODO_DT: VDD_FIXED pins have different aliases even if they connect directly to the main rail
This convention is carried over from H13c, and should be revisited... to help simplify aliases
In general if a pin has a different name that VDD_FIXEDx_S1, or VDD_FIXED_<core>_S1, it gets a unique alias

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (FABRIC, FIXED)

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 33 OF 700
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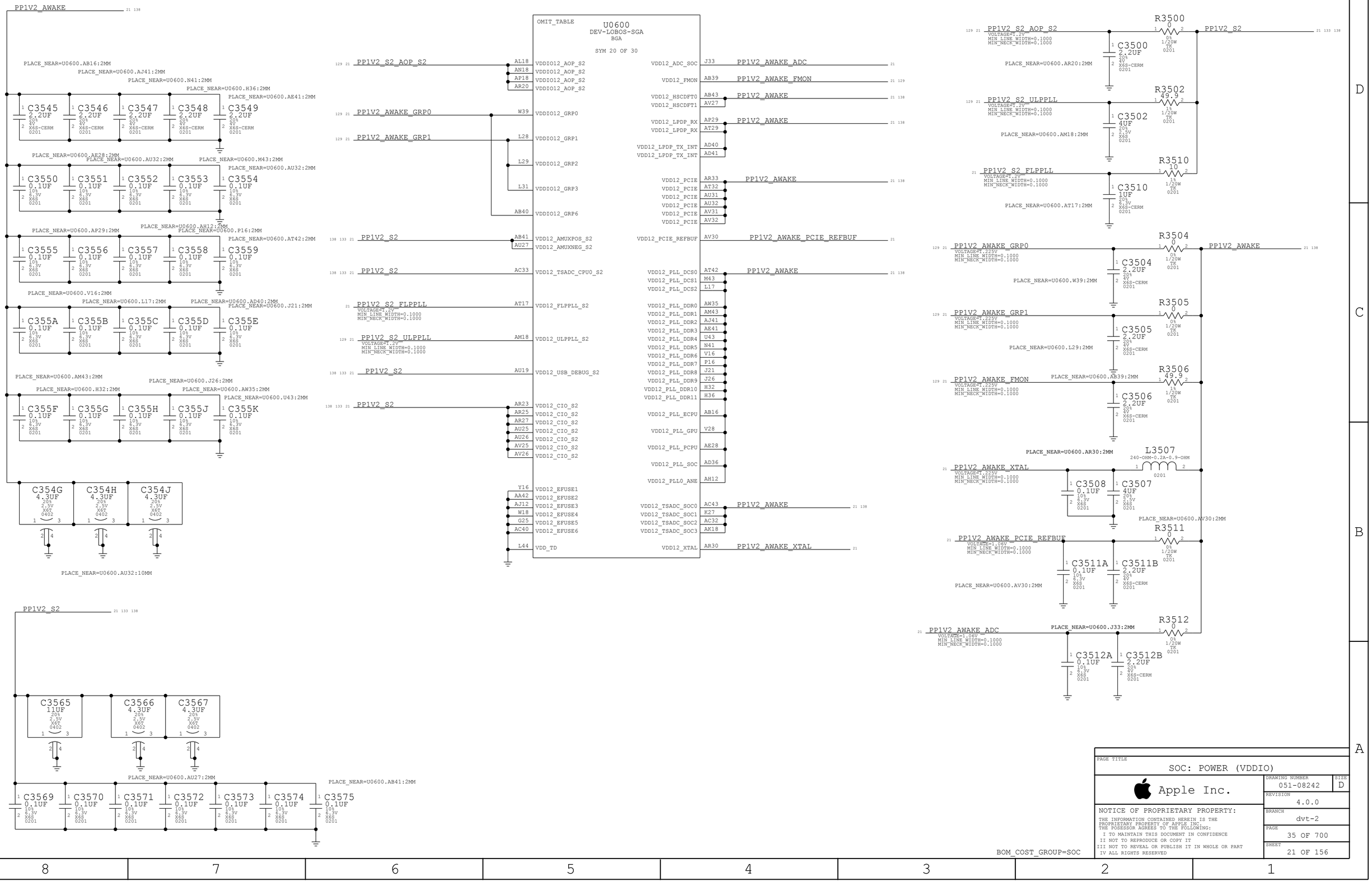
PP1V2_AWAKE
PLACE_NEAR=U0600.AB16:2MM
PLACE_NEAR=U0600.AJ41:2MM
PLACE_NEAR=U0600.N41:2MM
PLACE_NEAR=U0600.H36:2MM
PLACE_NEAR=U0600.AE41:2MM
C3545 2.2UF 20% 4V X6S-CERM 0201
C3546 2.2UF 20% 4V X6S-CERM 0201
C3547 2.2UF 20% 4V X6S-CERM 0201
C3548 2.2UF 20% 4V X6S-CERM 0201
C3549 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=U0600.AE28:2MM
PLACE_NEAR=U0600.AU32:2MM
PLACE_NEAR=U0600.M43:2MM
PLACE_NEAR=U0600.AU32:2MM
C3550 0.1UF 10% 6.3V X6S 0201
C3551 0.1UF 10% 6.3V X6S 0201
C3552 0.1UF 10% 6.3V X6S 0201
C3553 0.1UF 10% 6.3V X6S 0201
C3554 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=U0600.AH12:2MM
PLACE_NEAR=U0600.AP29:2MM
PLACE_NEAR=U0600.P16:2MM
PLACE_NEAR=U0600.AT42:2MM
C3555 0.1UF 10% 6.3V X6S 0201
C3556 0.1UF 10% 6.3V X6S 0201
C3557 0.1UF 10% 6.3V X6S 0201
C3558 0.1UF 10% 6.3V X6S 0201
C3559 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=U0600.V16:2MM
PLACE_NEAR=U0600.L17:2MM
PLACE_NEAR=U0600.AD40:2MM
PLACE_NEAR=U0600.J21:2MM
C355A 0.1UF 10% 6.3V X6S 0201
C355B 0.1UF 10% 6.3V X6S 0201
C355C 0.1UF 10% 6.3V X6S 0201
C355D 0.1UF 10% 6.3V X6S 0201
C355E 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=U0600.AM43:2MM
PLACE_NEAR=U0600.J26:2MM
PLACE_NEAR=U0600.H32:2MM
PLACE_NEAR=U0600.AW35:2MM
PLACE_NEAR=U0600.U43:2MM
C355F 0.1UF 10% 6.3V X6S 0201
C355G 0.1UF 10% 6.3V X6S 0201
C355H 0.1UF 10% 6.3V X6S 0201
C355J 0.1UF 10% 6.3V X6S 0201
C355K 0.1UF 10% 6.3V X6S 0201
C354G 4.3UF 20% 2.5V X6T 0402
C354H 4.3UF 20% 2.5V X6T 0402
C354J 4.3UF 20% 2.5V X6T 0402
PLACE_NEAR=U0600.AU32:10MM
OMIT_TABLE
U0600
DEV-LOBOS-SGA
BGA
SYM 20 OF 30
PP1V2_S2_AOP_S2
AL18 VDDIO12_AOP_S2
AN18 VDDIO12_AOP_S2
AP18 VDDIO12_AOP_S2
AR20 VDDIO12_AOP_S2
PP1V2_AWAKE_GRP0
W39 VDDIO12_GRP0
PP1V2_AWAKE_GRP1
L28 VDDIO12_GRP1
L29 VDDIO12_GRP2
L31 VDDIO12_GRP3
AB40 VDDIO12_GRP6
PP1V2_S2
AB41 VDD12_AMUXPOS_S2
AU27 VDD12_AMUXNEG_S2
PP1V2_S2
AC33 VDD12_TSADC_CPU0_S2
PP1V2_S2_FLPPLL
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
AT17 VDD12_FLPPLL_S2
PP1V2_S2_ULPPLL
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
AM18 VDD12_ULPPLL_S2
PP1V2_S2
AU19 VDD12_USB_DEBUG_S2
PP1V2_S2
AR23 VDD12_CIO_S2
AR25 VDD12_CIO_S2
AR27 VDD12_CIO_S2
AU25 VDD12_CIO_S2
AU26 VDD12_CIO_S2
AV25 VDD12_CIO_S2
AV26 VDD12_CIO_S2
Y16 VDD12_EFUSE1
AA42 VDD12_EFUSE2
AJ12 VDD12_EFUSE3
W18 VDD12_EFUSE4
G25 VDD12_EFUSE5
AC40 VDD12_EFUSE6
L44 VDD_TD
VDD12_ADC_SOC J33 PP1V2_AWAKE_ADC
VDD12_FMON AB39 PP1V2_AWAKE_FMON
VDD12_HSCDFT0 AB43 PP1V2_AWAKE
VDD12_HSCDFT1 AV27
VDD12_LPDP_RX AP29 PP1V2_AWAKE
VDD12_LPDP_RX AT29
VDD12_LPDP_TX_INT AD40
VDD12_LPDP_TX_INT AD41
VDD12_PCIE AR33 PP1V2_AWAKE
VDD12_PCIE AT32
VDD12_PCIE AU31
VDD12_PCIE AU32
VDD12_PCIE AV31
VDD12_PCIE AV32
VDD12_PCIE_REFBUF AV30 PP1V2_AWAKE_PCIE_REFBUF
VDD12_PLL_DCS0 AT42 PP1V2_AWAKE
VDD12_PLL_DCS1 M43
VDD12_PLL_DCS2 L17
VDD12_PLL_DDR0 AW35
VDD12_PLL_DDR1 AM43
VDD12_PLL_DDR2 AJ41
VDD12_PLL_DDR3 AE41
VDD12_PLL_DDR4 U43
VDD12_PLL_DDR5 N41
VDD12_PLL_DDR6 V16
VDD12_PLL_DDR7 P16
VDD12_PLL_DDR8 J21
VDD12_PLL_DDR9 J26
VDD12_PLL_DDR10 H32
VDD12_PLL_DDR11 H36
VDD12_PLL_ECPU AB16
VDD12_PLL_GPU V28
VDD12_PLL_PCPU AE28
VDD12_PLL_SOC AD36
VDD12_PLL0_ANE AH12
VDD12_TSADC_SOC0 AC43 PP1V2_AWAKE
VDD12_TSADC_SOC1 K27
VDD12_TSADC_SOC2 AC32
VDD12_TSADC_SOC3 AK18
VDD12_XTAL AR30 PP1V2_AWAKE_XTAL
R3500 0 0% 1/20W TK 0201
PP1V2_S2_AOP_S2
PP1V2_S2
VOLTAGE=T.2V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3500 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=U0600.AR20:2MM
R3502 49.9 1% 1/20W TK 0201
PP1V2_S2_ULPPLL
VOLTAGE=T.2V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3502 4UF 20% 2.5V X6S 0201
PLACE_NEAR=U0600.AM18:2MM
R3510 10 1% 1/20W TK 0201
PP1V2_S2_FLPPLL
VOLTAGE=T.2V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3510 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U0600.AT17:2MM
R3504 0 0% 1/20W TK 0201
PP1V2_AWAKE_GRP0
PP1V2_AWAKE
VOLTAGE=T.225V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3504 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=U0600.W39:2MM
R3505 0 0% 1/20W TK 0201
PP1V2_AWAKE_GRP1
VOLTAGE=T.225V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3505 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=U0600.L29:2MM
R3506 49.9 1% 1/20W TK 0201
PP1V2_AWAKE_FMON
PLACE_NEAR=U0600.AB39:2MM
VOLTAGE=T.225V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3506 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=U0600.AR30:2MM
L3507 240-OHM-0.2A-0.9-OHM 0201
PP1V2_AWAKE_XTAL
VOLTAGE=T.225V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3508 0.1UF 10% 6.3V X6S 0201
C3507 4UF 20% 2.5V X6S 0201
PLACE_NEAR=U0600.AV30:2MM
R3511 0 0% 1/20W TK 0201
PP1V2_AWAKE_PCIE_REFBUF
VOLTAGE=1.06V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3511A 0.1UF 10% 6.3V X6S 0201
C3511B 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=U0600.AV30:2MM
R3512 0 0% 1/20W TK 0201
PP1V2_AWAKE_ADC
PLACE_NEAR=U0600.J33:2MM
VOLTAGE=1.06V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
C3512A 0.1UF 10% 6.3V X6S 0201
C3512B 2.2UF 20% 4V X6S-CERM 0201
PP1V2_S2
C3565 11UF 20% 2.5V X6T 0402
C3566 4.3UF 20% 2.5V X6T 0402
C3567 4.3UF 20% 2.5V X6T 0402
PLACE_NEAR=U0600.AU27:2MM
PLACE_NEAR=U0600.AB41:2MM
C3569 0.1UF 10% 6.3V X6S 0201
C3570 0.1UF 10% 6.3V X6S 0201
C3571 0.1UF 10% 6.3V X6S 0201
C3572 0.1UF 10% 6.3V X6S 0201
C3573 0.1UF 10% 6.3V X6S 0201
C3574 0.1UF 10% 6.3V X6S 0201
C3575 0.1UF 10% 6.3V X6S 0201
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: POWER (VDDIO)
Apple Inc.
DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 35 OF 700
SHEET 21 OF 156
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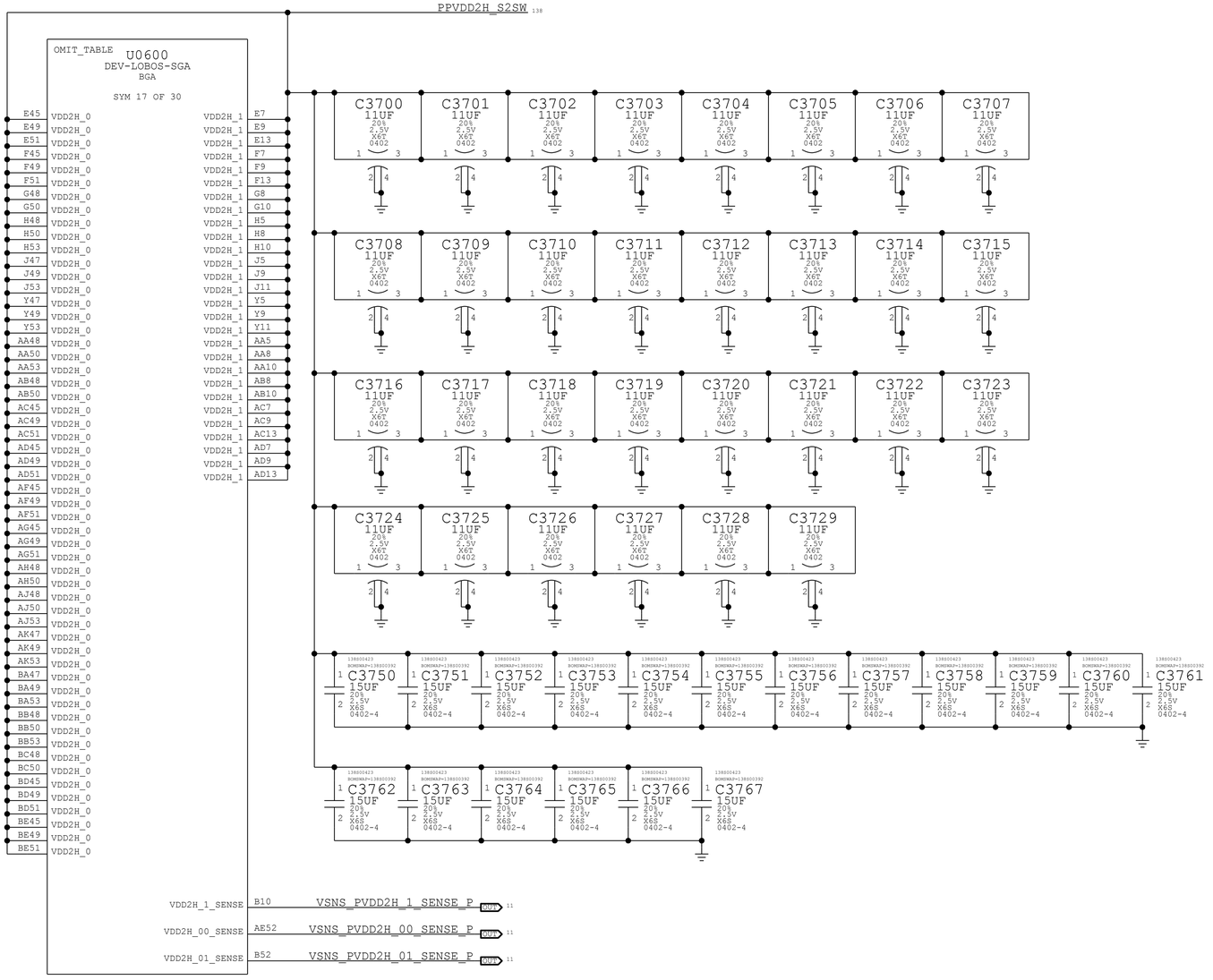

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H)

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DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 37 OF 700
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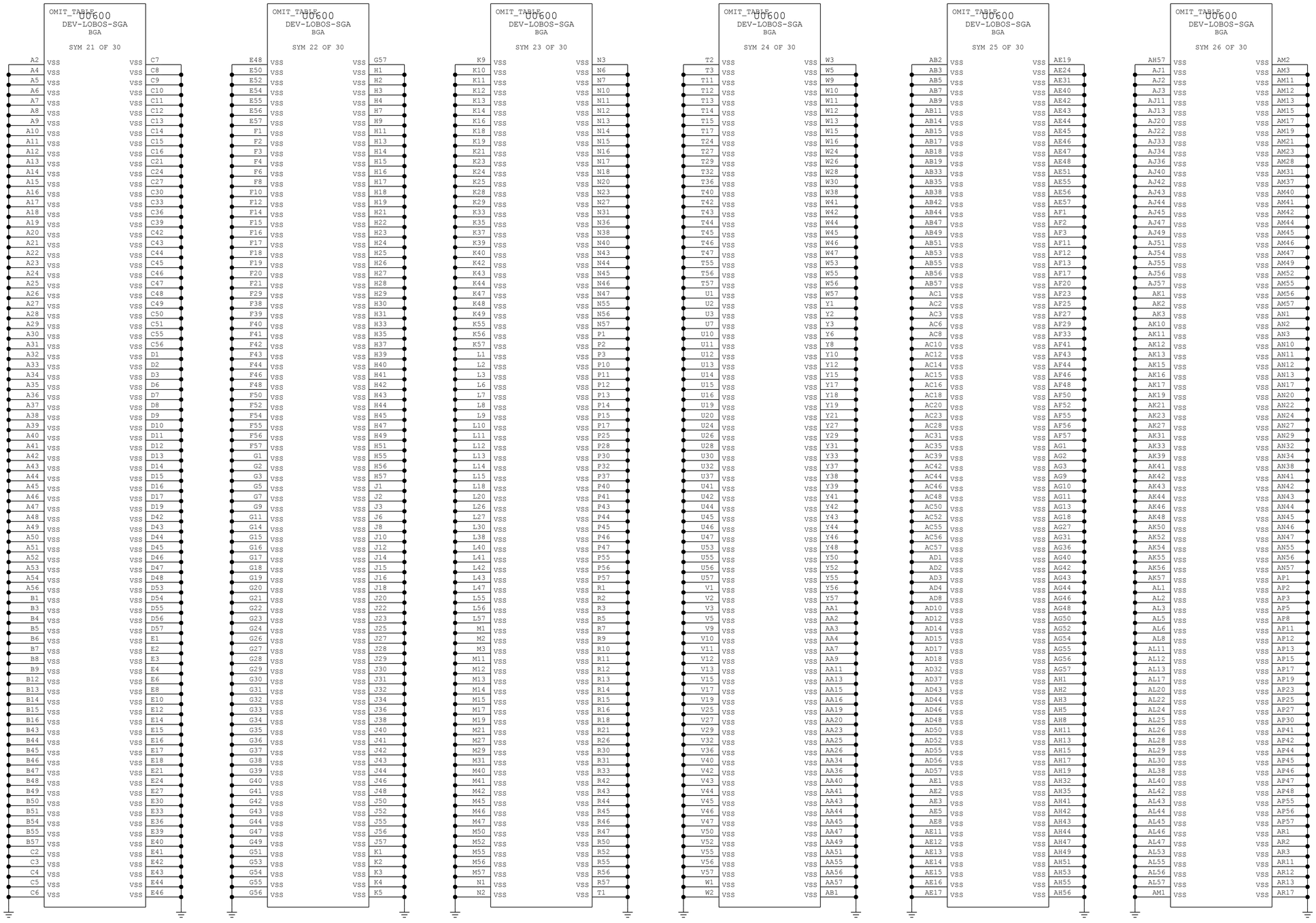

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-1

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REVISION 4.0.0
BRANCH dvt-2
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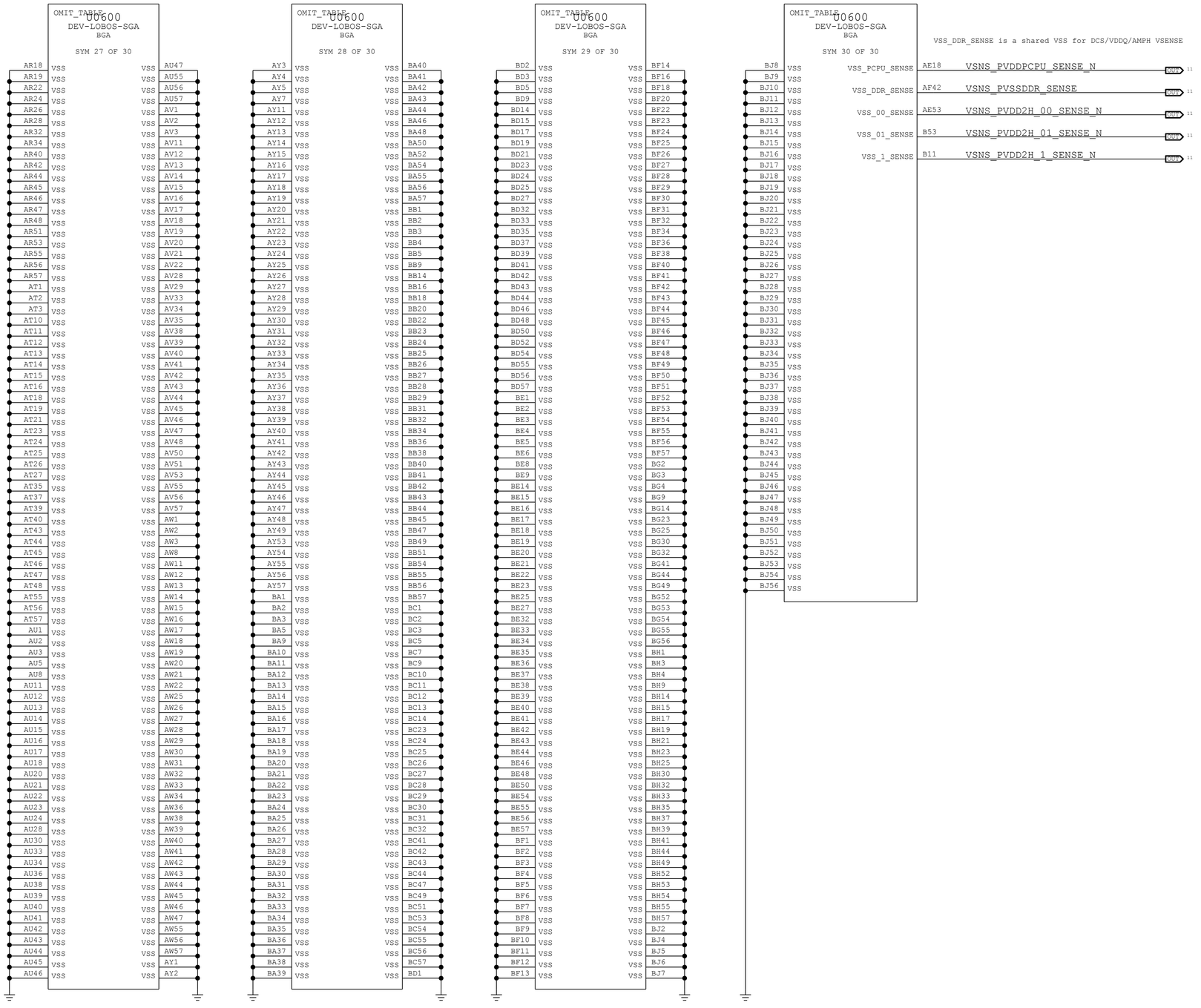

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: GND-2

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BRANCH: dvt-2
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Juno - Secure Element

AONSW nets will connect to S2 rails on
earlier programs and designated AON/AONSW rails
on some later programs. Consult power arch docs.

135 PP1V2_S2
Imax 15mA
ROOM=SE_JUNO
U5000.TB1:3mm
C5011 0.22UF 20% 6.3V X5R 0201

135 PP1V8_S2
Imax 230mA

VDDC_SE VOLTAGE=1.8
VDDA0_SE VOLTAGE=1.8
VDDNV_SE VOLTAGE=1.8
VDDNV_SYS VOLTAGE=1.8

ROOM=SE_JUNO U5000.AT1:3mm
C5014 10UF 20% 6.3V CER-X6S 0402
C5013 1500PF 10% 10V X7R 0201
C5010 0.22UF 20% 6.3V X5R 0201
C5009 0.22UF 20% 6.3V X5R 0201
C5016 0.22UF 20% 6.3V X5R 0201
C5015 0.22UF 20% 6.3V X5R 0201

U5000
SE310S
WLCSP
OMIT_TABLE

NC	B4	AIO	
NC	B3	RFU	
NC	F6	RFU	
NC	G5	RFU	
141 TP_SE_SYS_GPIO0	D1	SYS_GPIO0	
141 NC_SE_SYS_GPIO1	C3	SYS_GPIO1	
141 NC_SE_SYS_GPIO2	C4	SYS_GPIO2	
141 SE_IRQ_WAKE_R	D3	SYS_GPIO3	
141 NC_I2C_SE_SYS_SCL	C2	SYS_I2C_SCL	
141 NC_I2C_SE_SYS_SDA	D2	SYS_I2C_SDA	
12 IN SPMI_SE_CLK	B2	SYS_SPMI_SCLK	
12 IN SPMI_SE_DATA	C1	SYS_SPMI_SDATA	
NC	E1	TM	
SE_GPIO0	G5	NC_SE_SE_GPIO0 141	
SE_GPIO1	F5	TP_SE_SE_GPIO1 141	
SE_GPXC	E6	NC	
SE_GPXI	D6	NC	
SE_I2C_A_SCL	D5	NC_I2C_SE_SE_A_SCL 141	
SE_I2C_A_SDA	E5	NC_I2C_SE_SE_A_SDA 141	
SE_I2C_B_SCL	F4	NC_I2C_SE_SE_B_SCL 141	
SE_I2C_B_SDA	G4	NC_I2C_SE_SE_B_SDA 141	
SE_SPI_CLK	C5	NC	
SE_SPI_CS	E4	NC	
SE_SPI_MISO	G3	NC	
SE_SPI_MOSI	F3	GND IN 141	
RST*	E3	SE_PWR_EN_R	

VDDAO A5, VDDC A2, VDDHI A4, VDDIO B1, VDDIO_AUX F1, VDDIO_ISO C6, VDDLO A3, VDDNV_SE A6, VDDNV_SYS A1
VSS_DIG D4, VSS_DIG E2, VSS_DIG F2, VSS_DIG G1, VSS_DIG G2, VSS_PMU B5, VSS_SUB B6

Form factors should break out GPIO0 to a TP/PP
GPIO 1/2 should be NC'd on Form factors
=SE_SYS_GPIO3 (SE_IRQ_WAKE) should be deprecated pending validation

ROOM=SE_JUNO
R5050 1M 5% 1/20W TF 0201
R5051 1M 5% 1/20W TF 0201

NOSTUFF C5052 1.0UF 20% 6.3V X5R 0201-1 ROOM=SE_JUNO

ROOM=SE_JUNO
R5052 0 0% 1/20W TF 0201
SE_PWR_EN OUT 35 43

Form factors should break out GPIO1 to a TP/PP
and NC-alias GPIO0

<rdar://problem/89368110> [SE310S] Data Sheet
<rdar://problem/90105225> [SE310S] Juno Reference Schematic

BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE: Secure Element

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 50 OF 700
SHEET: 25 OF 156

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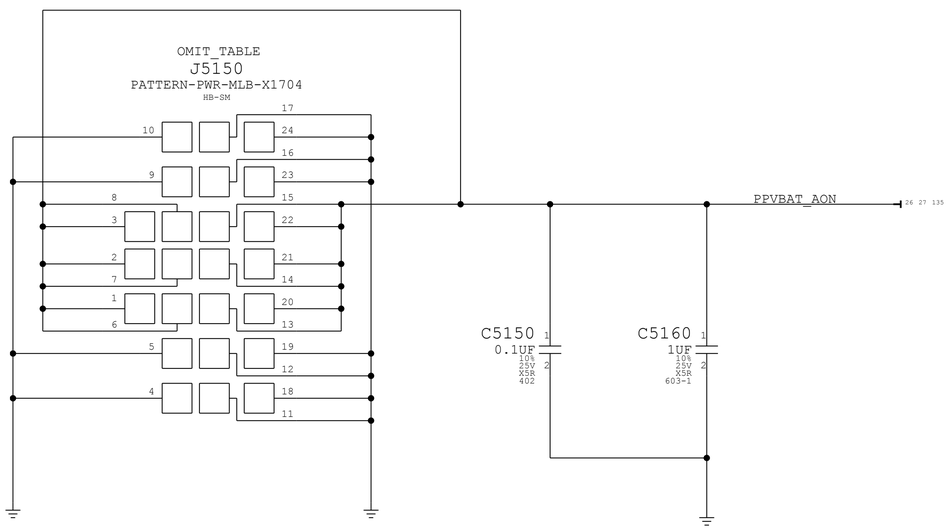
Battery Sub-System Debug Connector

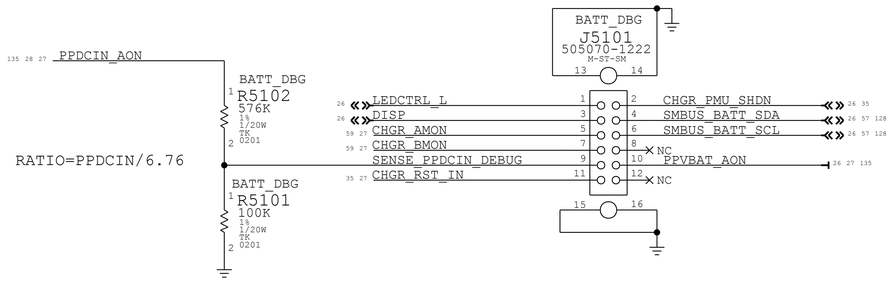
ARKANOID CONN

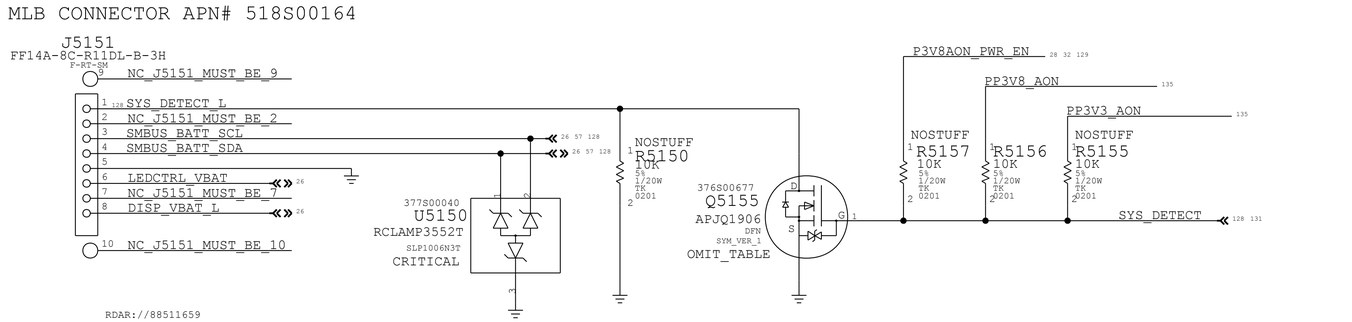
ARKANOID	MLB Connector / Signals		Saleae
J0301 - 1	6	SMBUS_BATT_SCL (= I2C_SMC_PWR_SCL)	0
J0301 - 3	4	SMBUS_BATT_SDA (= I2C_SMC_PWR_SDA)	1
J0301 - 5	2	CHGR_PMU_SHDN	2
J0301 - 7	1	LEDCTRL_L	3
J0302 - 1	3	DISP	4
J0302 - 3	5	CHGR_AMON	5
J0302 - 5	7	CHGR_BMON	6
J0302 - 7	9	1 / 6.76 * PPDCIN_AON	7
J0303 - 1	11	CHGR_RST_IN	8
J0303 - 3	12	—	9
J0303 - 5	10	PPVBAT_AON	10
J0303 - 7	8	—	11

BMU POWER FLEX HOTBAR'd TO THE MLB:

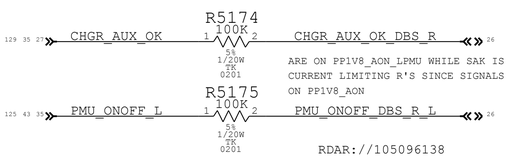
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-04146	1	PCBA,FLEX,BMU-POWER,X1703	J5150	CRITICAL	

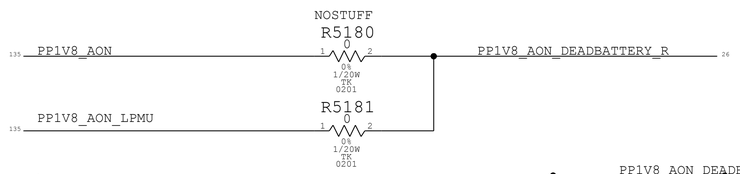


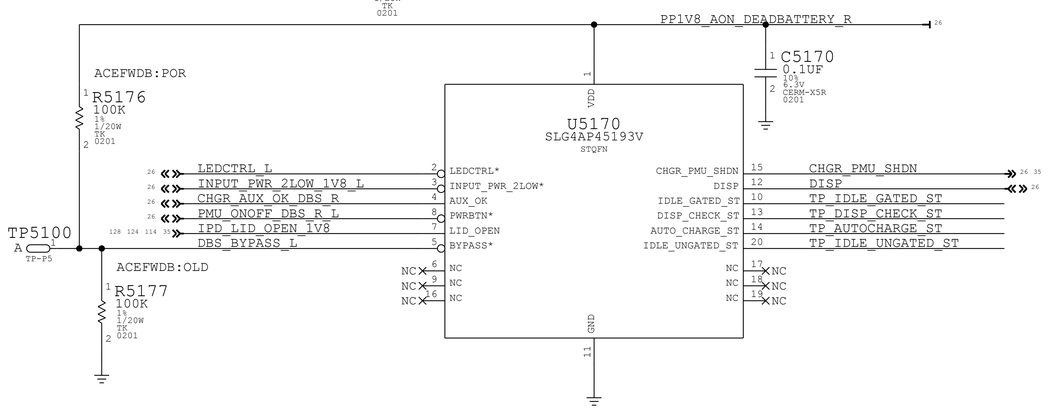




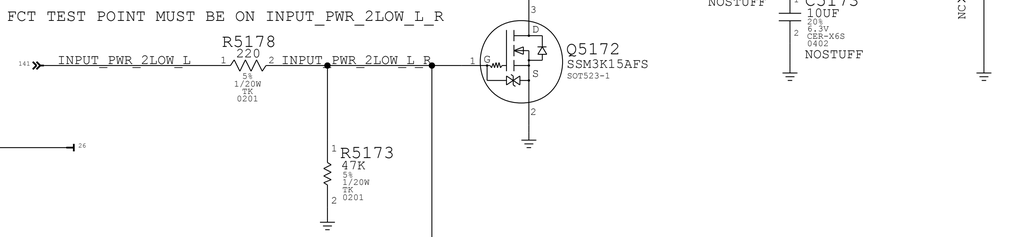
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S00557	1	NFET,30V,440MA,1.2OHM,DFN1006	Q5155	

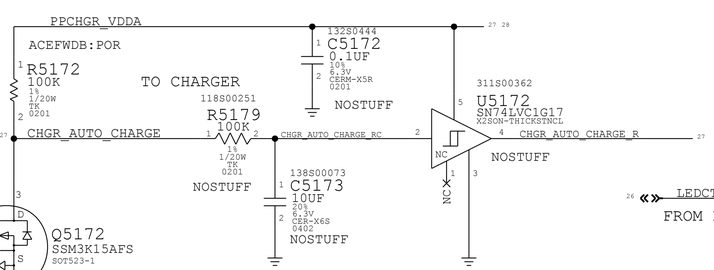


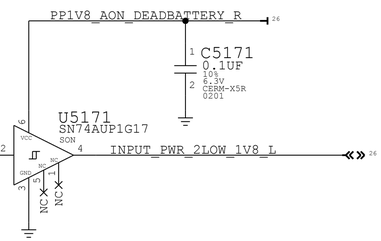


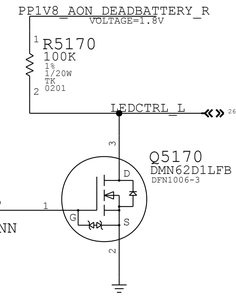


AUTOCHARGE SIGNAL
CONTROLLED BY ACES

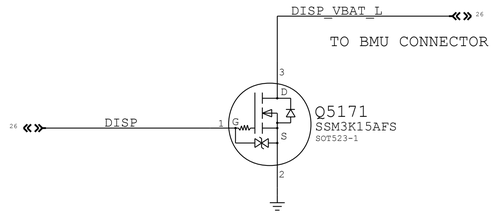








Q5170'S VGS NEEDS TO HANDLE 20V MIN



BOM_COST_GROUP=BATTERY

PAGE TITLE
BATTERY CONN & DEAD BATTERY SAK

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 51 OF 700
SHEET 26 OF 156

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*** OK2INTEGRATE ***

PPDCIN_AON_CHGR_R — VOLTAGE=20V

C5201 6.8UF, C5202 6.8UF, C5203 6.8UF, C5204 6.8UF, C5205 6.8UF, C5206 6.8UF, C5207 6.8UF, C5208 6.8UF — CRITICAL, 20% 35V-0.090HM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011

CHGR_LX1 — DIDT=TRUE SWITCH_NODE=TRUE
R5235 1.5 5% 0.1W TK 0603 110S00153
BOMOPTION=CHGR_PH_SNB
CHGR_SNB1 — DIDT=TRUE SWITCH_NODE=TRUE
C5235 150PF 5% 50V C0G-CERM 0402 131S0514
BOMOPTION=CHGR_PH_SNB

CHGR_LX2 — DIDT=TRUE SWITCH_NODE=TRUE
R5245 1.5 5% 0.1W TK 0603 110S00153
BOMOPTION=CHGR_PH_SNB
CHGR_SNB2 — DIDT=TRUE SWITCH_NODE=TRUE
C5245 150PF 5% 50V C0G-CERM 0402 131S0514
BOMOPTION=CHGR_PH_SNB

152S01218 CRITICAL L5230 2.7UH-20%-16A-0.0148OHM BMCBEJ-SM-COMBO

PPDCIN_AON_CHGR_R — MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1800
C5223 2.2UF 20% 35V X5R-CERM 0402 138S00030 — PLACE_NEAR=U5200.B5:2MM
C520D 2.2UF, C520B 2.2UF, C520C 2.2UF, C520A 2.2UF — 20% 35V X5R-CERM 0402 138S00030

CHGR_LX1 — DIDT=TRUE SWITCH_NODE=TRUE — CRITICAL Q5230 NTTFD2D8N03P1E WQFN-THICKSTNCL 376S00489
CHGR_LX2 — DIDT=TRUE SWITCH_NODE=TRUE — CRITICAL Q5240 NTTFD2D8N03P1E WQFN-THICKSTNCL 376S00489
V+, HSG, SW, LSG, GND

CHGR_GATE_Q1_R — GATE_NODE=TRUE DIDT=TRUE
CHGR_GATE_Q2_R — DIDT=TRUE GATE_NODE=TRUE
R5252 0 NA 0.09W TK 0402-1 116S00021 — PLACE_NEAR=Q5230.2:2MM
CHGR_GATE_Q2 — DIDT=TRUE GATE_NODE=TRUE
R5251 0 NA 0.09W TK 0402-1 116S00021 — PLACE_NEAR=Q5230.7:2MM
CHGR_GATE_Q3_R — DIDT=TRUE GATE_NODE=TRUE
R5253 0 0.09W TK 0402-1 116S00021 — PLACE_NEAR=Q5240.2:2MM
CHGR_GATE_Q3 — DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4_R — GATE_NODE=TRUE DIDT=TRUE

CHGR_LX1 — DIDT=TRUE SWITCH_NODE=TRUE
C5230 0.1UF 10% 25V X7R-CERM-1 0402 132S0438 — PLACE_NEAR=U5200.G1:2MM
CHGR_BOOT1_RC — SWITCH_NODE=TRUE DIDT=TRUE rdar://10419358O
R5230 2 5% 1/16W TK 0402 116S00048 — PLACE_NEAR=U5200.F1:2MM
CHGR_BOOT1 — DIDT=TRUE SWITCH_NODE=TRUE
CHGR_LX2 — DIDT=TRUE SWITCH_NODE=TRUE
C5240 0.1UF 10% 25V X7R-CERM-1 0402 132S0438 — PLACE_NEAR=U5240.B1:2MM
CHGR_BOOT2_RC — DIDT=TRUE SWITCH_NODE=TRUE
R5240 116S00022 0 0% 1/16W TK 0402 — PLACE_NEAR=U5240.7:2MM
CHGR_BOOT2 — DIDT=TRUE SWITCH_NODE=TRUE PLACE_NEAR=U5200.C1:2MM
CHGR_GATE_Q1 — DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4 — DIDT=TRUE GATE_NODE=TRUE

R5254 116S00021 0 NA 0.09W TK 0402-1 — PLACE_NEAR=Q5240.3:2MM
XW5260 SM 1
CHGR_PBUS_SNS_R — PLACE_NEAR=Q5240.7:2MM
R5290 117S00073 0 0% 1/20W TK 0201
CHGR_PBUS_SNS — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
CHGR_CSO_FILT_P
CHGR_CSO_FILT_N

RDAR://92187806 (X2406, REMOVING PBUS FUSES, F5200 AND F5201)

C5296 2.2UF 20% 25V X5R 0402-1 138S0941
C5295 2.2UF 20% 25V X5R 0402-1 138S0941
C5250 27UF, C5251 27UF, C5252 27UF, C5253 27UF, C5254 27UF, C5255 27UF, C5256 27UF, C5257 27UF — CRITICAL, 20% 18V TANT-POLY CASE-B12 128S00107
PPBUS_AON — TO SYSTEM

CRITICAL R5260 0.005 — NO_XNET_CONNECTION=1 — 107S00232 0612-4T 1% 1.5W MF
CHGR_CSO_P — PLACE_NEAR=U5200.A4:4MM
R5261 118S00397 1 1% 1/20W TK 0201
R5262 118S00397 1 1% 1/20W TK 0201
C5260 0.47UF 20% 4V CERM-X5R-1 0201 132S0257 — NO_XNET_CONNECTION=1
C5261 0.047UF 10% 50V CER-X7R 0402 132S0640
C5262 0.047UF 10% 50V CER-X7R 0402 132S0640

(BMON) 2-CELL: 0.010 OHM 3-CELL: 0.005 OHM
CRITICAL Q5265 SI7137DP SO-8 SYM-VER-2 376S0761 ALT1:376S00600 ALT2:376S00614
VOLTAGE=13.35V
PPVBAT_AON_CHGR_R — C5266 2.2UF 20% 25V X5R 0402-1 138S0941; C5265 2.2UF 20% 25V X5R 0402-1 138S0941; C5268 0.01UF 10% 25V X5R-CERM 0201 132S0391; C5267 0.1UF 10% 25V X5R 0201 132S0534
TO/FROM BATTERY — VOLTAGE=13.35V — PPVBAT_AON
MIN_NECK_WIDTH=0.1500 MIN_LINE_WIDTH=0.2500
C5269 0.1UF 10% 25V X5R 0201 132S0534
C5264 1000PF 10% 25V X7R 0201 132S00052
C5263 4700PF 10% 25V CER-X5R 0201-1 132S00390
27 CHGR_BGATE

FROM USB-C SOURCE PPDCIN_AON — 135 28 27 26
(AMON) 2-CELL: 0.02 OHM 3-CELL: 0.01 OHM
CRITICAL R5220 0.01 1% 1W MF 0.5% 0612-1-COMBO 107S00044 — NO_XNET_CONNECTION=1
CRITICAL C5291 6.8UF, DCINCAP_2MORE C5211 6.8UF — 20% 35V-0.090HM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5290 6.8UF, DCINCAP_2MORE C5210 6.8UF — 20% 35V-0.090HM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CHGR_CSI_P — 118S00397 R5221 1 1% 1/20W TK 0201 — PLACE_NEAR=U5200.D5:2MM
CHGR_CSI_N — 118S00397 R5222 1 1% 1/20W TK 0201 — PLACE_NEAR=U5200.C5:2MM
C5220 0.47UF 20% 4V CERM-X5R-1 0201 132S0257 — NO_XNET_CONNECTION=1
C5221 0.1UF 10% 50V CERM-X7R 0402 132S00261
C5222 0.047UF 10% 50V CER-X7R 0402 132S0640

118S00393 R5215 787K 1% 1/20W TK 0201
<RDAR://85838031> Q5216 376S00544 PRIMARY
132S0391 NOSTUFF C5216 0.01UF 10% 25V X5R-CERM 0201
R5216 158K 1% 1/20W TK 0201 118S00358
PACK_IGNORE=TRUE PACK_OPTION=CHGR_DEV
Q5216 SSM3K15AFS SOT523-1 CRITICAL 376S00544 WHAMOLA
R5217 117S00090 10K 5% 1/20W TK 0201 WHAMOLA PACK_IGNORE=TRUE PACK_OPTION=CHGR_DEV

PACK_IGNORE=TRUE PACK_OPTION=CHGR_EXT5V
WHAMOLA R5200 0 116S00014 5% 1/16W MF 0402
PP5V_CHGR_SW_R — PP5V_CHGR_SW
R5275 117S00062 5% 1/20W TK 0201
R5276 117S00109 5% 1/20W TK 0201
PPCHGR_VDDA — VOLTAGE=5V — C5275 2.2UF 20% 25V X5R-CERM 0402-1 138S0769
PPCHGR_VDDP — VOLTAGE=5V — C5277 10UF 20% 6.3V X5R-CERM 0603 138S00695

PLACE_NEAR=U5200.A5:2MM
C5278 138S00030 2.2UF 20% 35V X5R-CERM 0402
C5279 136S00030 2.2UF 20% 35V X5R-CERM 0402 MANDOLA_R_C
C5280 138S0692 1.0UF 20% 6.3V X5R 0201-1
C5271 132S00180 CRITICAL 0.12UF 10% 10V X5R 0402
C5270 132S00180 CRITICAL 0.12UF 10% 10V X5R 0402
R5207 0 0% 1/20W TK 0201 117S00073 — CHGR_COMP_R

U5200 RAA489901 WLCSP 998-28081 CRITICAL OMIT_TABLE

P_IN		GATE_Q1	H1 CHGR_GATE_Q1
CSIN		BOOT1	F1 CHGR_BOOT1
CSIP		LX1	G1 CHGR_LX1
PBUS_PWR		GATE_Q2	E1 CHGR_GATE_Q2
AUX_DET		GATE_Q3	D1 CHGR_GATE_Q3
		LX2	B1 CHGR_LX2
		BOOT2	C1 CHGR_BOOT2
		GATE_Q4	A1 CHGR_GATE_Q4
		PBUS_Q4SNS	A3 CHGR_PBUS_SNS
		CSOP	A4 CHGR_CSO_FILT_P
		CSON	B4 CHGR_CSO_FILT_N
		BGATE	B3 CHGR_BGATE
		VBAT	C3 CHGR_VBAT
		EN_VR1	F2 NC_CHGR_EN_VR1
		SMC_RST*	H4 NC_CHGR_SMC_RST_L
		IRQ*	H3 CHGR_INT_1V8_L
		TEST	H2 NC_CHGR_TEST
		(5V)EN_MVR	F4 CHGR_EN_MVR
		(OD)AUX_OK	F3 CHGR_AUX_OK
		AMON	D4 CHGR_AMON
		BMON	C4 CHGR_BMON
CHGR_CSI_FILT_N	B5		
CHGR_CSI_FILT_P	D5		
PPBUS_AON	A5		
CHGR_AUX_DET	D3		
PP1V8_CHGR_R	F5	VDDIO1P8	
I2C_SMC_PWR_1V8_SDA	G5	SDA	
I2C_SMC_PWR_1V8_SCL	H5	SCL	
CHGR_RST_IN	G2	SMC_RST_IN	
	G3	HPWR_EN*	
CHGR_COMP	E5	COMP	
PPCHGR_VDDA	G4	CELL	H:3-CELL L:2-CELL
CHGR_AUTO_CHARGE	B2	AUTO_CHARGE(OD)	
PP_SYS5V_CHGR	C2	SYS_5V	
	E4	AUX_SHORT(IPD)	
		AGND	E3
		PGND	E2

MANDOLA_R_C R5205 0 0% 1/20W TK 0201 117S00073 — VOLTAGE=5V
CHGR_AUTO_CHARGE — 0 0% 1/20W TK 0201 117S00073
ACEFWDB:OLD
CHGR_AUTO_CHARGE_R — PACK_IGNORE=TRUE PACK_OPTION=CHGR_DEV
R5202 117S00073 0 0% 1/20W TK 0201
R5203 117S00073 0 0% 1/20W TK 0201 WHAMOLA
R5204 0 0% 1/20W TK 0201 117S00073 — PP5V_S2_HOLD — MANDOLA_R_C
R5206 0 0% 1/20W TK 0201 117S00073 — MANDOLA_R_C
CHGR_AUX_DET_SHORT — CHGR_AUX_DET_SHORT_R
R5201 117S00090 10K 5% 1/20W TK 0201

USBC: ACE GPIO5
MAGSAFE: ACE GPIO6
<RDAR://68945820>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-31512	1	IC,RAA489901,PHIC,MANDOLA,OTP=4,WCSP40	U5200	CRITICAL	MANDOLA_IC:3A

Consult DCDC DRI before removing PP

PP5201 SM P2MM PS 1 CHGR_GATE_Q1 — PLACE_SIDE=TOP
PP5211 1 PS SM P2MM — PLACE_SIDE=BOTTOM PACK_OPTION=PP_LX_BOT
PP5202 SM P2MM PS 1 CHGR_GATE_Q2 — PLACE_SIDE=TOP
PP5212 1 PS SM P2MM — PLACE_SIDE=BOTTOM PACK_OPTION=PP_LX_BOT
PP5203 SM P2MM PS 1 CHGR_GATE_Q3 — PLACE_SIDE=TOP
PP5213 1 PS SM P2MM — PLACE_SIDE=BOTTOM PACK_OPTION=PP_LX_BOT
PP5204 SM P2MM PS 1 CHGR_GATE_Q4 — PLACE_SIDE=TOP
PP5214 1 PS SM P2MM — PLACE_SIDE=BOTTOM PACK_OPTION=PP_LX_BOT
PP5205 SM P2MM PS 1 CHGR_LX1 — PLACE_SIDE=TOP
PP5215 1 PS SM P2MM — PLACE_SIDE=BOTTOM
PP5206 SM P2MM PS 1 CHGR_LX2 — PLACE_SIDE=TOP
PP5216 1 PS SM P2MM — PLACE_SIDE=BOTTOM
PP5207 SM P2MM PS 1 CHGR_EN_MVR — PLACE_SIDE=TOP
PP5208 SM P2MM PS 1 CHGR_INT_1V8_L — PLACE_SIDE=TOP

PP5221 SM P2MM PS 1 CHGR_AUTO_CHARGE — PLACE_SIDE=BOTTOM
PP5220 SM P2MM PS 1 CHGR_AUX_DET_SHORT_R — PLACE_SIDE=BOTTOM
PP5219 SM P2MM PS 1 CHGR_AUX_DET — PLACE_SIDE=BOTTOM
PP5218 SM P2MM PS 1 CHGR_RST_IN — PLACE_SIDE=BOTTOM
PP5200 SM P2MM PS 1 CHGR_AMON — PLACE_SIDE=BOTTOM
PP5209 SM P2MM PS 1 CHGR_BMON — PLACE_SIDE=BOTTOM
PP5210 SM P2MM PS 1 CHGR_AUX_OK — PLACE_SIDE=BOTTOM
PP5217 SM P2MM PS 1 CHGR_EN_MVR — PLACE_SIDE=BOTTOM

BOM_COST_GROUP=BATTERY

XW5263 PLACE_NEAR=J5150.20:5MM — PLACE NEAR BATTERY CONN.
CHGR_VBAT_XW — 117S00077 R5263 1K 5% 1/20W TK 0201-1
CHGR_VBAT
CRITICAL Q5270 376S00224 PMZB550UNE-S500 SOT883B SYM_VER_2
WHAMOLA PACK_IGNORE=TRUE PACK_OPTION=CHGR_DEV
PPDCIN_AON — 118S00364 R5271 200K 1% 1/20W TK 0201
SAVE_BAT_S — SAVE_BAT_G
R5270 117S00119 24K 5% 1/20W TK 0201
CRITICAL D5270 371S00307 DFN0201 DZD5V6LP3-55 ALLOW_APPLE_PREFIX=D
WHAMOLA PACK_IGNORE=TRUE PACK_OPTION=CHGR_DEV
<RDAR://37259372&39763505&84523221>

PAGE TITLE: PBUS SUPPLY & BATTERY CHARGER
Apple Inc.
DRAWING NUMBER: 051-08242 SIZE: D
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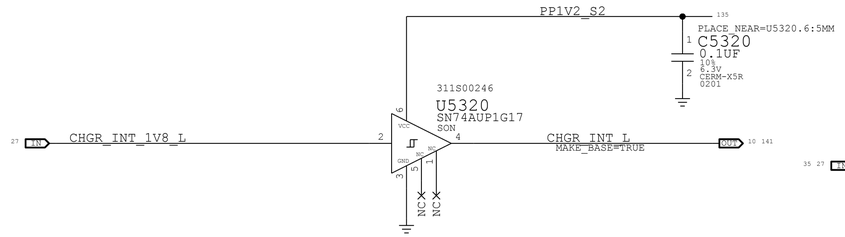
*** OK2INTEGRATE ***

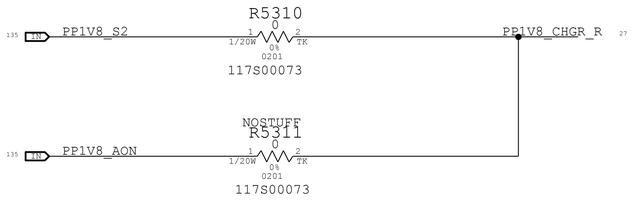
CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

IRQ_L IS PUSH PULL OUTPUT

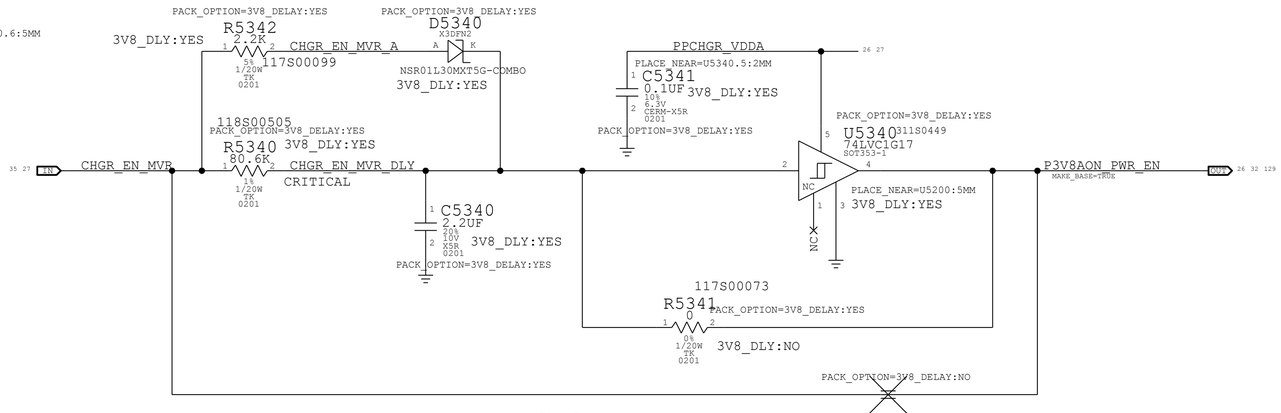




DELAY FOR 3.8V VR ENABLE

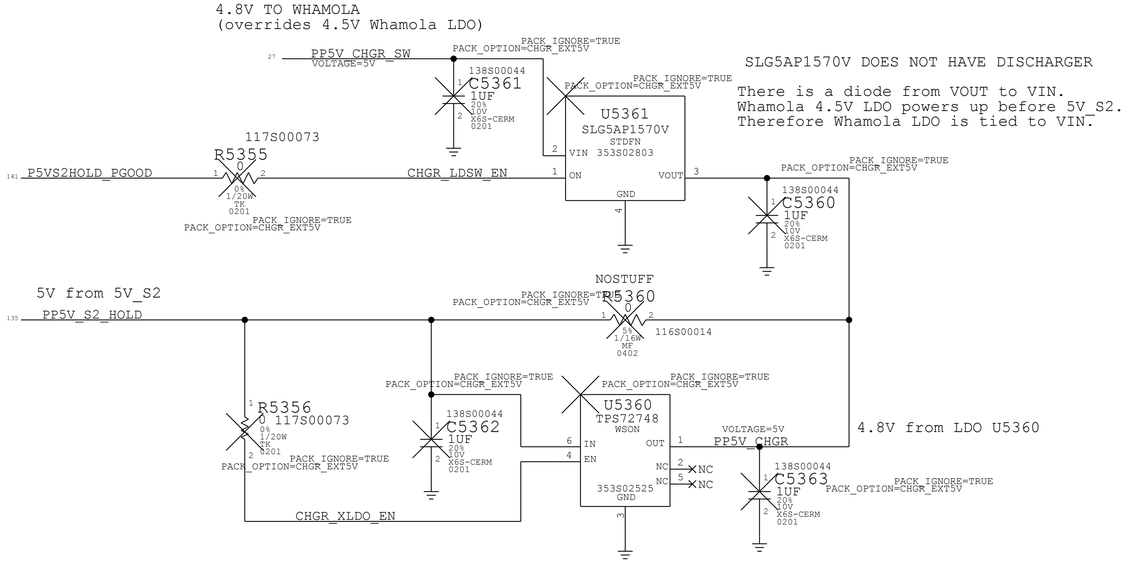
TYPICAL DELAY: RISING = 2MS,
FALLING = 70MS

R5340 AND C5340 UPDATED PER RDAR://62686034
RDAR://84281699



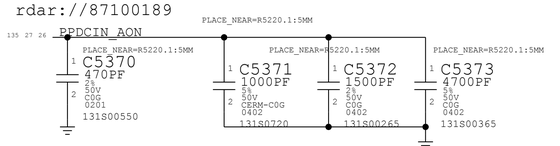
DELAY FOR 3.8V VR ENABLE- BYPASSED

SWITCHOVER TO EXTERNAL 5V



LDO is enabled before the load switch is enabled.
LDO DISABLED TO PREVENT 5V_S2 DISCHARGE BY U5360.

PLACE NEAR R5220
rdar://87100189



BOM_COST_GROUP=BATTERY

PAGE TITLE: BATTERY CHARGER SUPPORT

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
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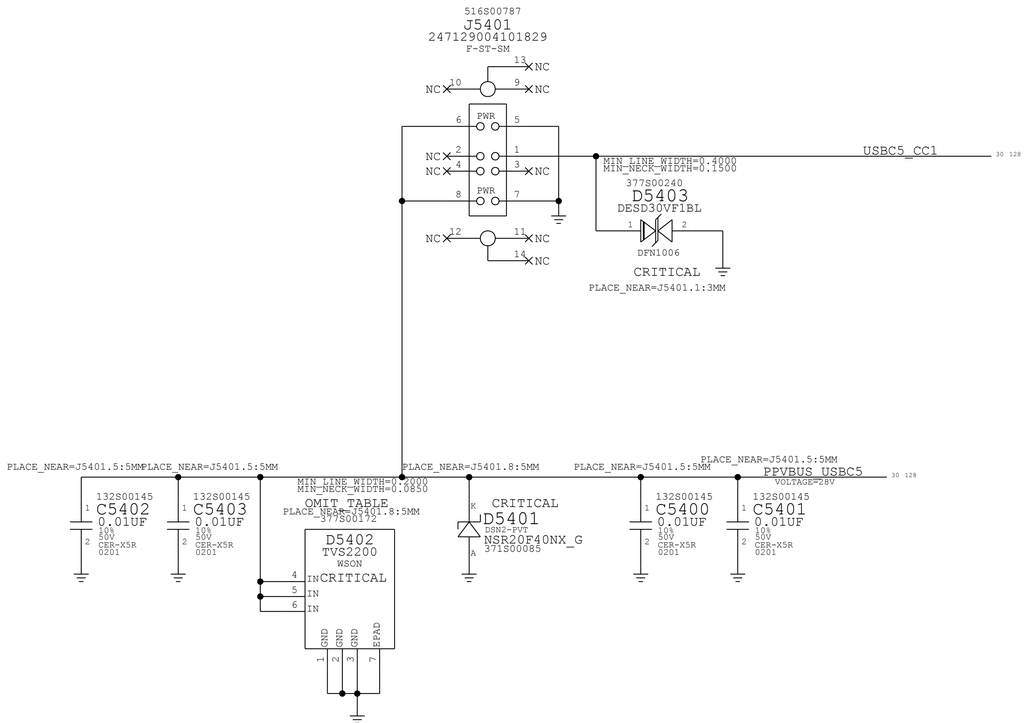
** OK2PLACE **

MAGSAFE B2B connector and VBUS protection



TVS PROTECTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S00172	1	IC,TVS,UNIDIR,22VRWM,28VCL@40A,2X2,SON6	D5402	ACE3:20V
377S00251	1	IC,TVS,UNIDIR,33VRWM,40VCL@35A,2X2,SON6	D5402	ACE3:28V

BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: CONNECTOR

Apple Inc.

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REVISION 4.0.0
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*** IN PROGRESS ***

31 PPHV_INT5_AONSW
MAX 100uF TOTAL ON RAIL

R5500 1K 1% 1/16W TK 0402
VOLTAGE=0V MAKE_BASE=TRUE
ACE5_VCONN — ACE5_VCONN — ACE5_VCONN (MAKE_BASE=TRUE)

PP_5V0 (K10 K12 L9 L11 M10 M12 N9 N11) PP_CABLE (M14 N13) PP_HV (D2 D4 E1 E3 F2 F4 G1 G3 H2 H4 J1 J3 K2 K4 L1 L3 M2 M4 N1 N3) VBUS (D6 D8 E5 E7 F6 F8 G5 G7 H6 H8 J5 J7 K6 K8 L5 L7 M6 M8 N5 N7)

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

1M 1% 1/20W TK 0201 R5501 PD_UART_UPC5_RX_TX 30
100K 5% 1/20W TK 0201 R5502 PD_UPC5_MRESET 30
100K 5% 1/20W TK 0201 R5503 PD_UPC5_HPD 30
100K 5% 1/20W TK 0201 R5521 UPC5_GPIO21 30
100K 5% 1/20W TK 0201 R5522 UPC5_GPIO18 (MAKE_BASE=TRUE) 30
UPC5_GPIO18

GND 30
PACK_OPTION=UPC5_STRAP3:GND
NOSTUFF 0 0% 1/20W TK 0201 R5515 UPC5_STRAP3_I2C_ADDR0 30
PACK_OPTION=UPC5_STRAP3:RPD
NOSTUFF 140K 1% 1/20W TK 0201 R5516 UPC5_STRAP4_I2C_ADDR1 30
UPC5 ADDRESS: ADDR0=NC ADDR1=NC
GND 30
GND 30
MAKE_BASE=TRUE

U5500
SN2012024
BGA
353S02973
OMIT_TABLE

	M22	HRESET	
30 PD_UPC5_MRESET	H18	GPIO14_MRESET	
NC_UPC5_RESET_L	B4	GPIO15_RESETZ	
31 UART UPC5_SER_DBG	F26	GPIO0	
31 BI UPC5_GPIO1	D18	GPIO1	
31 BI UPC5_GPIO2	K24	GPIO2	
31 BI UPC5_GPIO3	L21	GPIO3	
31 BI UPC5_GPIO4	J25	GPIO4	
31 BI UPC5_GPIO5	J9	GPIO5	
31 BI UPC5_GPIO6	C1	GPIO6	
31 BI UPC5_GPIO7	C5	GPIO7	
31 BI UPC5_GPIO8	F10	GPIO8	
31 BI UPC5_GPIO9	H10	GPIO9	
31 BI UPC5_GPIO10	A3	GPIO10	
31 BI UPC5_GPIO11	L25	GPIO11	
INPUT_PWR_2LOW_L	E11	GPIO12	
31 BI UPC5_GPIO16	M26	GPIO16_DFU_BOOTED_L	
31 BI UPC5_GPIO17	G19	GPIO17_FORCE_RST_REQ	
30 UPC5_GPIO18	L13	GPIO18_LSTXRX	
30 UPC5_GPIO18	C3	GPIO19_LSRX	
89 OUT UPC5_CHGR_AUX_DET_SHORT	N23	GPIO20_SS_HOLD	
30 UPC5_GPIO21	G25	GPIO21_LSX_DIR	
30 GND	J17	STRAP0_BUSPOWER	
30 GND	L27	STRAP1_I2C_SPMI_SEL	
31 IN UPC0_SOC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN	
30 UPC5_STRAP3_I2C_ADDR0	M20	STRAP3_I2C_ADDR0	
30 UPC5_STRAP4_I2C_ADDR1	N21	STRAP4_I2C_ADDR1	
30 GND	J21	STRAP5_VDDIO_CFG	
UPC5_R_OSC	B10	R_OSC	
NC_UPC5_AID0	F14	AID0	
NC_UPC5_AID1	G15	AID1	
NC_UPC5_AID2	H14	AID2	
NC_UPC5_AID3	E15	AID3	
30 UPC5_I2CC_SDA	A25	I2CC_SDA	
30 UPC5_I2CC_SCL	B26	I2CC_SCL	
141 31 30 BI I2C_UPC01_3V3_SDA	K28	I2C1_SDA_GPIO23	
141 31 30 IN I2C_UPC01_3V3_SCL	J27	I2C1_SCL_GPIO22	
NC_INT_I2C_UPC5_L	H26	I2C_IRQ1Z	
89 BI SPMI_UPC5_DATA	N25	SPMI_I2C2_DATA 1V25	
89 IN SPMI_UPC5_CLK	M24	SPMI_I2C2_CLK 1V25	
NC_INT_I2C_SMC_UPC5_L	K26	I2C_IRQ2Z	
31 OUT SPI_UPC5_R_CLK	G27	SPI_CLK	
31 OUT SPI_UPC5_R_MOSI	H28	SPI_COPI	
31 IN SPI_UPC5_R_MISO	F28	SPI_CIPO	
31 OUT SPI_UPC5_R_CS_L	E27	SPI_CSZ	
31 12 BI SWD_UPC_SWDIO5	E25	SWD_DATA IPU	
31 12 IN SWD_UPC_SWCLK5	E23	SWD_CLK IPU	
30 PD_UART_UPC5_RX_TX	D28	UART_RX	
	C27	UART_TX	
UPC5_RP	A15	USB_RP1_P	
UPC5_RP	B16	USB_RP1_N	
UPC5_RP	A17	USB_RP2_P	
UPC5_RP	B18	USB_RP2_N	
UPC5_RP	A19	USB_RP3_P	
UPC5_RP	B20	USB_RP3_N	
UPC5_AUX	D14	AUX_P	
UPC5_AUX	C15	AUX_N	
30 PD_UPC5_HPD	G11	GPIO13_HPDTXRX	
UPC5_DBG	E19	DEBUG0_GPIO24	
UPC5_DBG	F18	DEBUG1_GPIO25	
UPC5_DBG	H22	DEBUG2_GPIO26	
UPC5_DBG	D22	DEBUG3_GPIO27	
UPC5_DBG	G23	DEBUG4_GPIO28	
UPC5_DBG	F22	DEBUG5_GPIO29	
UPC5_DBG	C23	DEBUG6_GPIO30	
UPC5_DBG	D26	DEBUG7_GPIO31	

DIGITAL CORE I/O & CONTROL
POWER
TYPE-C
PORT MUX

R5504 15K 0.1% 1/20W TK 0201 CRITICAL
USE INTERNAL LAYER LIMIT BOARD LEAKAGE

R5505 100K 5% 1/20W TK 0201 UPC5_RP (MAKE_BASE=TRUE)
R5506 100K 5% 1/20W TK 0201 UPC5_AUX (MAKE_BASE=TRUE)
R5507 100K 5% 1/20W TK 0201 UPC5_DBG (MAKE_BASE=TRUE)

PP3V3_UPC5_LDO 30 31
1M 1% 1/20W TK 0201 R5517 UPC5_I2CC_SDA 30
1M 1% 1/20W TK 0201 R5518 UPC5_I2CC_SCL 30
NOSTUFF
1.5K 1% 1/20W TK 0201 R5519 I2C_UPC01_3V3_SDA 30 31 141
1.5K 1% 1/20W TK 0201 R5520 I2C_UPC01_3V3_SCL 30 31 141
NOSTUFF

GROUND
GND
A1 B2 K16 K20 M28 N19 N27

PPVBUS_USBC5 29 128
C5501 1UF 20% 30V X5R 0402
PP3V3_S2 135
C5500 10UF 20% 6.3V CERM 0402
PP1V2_S2 31 135
C5502 1.0UF 20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750 VOLTAGE=3.3V
PP3V3_UPC5_LDO 30 31
C5503 10UF 20% 6.3V CERM 0402
C5504 10UF 20% 6.3V CERM 0402

VIN_3V3 C19
VDDIO C25
LDO_3V3 B22
LDO_1V8 A23 PP1V8_UPC5_LDO VOLTAGE=1.8
VIN_LV B28 UPC5_LV
VOUT_LV B24
SS A5 UPC5_SS
LDO_CORE A21 PP1V5_UPC5_LDO_CORE VOLTAGE=1.5V MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750
C_CC1 M16 N15 USBC5_CC1 (MAKE_BASE=TRUE)
C_CC2 M18 N17 USBC5_CC2 CKPLUS_WAIVE=SINGLE_COMP_NET
RPD_G1 L17 USBC5_CC1
RPD_G2 L19 GND (MAKE_BASE=TRUE)
C_USB_TP A11 USBC5_WPD
C_USB_TN A13 USBC5_WPD
C_USB_BP B12 USBC5_WPD
C_USB_BN B14 USBC5_WPD
C_SBU1 C11 USBC5_WPD
C_SBU2 D10 USBC5_WPD
3V3 LDCM B8 NC_USBC5_LDCM
3V3 LDCM_LB C7 NC_USBC5_LDCM_LB
3V3 LDCM_SENSE A7 USBC5_LDCM_SENSE
3V3 LDCM_COMP B6 USBC5_LDCM_COMP
3V3 LDCM_SW A9 USBC5_LDCM_SW

C5505 10UF 20% 6.3V CERM 0402
C5511 0.68UF 5% 6.3V X6S 0402
R5512 1K 1% 1/20W TK 0201
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500
C5506 220PF 5% 50V C0G 0201-1
R5510 10K 1% 1/16W TK 0402-3 (USBC5_WPD, MAKE_BASE=TRUE)
R5509 10K 1% 1/20W TK 0201
R5508 100K 5% 1/20W TK 0201

ACE3 PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S03508	1	IC,SN2012025,ACE3,A1,USBPD W/20HV,BGA149	U5500	ACE3:20V
353S03507	1	IC,SN2012024,ACE3,A1,USBPD W/28HV,BGA149	U5500	ACE3:28V

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: PORT CONTROLLER
Apple Inc.
DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
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SHEET 30 OF 156

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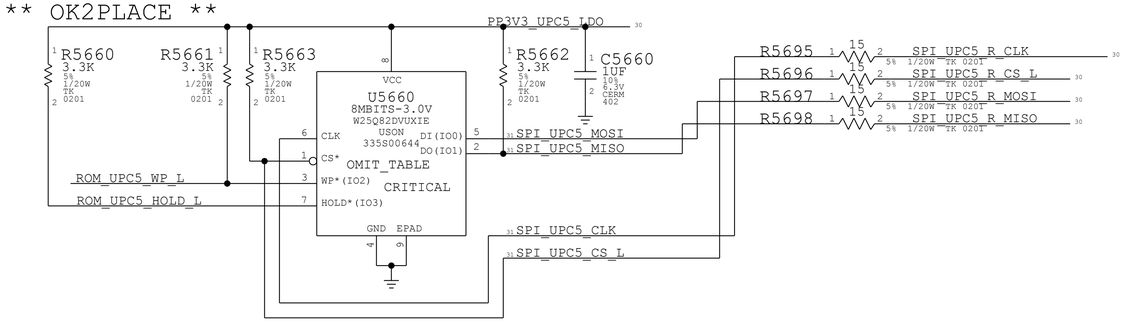
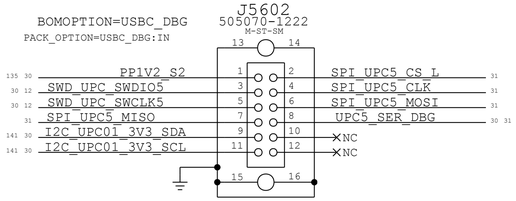
** OK2PLACE **

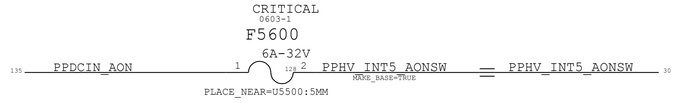


AARDVARKANOID CONN



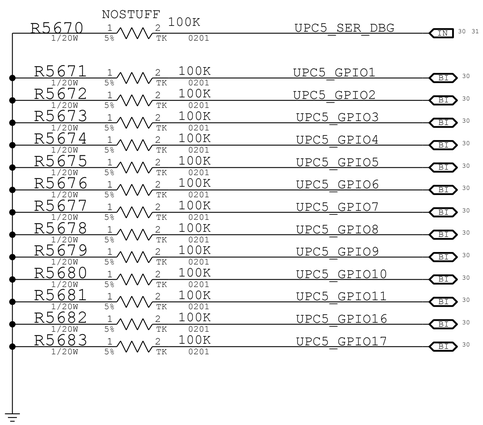
Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CONNECTION TO DCIN



UPC5 FUSE

Unused ports and GPIOs



BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: CONTROLLER SUPPORT

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
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*** OK2INTEGRATE ***

3V8 AON CONTROLLER
42A DESIGN

136 133 33 PPVIN_P3V8AON

5.5 < VIN < 13.5 V

C5704 2.2UF 20% 25V X6S-CERM 0402 138S00042
BYPASS=U5700.8:U5700.33:15MM

135 PP5V_S2_HOLD

4.75 < VDRV < 5.5 V
VDRV IS EXTERNAL OPTION TO POWER IC INSTEAD OF VIN TO SAVE POWER

C5700 10UF 20% 16V X6S 0603-1 138S00248
BYPASS=U5700.6:U5700.33:15MM
0603 SIZE REQUESTED BY DCDC

32 PP5V_AON_P3V8AON

4.75 < LDO5 < 5.25 V
MAX I_OUT TYP 160 MA
LDO5 NOT TO BE USED BY SYSTEM IN 42A DESIGNS

C5702 10UF 20% 16V X6S 0603-1 138S00248
BYPASS=U5700.7:U5700.33:15MM
0603 SIZE REQUESTED BY DCDC

33 P3V8AON_PVCC

C5701 10UF 20% 16V X6S 0603-1 138S00248
BYPASS=U5700.5:U5700.33:15MM
0603 SIZE REQUESTED BY DCDC

129 28 26 PP_EN P3V8AON_PWR_EN — R5710 0 0% 1/20W TK 0201 — P3V8AON_EN_R

VIH_MIN 1.07 V
VIL_MAX 0.63 V

129 35 PP_EN P3V8AON_LPM — R5711 0 0% 1/20W TK 0201 — P3V8AON_LPM_R

VIH_MIN 1.1 V
VIL_MAX 0.5 V

32 PP5V_AON_P3V8AON — R5712 47K 5% 1/20W TK 0201 — P3V8AON_LPM

PU TO INT LDO5 OR OTHER RAIL

P3V8AON_FAULT_L

127 32 I2C_P3V8AON_SCL
127 32 I2C_P3V8AON_SDA

VIH_MIN 1.1 V
VIL_MAX 0.5 V
GND'ED FOR POR (DATASHEET TABLE 1.5)

I2C Address
7 bit: 0x36
8 bit Wr: 0x6C

FAULT PULL DOWN CURRENT 1-2 MA TYPICAL

P3V8AON_IMON

IMON NOT TO BE USED SYSTEM-SIDE
<RDAR://58648650>
IMON IS 2.646 V @ 42 A
VENDOR REQUIRES R>1M, C<50PF

R5750 1M 5% 1/20W TK 0201 117S00096 — P3V8AON_IMON_P3V8AON

C5751 10PF 5% 25V C0G 0201 131S00003

NOSTUFF R5751 2.21K 1% 1/20W TK 0201 118S00367

P3V8AON_GPIO

OPEN FOR PRODUCTION APPLICATION
PER DATASHEET REV 1.0

NOSTUFF R5700 100K 5% 1/20W TK 0201

P3V8AON_SS

LONG STARTUP TIME SO INRUSH BELOW 0.5A USB LIMIT

C5703 0.22UF 10% 25V X5R 0201-1 132S00202

U5700
RAA225501C-R0C1
QFN-THICKSTNCL
OMIT_TABLE
353S02662

"BOM2" SCH SYMBOL IS FOR 42A OTP

8	VIN		
6	VDRV		
7	LDO5		
5	PVCC		
12	ENABLE	(9M PD)	
13	LPM	(9M PD)	
10	SCL		
9	SDA		
14	FAULT*	(OD)	
18	TMON	(0-4.5V)	
11	GPIO		
17	SOFTSTART		
EPAD	33		

F_SW IS REGISTER CONTROLLED
ICCMAX 42A DESIGN: 1 MHZ

BOOT1	4	P3V8AON_BST1	IN 33
UGATE1	3	P3V8AON_DRVH1	OUT 33
PHASE1	2	P3V8AON_SW1	IN 33 133
LGATE1	1	P3V8AON_DRVL1	OUT 33
BOOT2	29	P3V8AON_BST2	IN 33
UGATE2	30	P3V8AON_DRVH2	OUT 33
PHASE2	31	P3V8AON_SW2	IN 33 133
LGATE2	32	P3V8AON_DRVL2	OUT 33
BOOT3	28	P3V8AON_BST3	IN 33
UGATE3	27	P3V8AON_DRVH3	OUT 33
PHASE3	26	P3V8AON_SW3	IN 33 133
LGATE3	25	P3V8AON_DRVL3	OUT 33
VSEN	15	P3V8AON_VSENSE	IN 33
VRTN	16	P3V8AON_VRTN	IN 33
CSP1	19	P3V8AON_ISEN1_P	IN 33
CSN1	20	P3V8AON_ISEN1_N	IN 33
CSP2	21	P3V8AON_ISEN2_P	IN 33
CSN2	22	P3V8AON_ISEN2_N	IN 33
CSP3	23	P3V8AON_ISEN3_P	IN 33
CSN3	24	P3V8AON_ISEN3_N	IN 33

TPT_P3V8AON_PU_RAIL — TP5700 TP-P5 3V8_AON_I2C-DEV

NOSTUFF R5760 1K 5% 1/20W TK 0201-1
NOSTUFF R5761 1K 5% 1/20W TK 0201-1

CKPLUS_WAIVE=I2C_PULLUP
I2C_P3V8AON_SCL 32 127
CKPLUS_WAIVE=I2C_PULLUP
I2C_P3V8AON_SDA 32 127

R5762 0 0% 1/20W TK 0201
R5763 0 0% 1/20W TK 0201

GND MAKE_BASE=TRUE
GND MAKE_BASE=TRUE

rdar://70382922 J129: Iceman BOM2 OTP Tracker

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02662	1	IC,RAA225501B,ICE,BOM2,A2,OTP-R0C1,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_BOM2_R0C1
353S02604	1	IC,RAA225501B,ICE,BOM2,A2,OTP-R0C0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_BOM2_R0C0
353S02473	1	IC,RAA225501C,ICE,BOM2,A1,OTP-R0C0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_BOM2_R0C0

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON (1/2)

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DRAWING NUMBER 051-08242 SIZE D
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SHEET 32 OF 156

*** OK2INTEGRATE ***

42A DESIGN

ICCMAX = 42 A

BOM_COST_GROUP=SOC POWER

PAGE TITLE	POWER: 3V8 AON (2/2)
Apple Inc.	DRAWING NUMBER 051-08242 SIZE D
	REVISION 4.0.0
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	SHEET 33 OF 156

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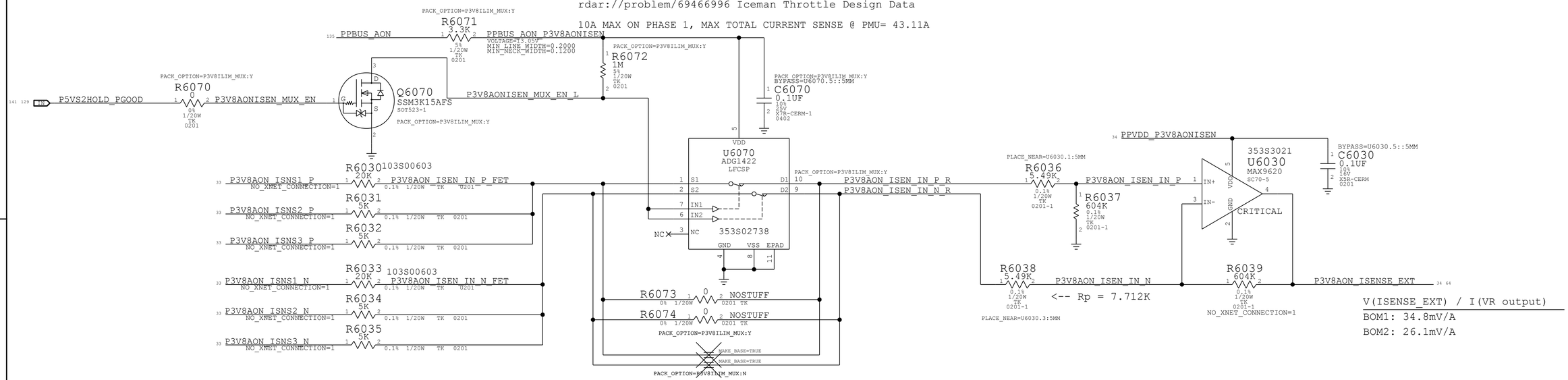
P3V8 LOW SIDE ISENSE AND ILIMIT (SUMMING AMP FOR 3 PHASES)

rdar://problem/69466996 Iceman Throttle Design Data

10A MAX ON PHASE 1, MAX TOTAL CURRENT SENSE @ PMU= 43.11A

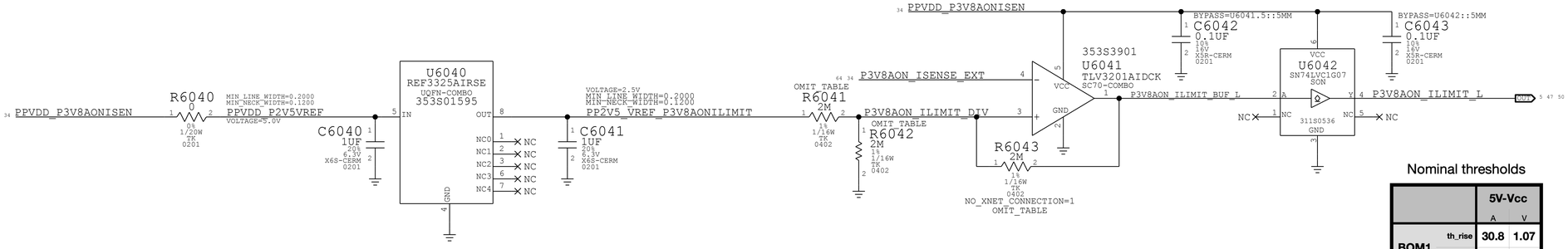


V(ISENSE_EXT) / I(VR output)

BOM1: 34.8mV/A

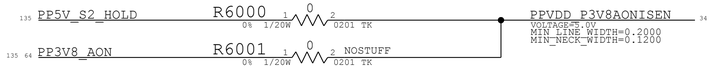
BOM2: 26.1mV/A

PHASE 1 VSENSE GAIN: 8.75
PHASE 2/3 VSENSE GAIN: 35
4:1 WEIGHT FOR PHASE 1 RTREE



Nominal thresholds

		5V-Vcc	
		A	V
BOM1	th_rise	**30.8**	**1.07**
	th_fall	29.3	1.02
BOM2	th_rise	**42.9**	**1.12**
	th_fall	40.6	1.06



Call one of these BOM GROUPs in the main BOM:

BOM GROUP	BOM OPTIONS
P3V8ILIM:BOM1_5V	P3V8ILIM_RT:22K,P3V8ILIM_RB:15K4,P3V8ILIM_RF:866K
P3V8ILIM:BOM2_5V	P3V8ILIM_RT:20K,P3V8ILIM_RB:15K,P3V8ILIM_RF:715K

Don't Call these OPTIONs directly:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S00178	1	RES,0402,1%,1/16W,20K	R6041	P3V8ILIM_RT:20K
114S00277	1	RES,0402,1%,1/16W,22K	R6041	P3V8ILIM_RT:22K
114S00177	1	RES,0402,1%,1/16W,15K	R6042	P3V8ILIM_RB:15K
114S00201	1	RES,0402,1%,1/16W,15.4K	R6042	P3V8ILIM_RB:15K4
114S00179	1	RES,0402,1%,1/16W,715K	R6043	P3V8ILIM_RF:715K
114S00202	1	RES,0402,1%,1/16W,866K	R6043	P3V8ILIM_RF:866K

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON OUTPUT THROTTLE

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

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NC_FPMU_GPIO1 == MAKE_BASE=TRUE NC_FPMU_GPIO1
NC_FPMU_GPIO2 == MAKE_BASE=TRUE NC_FPMU_GPIO2
NC_FPMU_GPIO3 == MAKE_BASE=TRUE NC_FPMU_GPIO3
NC_FPMU_GPIO4 == MAKE_BASE=TRUE NC_FPMU_GPIO4
NC_FPMU_GPIO5 == MAKE_BASE=TRUE NC_FPMU_GPIO5
NC_FPMU_GPIO6 == MAKE_BASE=TRUE NC_FPMU_GPIO6
NC_FPMU_GPIO7 == MAKE_BASE=TRUE NC_FPMU_GPIO7
NC_FPMU_GPIO8 == MAKE_BASE=TRUE NC_FPMU_GPIO8
NC_FPMU_GPIO9 == MAKE_BASE=TRUE NC_FPMU_GPIO9
NC_FPMU_GPIO10 == MAKE_BASE=TRUE NC_FPMU_GPIO10
NC_FPMU_GPIO11 == MAKE_BASE=TRUE NC_FPMU_GPIO11

NC_FPMU_GPIO13 == MAKE_BASE=TRUE NC_FPMU_GPIO13
NC_FPMU_GPIO14 == MAKE_BASE=TRUE NC_FPMU_GPIO14
NC_FPMU_GPIO15 == MAKE_BASE=TRUE NC_FPMU_GPIO15
NC_FPMU_GPIO16 == MAKE_BASE=TRUE NC_FPMU_GPIO16
NC_FPMU_GPIO17 == MAKE_BASE=TRUE NC_FPMU_GPIO17
NC_FPMU_GPIO18 == MAKE_BASE=TRUE NC_FPMU_GPIO18
NC_FPMU_GPIO19 == MAKE_BASE=TRUE NC_FPMU_GPIO19
NC_FPMU_GPIO20 == MAKE_BASE=TRUE NC_FPMU_GPIO20
NC_FPMU_GPIO21 == MAKE_BASE=TRUE NC_FPMU_GPIO21
NC_FPMU_GPIO22 == MAKE_BASE=TRUE NC_FPMU_GPIO22
NC_FPMU_GPIO23 == MAKE_BASE=TRUE NC_FPMU_GPIO23
NC_FPMU_GPIO24 == MAKE_BASE=TRUE NC_FPMU_GPIO24
NC_FPMU_GPIO27 == MAKE_BASE=TRUE NC_FPMU_GPIO27

NC_DP2HDMI_CEC_IRQ == MAKE_BASE=TRUE NC_DP2HDMI_CEC_IRQ
NC_LPMU_GPIO8_RSVD == MAKE_BASE=TRUE NC_LPMU_GPIO8_RSVD
NC_LPMU_GPIO12_RSVD == MAKE_BASE=TRUE NC_LPMU_GPIO12_RSVD
NC_SD_MAIN_PWR_EN == MAKE_BASE=TRUE NC_SD_MAIN_PWR_EN

NC_ENET_LOM_RESET == MAKE_BASE=TRUE NC_ENET_LOM_RESET
NC_PMU_PSU_12V_PGOOD == MAKE_BASE=TRUE NC_PMU_PSU_12V_PGOOD
NC_PMU2_SHDN == MAKE_BASE=TRUE NC_PMU2_SHDN
NC_PMU_WAKE2LF == MAKE_BASE=TRUE NC_PMU_WAKE2LF
NC_FPMU_AMUX_AY == MAKE_BASE=TRUE NC_FPMU_AMUX_AY
NC_FPMU_AMUX_BY == MAKE_BASE=TRUE NC_FPMU_AMUX_BY
NC_LPMU_AMUX_AY == MAKE_BASE=TRUE NC_LPMU_AMUX_AY
NC_LPMU_AMUX_BY == MAKE_BASE=TRUE NC_LPMU_AMUX_BY
NC_LPMU_LDOX_EN == MAKE_BASE=TRUE NC_LPMU_LDOX_EN

IPD_LID_OPEN_1V8 == MAKE_BASE=TRUE IPD_LID_OPEN_1V8 (IN) 26 114 124 128
SDCONN_STATE_CHANGE == MAKE_BASE=TRUE SDCONN_STATE_CHANGE (IN) 97
CHGR_AUX_OK == MAKE_BASE=TRUE CHGR_AUX_OK (IN) 26 27 129
IPD_WAKE_L == MAKE_BASE=TRUE IPD_WAKE_L (IN) 123
SD_PWR_EN == MAKE_BASE=TRUE SD_PWR_EN (OUT) 98
IPD_PWR_EN == MAKE_BASE=TRUE IPD_PWR_EN (OUT) 121 124 129
P3V8AON_LPM == MAKE_BASE=TRUE P3V8AON_LPM (OUT) 32 35 129
LCD_PWR_EN == MAKE_BASE=TRUE LCD_PWR_EN (OUT) 110
BL_PWR_EN == MAKE_BASE=TRUE BL_PWR_EN (OUT) 111 128
BL_PMIC_PWR_EN == MAKE_BASE=TRUE BL_PMIC_PWR_EN (OUT) 112 128
PMU_CLK32K_IPD_R == MAKE_BASE=TRUE PMU_CLK32K_IPD_R 35
EDP_BKLT_1V29_EN == MAKE_BASE=TRUE EDP_BKLT_1V29_EN (IN) 110 129
P5VS2HOLD_PWR_EN == MAKE_BASE=TRUE P5VS2HOLD_PWR_EN 35
P5VS2HOLD_PWR_EN (OUT) 94 129 141

IPD_PWR_EN and P5VS2HOLD_PWR_EN stay high through all Software-controlled Resets
...so IPD rails and PP5V_S2 only disable during ship-mode, and unuexpected resets
(SOCHOT, SPF, astris reset, etc)

PP3V8_AON_LPMU == PP3V8_AON_LPMU 41 43 44 45 136 138
PP3V8_AON_FPMU == PP3V8_AON_FPMU 35 37 39 40 45 136 138
NC_LPMU_VLDORTC == NC_LPMU_VLDORTC MAKE_BASE=TRUE
NC_LPMU_VLDORTC2 == NC_LPMU_VLDORTC2 MAKE_BASE=TRUE
PP3V8_AON_FPMU == PP3V8_AON_FPMU 35 37 39 40 45 136 138
NC_FPMU_LDO2 == NC_FPMU_LDO2 MAKE_BASE=TRUE
PP3V8_AON_FPMU == PP3V8_AON_FPMU 35 37 39 40 45 136 138
NC_FPMU_LDO4 == NC_FPMU_LDO4 MAKE_BASE=TRUE

Scrub these APNs as the build approaches

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-31606	1	Chapel,Portables,LPMU,OTP-API	U8100	CRITICAL	SOC:S
998-31607	1	Chapel,Portables,FPMU,OTP-BPI	U7700	CRITICAL	SOC:S
998-31608	1	Chapel,Portables,LPMU,OTP-CPI	U8100	CRITICAL	SOC:C
998-31609	1	Chapel,Portables,FPMU,OTP-DPI	U7700	CRITICAL	SOC:C

PACK_OPTIONS TO INCLUDE IN NETLIST
PMU_COINCELL:N
PMUOSC:QRTZ
PMU_CFGOTP:GND
VPP:GND
FPMU_SW0
FPMU_LDO3

<- Change :R options to :GND for DVT and beyond
(VPP applies to Spitfire design too)

BOM GROUP	BOM OPTIONS
CHAPEL_PORTABLES	PBUS:3S,PMUOSC:QRTZ

BOM_COST_GROUP=SOC POWER

43 IN SGPIO_CLK0_R — 131S00003 C7400 10PF 5% 25V C0G 0201 — SGPIO_SCLK0
R7400 10 5% 1/20W TK 0201 PLACE_NEAR=U8100.M11:15MM

SGPIO_SCLK0 — R7406 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=U9300.A6:15MM — SGPIO_VDDHVR_CLK (OUT)
R7408 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA200.L1:15MM — SGPIO_CLVR1_CLK (OUT)
R7409 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA300.L1:15MM — SGPIO_CLVR2_CLK (OUT)
R740B 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA500.L1:15MM — SGPIO_CLVR4_CLK (OUT)
R7404 10 5% 1/20W TK 0201 PACK_OPTION=SOC:S PLACE_NEAR=U7700.M1:15MM — SGPIO_FPMU_CLK (OUT) 35 39
R7405 10 5% 1/20W TK 0201 PACK_OPTION=SOC:S PLACE_NEAR=U9300.A6:15MM — SGPIO_PCPUVR_CLK (OUT) 47

R740F 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=U9300.B6:15MM — SGPIO_VDDHVR_DATA (BI)
R740H 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA200.K1:15MM — SGPIO_CLVR1_DATA (BI)
R740I 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA300.K1:15MM — SGPIO_CLVR2_DATA (BI)
R740K 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA500.K1:15MM — SGPIO_CLVR4_DATA (BI)
R740C 10 5% 1/20W TK 0201 PLACE_NEAR=U7700.L11:15MM — SGPIO_FPMU_DATA (BI) 39
R740D 10 5% 1/20W TK 0201 PACK_OPTION=SOC:S PLACE_NEAR=U9300.B6:15MM — SGPIO_PCPUVR_DATA (BI) 47

43 IN SGPIO_CLK1_R — 131S00003 C7401 10PF 5% 25V C0G 0201 — SGPIO_SCLK1
R7401 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=U8100.M10:15MM

SGPIO_SCLK1 — R7403 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=U7700.M11:15MM — SGPIO_FPMU_CLK (OUT) 35 39
R7407 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA100.L1:15MM — SGPIO_CLVR0_CLK (OUT)
R740A 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA400.L1:15MM — SGPIO_CLVR3_CLK (OUT)

R74A1 10 5% 1/20W TK 0201 PLACE_NEAR=U8100.M10:15MM PACK_OPTION=SOC:S — SGPIO_GPUVR_CLK (OUT) 50

R740G 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA100.K1:15MM — SGPIO_CLVR0_DATA (BI)
R740J 10 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C PLACE_NEAR=UA400.K1:15MM — SGPIO_CLVR3_DATA (BI)
R740E 10 5% 1/20W TK 0201 PACK_OPTION=SOC:S PLACE_NEAR=U9600.B6:15MM — SGPIO_GPUVR_DATA (BI) 50

43 BI SGPIO_DATA_R — 131S00003 C7402 10PF 5% 25V C0G 0201 — SGPIO_DATA
R7402 10 5% 1/20W TK 0201 PLACE_NEAR=U8100.L11:15MM

43 41 PP1V2_AON_LPMU
R7425 10K 5% 1/20W 0201 TK NOSTUFF
42 BI LPMU_CRASH0_L — R7420 0 0% 1/20W 0201 TK — FPMU_CRASH0_L (BI) 35 39 129
R7426 10K 5% 1/20W 0201 TK NOSTUFF
43 BI LPMU_CRASH1_L — R7421 0 0% 1/20W 0201 TK — PCPUVR_SCRASH_L (BI) 129 138
R7427 1K 5% 1/20W 0201-1 TK NOSTUFF
BI LPMU_CRASH2_L — R7422 0 0% 1/20W 0201 TK — GPUVR_SCRASH_L (BI) 129 138

141 37 35 PP1V8_AON_FPMU
C7470 0.1UF 10% 25V X5R 0201 PLACE_NEAR=U7470.5:5MM
IN CHGR_EN_MVR — U7470 74LVC1G17 SOT353-1 311S0449 — CHGR_EN_MVR_1V8_R
R7470 1K 5% 1/20W 0201-1
R7471 1K 5% 1/20W TK 0201-1 NOSTUFF
R7475 0 0% 1/20W TK 0201 NOSTUFF — FPMU_CRASH1_L (BI) 35 129

141 37 35 PP1V8_AON_FPMU
C7471 0.1UF 10% 6.3V CERM-X5R 0201 13280444 BYPASS=U7471::3MM
U7471 SN74AUP1G07 X2SON-THICKSTNCL VCC GND NC — FPMU_CRASH0_L (BI) 35 39 129

32K Series R values all tbd from SIPI

35 IN PMU_CLK32K_IPD_R — R7413 22 5% 1/20W TK 0201 — IPD_TOUCH_CLK_CONN (OUT) 123
43 IN PMU_CLK32K_SOC_R — R7412 22 5% 1/20W TK 0201 — PMU_CLK32K_SOC (OUT) 10 127
43 IN PMU_CLK32K_WLBT_R — R7411 22 5% 1/20W TK 0201 — PMU_CLK32K_WLBT (OUT) 99 100
138 43 IN NC_PMU_CLK32K_CLVR_R — R7410 22 5% 1/20W TK 0201 PACK_IGNORE=TRUE PACK_OPTION=SOC:C — NC_PMU_CLK32K_CLVR (OUT) 138
43 IN PMU_FORCE_DFU — R7415 680 5% 1/20W 0201 TK — PMU_UPC_FORCE_DFU (OUT) 131 141

Series R to allow the debug button to overdrive PMU_FORCE_DFU high

For ICs powered by 3V8 or PBUS (** items are known necessary)

129 35 32 P3V8AON_LPM — R7485 100K 5% 1/20W 0201 TK
43 25 SE_PWR_EN — R7480 47K 5% 1/20W 0201 TK
100 99 43 WLBT_PWR_EN — R7486 100K 5% 1/20W 0201 TK
35 P5VS2HOLD_PWR_EN — NOSTUFF R7483 100K 5% 1/20W 0201 TK

135 PP1V8_AON
C7440 0.1UF 10% 25V X5R 0201 PLACE_NEAR=U7440.1:5MM
U7440 SLG4AP43601 STQFN VDD GND
BTN1 BTN2 RESET CHGR_RST_IN
CRITICAL 343S00387
NC NC NC NC NC NC NC NC NC

131 128 125 43 26 IN PMU_ONOFF_L — R7472 100K 5% 1/20W 0201 TK — PMU_ONOFF_R_L
131 128 121 43 IN PMU_RSLOC_RST_L — R7473 100K 5% 1/20W 0201 TK — PMU_RSLOC_RST_R_L

CHGR_RST_IN — OUT 26 27
26 IN CHGR_PMU_SHDN
PLACE_NEAR=U7441.1:5MM C7441 0.1UF 10% 25V X5R 0201
U7441 SN74AUP1G32 SOT553
PMU_SHDN_R — R7441 1K 5% 1/20W TK 0201-1 — PMU_SHDN (OUT) 43 128 131

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Desense Caps for every rail

1 set for 1- and 2- phase BUCKs
2 set for 3- and 4- phase BUCKs

LPMU

138 44 42 PPVDD_SOC_S1
- 0: C7600 12PF 25V NPO-C0G 5% 0201
- C7601 3.0PF +/-0.1PF 0201
- C7602 1.8PF +/-0.1PF 201
- C7603 12PF 25V NPO-C0G 5% 0201
- C7604 3.0PF +/-0.1PF 0201
- C7605 1.8PF +/-0.1PF 201

138 133 44 42 PPVDD_SRAM_S1
- 1: C7610 12PF 25V NPO-C0G 5% 0201
- C7611 3.0PF +/-0.1PF 0201
- C7612 1.8PF +/-0.1PF 201
- C7613 12PF 25V NPO-C0G 5% 0201
- C7614 3.0PF +/-0.1PF 0201
- C7615 1.8PF +/-0.1PF 201

138 44 42 PPVDD_ECPU_AWAKE
- 2: C7620 12PF 25V NPO-C0G 5% 0201
- C7621 3.0PF +/-0.1PF 0201
- C7622 1.8PF +/-0.1PF 201
- C7623 12PF 25V NPO-C0G 5% 0201
- C7624 3.0PF +/-0.1PF 0201
- C7625 1.8PF +/-0.1PF 201

138 44 42 PP1V8_S2SW_VDD1
- 3: C7630 12PF 25V NPO-C0G 5% 0201
- C7631 3.0PF +/-0.1PF 0201
- C7632 1.8PF +/-0.1PF 201

44 42 =PPVOUT_LPMU_BUCK5_REG
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK5:Y
- 5: C7650 12PF 25V NPO-C0G 5% 0201
- C7651 3.0PF +/-0.1PF 0201
- C7652 1.8PF +/-0.1PF 201
- C7653 12PF 25V NPO-C0G 5% 0201
- C7654 3.0PF +/-0.1PF 0201
- C7655 1.8PF +/-0.1PF 201

138 44 42 PPVDDQ1_S1
- 6: C7660 12PF 25V NPO-C0G 5% 0201
- C7661 3.0PF +/-0.1PF 0201
- C7662 1.8PF +/-0.1PF 201

138 44 42 PPVDD_AMPH1_S2SW
- 7: C7670 12PF 25V NPO-C0G 5% 0201
- C7671 3.0PF +/-0.1PF 0201
- C7672 1.8PF +/-0.1PF 201

138 44 43 PP1V2_S2
- 8: C7680 12PF 25V NPO-C0G 5% 0201
- C7681 3.0PF +/-0.1PF 0201
- C7682 1.8PF +/-0.1PF 201

138 44 43 PPVDD_ECPU_SRAM_AWAKE
- 9: C7690 12PF 25V NPO-C0G 5% 0201
- C7691 3.0PF +/-0.1PF 0201
- C7692 1.8PF +/-0.1PF 201

138 41 NC_LPMU_SW2
PACK_IGNORE=TRUE
PACK_OPTION=LPMU_SW2
- SW2: C76M0 12PF 25V NPO-C0G 5% 0201
- C76M1 3.0PF +/-0.1PF 0201
- C76M2 1.8PF +/-0.1PF 201

FPMU

138 40 38 PPVDD_DCS_S1
- 0: C76A0 12PF 25V NPO-C0G 5% 0201
- C76A1 3.0PF +/-0.1PF 0201
- C76A2 1.8PF +/-0.1PF 201
- C76A3 12PF 25V NPO-C0G 5% 0201
- C76A4 3.0PF +/-0.1PF 0201
- C76A5 1.8PF +/-0.1PF 201

138 40 38 PPVDD_FABRIC_S1
- 1: C76B0 12PF 25V NPO-C0G 5% 0201
- C76B1 3.0PF +/-0.1PF 0201
- C76B2 1.8PF +/-0.1PF 201
- C76B3 12PF 25V NPO-C0G 5% 0201
- C76B4 3.0PF +/-0.1PF 0201
- C76B5 1.8PF +/-0.1PF 201

138 40 38 PPVDD_DISP_S1
- 2: C76C0 12PF 25V NPO-C0G 5% 0201
- C76C1 3.0PF +/-0.1PF 0201
- C76C2 1.8PF +/-0.1PF 201
- C76C3 12PF 25V NPO-C0G 5% 0201
- C76C4 3.0PF +/-0.1PF 0201
- C76C5 1.8PF +/-0.1PF 201

138 40 38 PP1V8_S2
- 3: C76D0 12PF 25V NPO-C0G 5% 0201
- C76D1 3.0PF +/-0.1PF 0201
- C76D2 1.8PF +/-0.1PF 201

138 40 38 PPVDDQ0_S1
- 4: C76E0 12PF 25V NPO-C0G 5% 0201
- C76E1 3.0PF +/-0.1PF 0201
- C76E2 1.8PF +/-0.1PF 201

138 40 38 PPVDD2H_S2SW
PACK_OPTION=FBUCK5:Y
- 5: C76F0 12PF 25V NPO-C0G 5% 0201
- C76F1 3.0PF +/-0.1PF 0201
- C76F2 1.8PF +/-0.1PF 201
- C76F3 12PF 25V NPO-C0G 5% 0201
- C76F4 3.0PF +/-0.1PF 0201
- C76F5 1.8PF +/-0.1PF 201

138 133 40 38 PPVDD_CIO_S2SW
- 6: C76G0 12PF 25V NPO-C0G 5% 0201
- C76G1 3.0PF +/-0.1PF 0201
- C76G2 1.8PF +/-0.1PF 201

138 40 38 PPVDD_FIXED_S1
- 7: C76H0 12PF 25V NPO-C0G 5% 0201
- C76H1 3.0PF +/-0.1PF 0201
- C76H2 1.8PF +/-0.1PF 201

138 40 39 PP1V2_AWAKE
- 8: C76I0 12PF 25V NPO-C0G 5% 0201
- C76I1 3.0PF +/-0.1PF 0201
- C76I2 1.8PF +/-0.1PF 201

138 40 39 PPVDD_AMPH0_S2SW
- 9: C76J0 12PF 25V NPO-C0G 5% 0201
- C76J1 3.0PF +/-0.1PF 0201
- C76J2 1.8PF +/-0.1PF 201

BOM_COST_GROUP=WIRELESS

PAGE TITLE: PMU OUTPUT DESENSE CAPS

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135	PP1V8_S2	U18	VIN_SW0	VOUT_SW0	U17	PP1V8_S2SW_SNS	37 135
138	PP1V8_S2	V19	VIN_SW1	VOUT_SW1	V20	PP1V8_AWAKE	37 138
138	GND	W19	VIN_SW2	VOUT_SW2	W20	NC_FPMU_SW2	37 138
37	PPVDD_VCP_FPMU (VOLTAGE=5V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000)	Y19	VCP_OUT	VOUT_SW2	Y20		
		AA19	VCP_OUT	VOUT_SW2	AA20		
138	GND	N19	VDD_LDO0	VLDO0	N20	NC_FPMU_LDO0	37 138
138	PP3V8_AON_FPMU	P19	VDD_LDO1	VLDO1	P20	PP1V8_AWAKE_SEPROM_LDO	37 138
35	PP3V8_AON_FPMU	P18	VDD_LDO2	VLDO2	P17	NC_FPMU_LDO2	35 37
135	PP1V8_S2	R18	VDD_LDO3	VLDO3	R17	PP1V2_AWAKESW_BLC	37 135
138 35	PP3V8_AON_FPMU	R19	VDD_LDO4	VLDO4	R20	NC_FPMU_LDO4	35 37 138
138	GND	N18	VDD_LDO5	VLDO5	N17	NC_FPMU_LDO5	37 138
138 136 45 40 39 37 35	PP3V8_AON_FPMU	M9	VDD_MAIN	VLDO9	R16	PP1V8_AON_FPMU (VOLTAGE=1.8V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000)	35 37 141
		L3	VDD_MAIN1				
		L16	VDD_MAIN2	VLDO9B	N16	PP1V2_AON_FPMU (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000)	37
		U15	VDD_MAIN3				
		P15	VDD_MAIN_LDO	VREF_ADC	K9	FPMU_VREFADC (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000)	37
		P16	VDD_MAIN_LDO	VREF	K7	FPMU_VREF (VOLTAGE=1.0V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000)	37
				VLDOINT	N15	PP1V5_LDOINT_FPMU (VOLTAGE=1.5V, MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000)	37
		T17	VDD_RTC_ALT	VLDORTC	T18	NC	
				VLDORTC2	T19	NC	
138 37	PP3V3_AON	P13	VDDIO_3V3	VDD_ANA	C14		
138 37	PP1V8_S2	N10	VDDIO_1V8	VDD_ANA	E8		
138 37	PP1V2_S2	N11	VDDIO_1V2	VDD_ANA	G3		
				VDD_ANA	H16		
				VDD_ANA	L9		
35	PP3V8_AON_FPMU	L8	VDD_MAIN_SNS (1:0001 SYNAPSE_IDentity 1:0001 SYNC_DATE)	VDD_ANA	M4		
		L7	VDD_HI_SNS	VDD_ANA	M17		
				VDD_ANA	R3		
				VDD_ANA	U8		
35	EDP_BKLT_1V29_EN (IN)	T14	LDOX_EN (1V8S2)	VDD_ANA	U16		
				VDD_ANA	W14		
				VDD_ANA	W18		
				VDD_DIG	F14		
				VDD_DIG	G5		
				VDD_DIG	J12		
				VDD_DIG	P5		
				VDD_DIG	U14		

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		VSS_REF	K8
B13	VSS	VSS	J16
C15	VSS	VSS	K2
C16	VSS	VSS	K12
D11	VSS	VSS	K16
D12	VSS	VSS	L4
D14	VSS	VSS	L5
D16	VSS	VSS	M3
E3	VSS	VSS	M16
E4	VSS	VSS	M18
E5	VSS	VSS	N3
E6	VSS	VSS	N14
E7	VSS	VSS	P3
E9	VSS	VSS	P10
E10	VSS	VSS	P14
E12	VSS	VSS	R4
E13	VSS	VSS	R5
E14	VSS	VSS	R15
E16	VSS	VSS	T3
F3	VSS	VSS	T16
F6	VSS	VSS	U3
F7	VSS	VSS	U4
F15	VSS	VSS	U5
F16	VSS	VSS	U6
G4	VSS	VSS	U7
G12	VSS	VSS	U9
G15	VSS	VSS	U19
G16	VSS	VSS	V11
H11	VSS	VSS	V12
H14	VSS	VSS	V14
H15	VSS	VSS	V16
J3	VSS	VSS	V18
J4	VSS	VSS	W16
J15	VSS	VSS	Y13

XW77A0
SHORT-20L-0.1MM-SM
1 2
GND_VSS_REF_FPMU (MAKE_BASE=TRUE, VOLTAGE=0V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.1000) 37

PP3V8_AON_FPMU 35 37 39 40 45 136

C7700	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.M9:5MM
C7701	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.L3:5MM
C7702	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.L16:5MM
C7703	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.U15:5MM
C7704	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.P15:5MM

PPVDD_VCP_FPMU 37

PP3V3_AON 37 138
PP1V8_S2 37 138
PP1V2_S2 37 138

C7720	0.1UF 10% 25V X6S-CERM 0201	
C7710	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.P13:5MM
C7711	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.N10:5MM
C7712	0.1UF 10% 25V X6S-CERM 0201	PLACE_NEAR=U7700.N11:5MM

PP1V8_S2SW_SNS 37 135
PP1V8_AWAKE 37 138
NC_FPMU_SW2 37 138

C7790	2.2UF 20% 4V X6S-CERM 0201	PACK_OPTION=FPMU_SW0
C7792	2.2UF 20% 4V X6S-CERM 0201	
C7794	2.2UF 20% 4V X6S-CERM 0201	PACK_IGNORE=TRUE PACK_OPTION=FPMU_SW2

NC_FPMU_LDO0 37 138
PP1V8_AWAKE_SEPROM_LDO 37 138
NC_FPMU_LDO2 35 37

C7760	10UF 20% 6.3V CER-X6S 0402	PACK_IGNORE=TRUE PACK_OPTION=FPMU_LDO0
C7762	10UF 20% 6.3V CER-X6S 0402	
C7764	10UF 20% 6.3V CER-X6S 0402	PACK_IGNORE=TRUE PACK_OPTION=FPMU_LDO2
C7765	10UF 20% 6.3V CER-X6S 0402	

PP1V2_AWAKESW_BLC 37 135
NC_FPMU_LDO4 35 37 138
NC_FPMU_LDO5 37 138

C7766	10UF 20% 6.3V CER-X6S 0402	PACK_OPTION=FPMU_LDO3
C7768	10UF 20% 6.3V CER-X6S 0402	PACK_IGNORE=TRUE PACK_OPTION=FPMU_LDO4
C776A	10UF 20% 6.3V CER-X6S 0402	PACK_IGNORE=TRUE PACK_OPTION=FPMU_LDO5

PP1V8_AON_FPMU 35 37 141
PP1V2_AON_FPMU 37
FPMU_VREFADC 37
FPMU_VREF 37
PP1V5_LDOINT_FPMU 37

C7770	4.7UF 20% 6.3V CER 0402	
C7772	4.7UF 20% 6.3V CER 0402	
C7774	0.22UF 10% 10V X6S 0201	
C7776	2.2UF 10% 10V X6S-CERM 0402-0.1MM	
C7778	20UF 20% 2.5V X6S-CERM 0402	PLACE_NEAR=U7700.N15:5MM

GND_VSS_REF_FPMU 37

PP1V5_LDOINT_FPMU 37

C7780	0.1UF 10% 25V X6S-CERM 0201	
C7781	0.1UF 10% 25V X6S-CERM 0201	
C7782	0.1UF 10% 25V X6S-CERM 0201	
C7783	0.1UF 10% 25V X6S-CERM 0201	
C7784	0.1UF 10% 25V X6S-CERM 0201	
C7785	0.1UF 10% 25V X6S-CERM 0201	
C7786	0.1UF 10% 25V X6S-CERM 0201	
C7787	0.1UF 10% 25V X6S-CERM 0201	

Distribute these caps under VDD_ANA and VDD_DIG pins

BOM_COST_GROUP=SOC POWER

PAGE TITLE
FPMU VIN/LDO/SW/GND

Apple Inc.

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OMIT_TABLE

U7700
CHAPEL-PMU
WLCSP
SYM 2 OF 6

L7800
1.0UH-20%-4A-0.034OHM
PIKD20161B
CRITICAL
152S01283

PPVDD_DCS_S1 (138 40 36) → PP7800 → FPMU_BUCK0_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) → A15 / B15 → BUCK0_LX0

L7801
0.1UH-20%-10.3A-0.01OHM
PCCE20161B-SM
CRITICAL
OMIT_TABLE
152S01268

PP7801 → FPMU_BUCK0_LX1 (SWITCH_NODE=TRUE, DIDT=TRUE) → C17 / C18 / C19 / C20 → BUCK0_LX1

PP7803 → FPMU_BUCK0_LX3 (SWITCH_NODE=TRUE, DIDT=TRUE) → E17 / E18 / E19 / E20 → BUCK0_LX3

L7802
0.1UH-20%-10.3A-0.01OHM
PCCE20161B-SM
CRITICAL
152S01268

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK0_5PH

PP7802 (X) → PP7804 (X) → FPMU_BUCK0_LX2 (SWITCH_NODE=TRUE, DIDT=TRUE) → G17 / G18 / G19 / G20 → BUCK0_LX2

FPMU_BUCK0_LX4 (SWITCH_NODE=TRUE, DIDT=TRUE) → J17 / J18 / J19 / J20 → BUCK0_LX4

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7800
SHORT-20L-0.1MM-SM

PPVDD_DCS_S1 (138) → FPMU_BUCK0_FB_R → R7800 0 TK 0201 0% 1/20W → FPMU_BUCK0_FB → D15 / E15 → BUCK0_FB / BUCK0_VSS_FB

<--- Length Match FB traces --->

XW7801
SHORT-20L-0.1MM-SM
NO_XNET_CONNECTION=1
PLACE_NEAR=U0600:10MM

L7810
1.0UH-20%-4A-0.034OHM
PIKD20161B
CRITICAL
152S01283

PPVDD_FABRIC_S1 (138 40 36) → PP7810 → FPMU_BUCK1_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) → T1 / T2 → BUCK1_LX0

L7811
0.1UH-20%-10.3A-0.01OHM
PCCE20161B-SM
CRITICAL
OMIT_TABLE
152S01268

PP7811 → FPMU_BUCK1_LX1 (SWITCH_NODE=TRUE, DIDT=TRUE) → V3 / W3 / Y3 / AA3 → BUCK1_LX1

PP7813 → FPMU_BUCK1_LX3 (SWITCH_NODE=TRUE, DIDT=TRUE) → V5 / W5 / Y5 / AA5 → BUCK1_LX3

L7812
0.1UH-20%-10.3A-0.01OHM
PCCE20161B-SM
CRITICAL
OMIT_TABLE
152S01268

PP7812 → FPMU_BUCK1_LX2 (SWITCH_NODE=TRUE, DIDT=TRUE) → V7 / W7 / Y7 / AA7 → BUCK1_LX2

PP7814 → FPMU_BUCK1_LX4 (SWITCH_NODE=TRUE, DIDT=TRUE) → V9 / W9 / Y9 / AA9 → BUCK1_LX4

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7810
SHORT-20L-0.1MM-SM

PPVDD_FABRIC_S1 (138) → FPMU_BUCK1_FB_R → R7810 0 TK 0201 0% 1/20W → FPMU_BUCK1_FB → T4 / T5 → BUCK1_FB / BUCK1_VSS_FB

L7820
1.0UH-20%-4A-0.034OHM
PIKD20161B
CRITICAL
152S01283

PPVDD_DISP_S1 (138 40 36) → PP7820 → FPMU_BUCK2_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) → F1 / F2 → BUCK2_LX0

L7821
0.15UH-20%-8.8A-0.015OHM
PIIA20161B
CRITICAL
152S00887

PP7821 → FPMU_BUCK2_LX1 (SWITCH_NODE=TRUE, DIDT=TRUE) → A3 / B3 / C3 / D3 → BUCK2_LX1

NC A5 / NC B5 / NC C5 / NC D5 → BUCK2_LX3

L7822
0.1UH-20%-10.3A-0.01OHM
PCCE20161B-SM
CRITICAL
OMIT_TABLE
152S01268

PP7822 → FPMU_BUCK2_LX2 (SWITCH_NODE=TRUE, DIDT=TRUE) → A7 / B7 / C7 / D7 → BUCK2_LX2

PP7824 → FPMU_BUCK2_LX4 (SWITCH_NODE=TRUE, DIDT=TRUE) → A9 / B9 / C9 / D9 → BUCK2_LX4

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7820
SHORT-20L-0.1MM-SM

PPVDD_DISP_S1 (138) → FPMU_BUCK2_FB_R → R7820 0 TK 0201 0% 1/20W → FPMU_BUCK2_FB → F4 / F5 → BUCK2_FB / BUCK2_VSS_FB

L7830
0.47UH-20%-6.9A-0.022OHM
MEMK2520-SM
CRITICAL
152S01325

BUCK3_LX ← Y17 / AA17 ← FPMU_BUCK3_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7830 → PP1V8_S2 (36 40 138)

PLACE_NEAR=C8030:3MM
NO_XNET_CONNECTION=1
XW7830
SHORT-20L-0.1MM-SM

BUCK3_FB ← V17 ← FPMU_BUCK3_FB_R ← R7830 0 TK 0201 0% 1/20W ← FPMU_BUCK3_FB ← W17 / BUCK3_VSS_FB

L7840
1.0UH-20%-4A-0.034OHM
PIKD20161B
CRITICAL
152S01283

BUCK4_LX0 ← A13 ← FPMU_BUCK4_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7840 → PPVDDQ0_S1 (36 40 138)

L7841
0.22UH-20%-6.7A-0.023OHM
PINA201T-SM
CRITICAL
152S00204

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK4_2PH

BUCK4_LX1 ← A11 / B11 / C11 ← FPMU_BUCK4_LX1 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7841 (X)

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7840
SHORT-20L-0.1MM-SM

BUCK4_FB ← D13 ← FPMU_BUCK4_FB_R ← R7840 0 TK 0201 0% 1/20W ← FPMU_BUCK4_FB ← C13 / BUCK4_VSS_FB

L7850
1.0UH-20%-4A-0.034OHM
PIKD20161B
CRITICAL
152S01283

BUCK5_LX0 ← K1 ← FPMU_BUCK5_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7850 → PPVDD2H_S2SW (36 40 138)

PACK_OPTION=FBUCK5:Y

L7851
0.1UH-20%-10.3A-0.01OHM
PCCE20161B-SM
CRITICAL
OMIT_TABLE
152S01268

BUCK5_LX1 ← M1 / M2 ← FPMU_BUCK5_LX1 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7851

BUCK5_LX2 ← P1 / P2 ← FPMU_BUCK5_LX2 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7852

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7850
SHORT-20L-0.1MM-SM

BUCK5_FB ← K4 ← FPMU_BUCK5_FB_R ← R7850 0 TK 0201 0% 1/20W ← FPMU_BUCK5_FB ← K3 / BUCK5_VSS_FB

MAKE_BASE=TRUE
PACK_OPTION=FBUCK5:N

L7860
1.0UH-20%-4A-0.034OHM
PIKD20161B
CRITICAL
152S01283

BUCK6_LX0 ← AA13 ← FPMU_BUCK6_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7860 → PPVDD_CIO_S2SW (36 40 133 138)

L7861
0.22UH-20%-6.7A-0.023OHM
PINA201T-SM
CRITICAL
152S00204

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK6_2PH

BUCK6_LX1 ← W11 / Y11 / AA11 ← FPMU_BUCK6_LX1 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7861 (X)

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7860
SHORT-20L-0.1MM-SM

BUCK6_FB ← V13 ← FPMU_BUCK6_FB_R ← R7860 0 TK 0201 0% 1/20W ← FPMU_BUCK6_FB ← W13 / BUCK6_VSS_FB

L7870
0.47UH-20%-6.9A-0.022OHM
MEMK2520-SM
CRITICAL
152S01325

BUCK7_LX ← Y15 / AA15 ← FPMU_BUCK7_LX0 (SWITCH_NODE=TRUE, DIDT=TRUE) ← PP7870 → PPVDD_FIXED_S1 (36 40 138)

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7870
SHORT-20L-0.1MM-SM

BUCK7_FB ← V15 ← FPMU_BUCK7_FB_R ← R7870 0 TK 0201 0% 1/20W ← FPMU_BUCK7_FB ← W15 / BUCK7_VSS_FB

BOM_COST_GROUP=SOC POWER

PAGE TITLE: FPMU BUCKS 0-7

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DRAWING NUMBER: 051-08242 | SIZE: D
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(Pin Notes) are based on OTP version xPD: https://seg-docs.csg.apple.com/projects/chapel/release/OTP/A0/
[Pin Notes] are based on iBoot overrides: rdar://96232826

GPIO without (OTP notes) are Input/PD/1V8AON
GPIO without [iBoot overrides notes] are left in their OTP config
GPIO that are unused (NC) in a given project are left in their OTP config

OMIT_TABLE

U7700
CHAPEL-PMU
WLCSP

SYM 4 OF 6

66	PCPU_ISENSE	G8	AMUX_A<0>	GPIO1	H12	NC_FPMU_GPIO1	35
66	GPU_ISENSE	F13	AMUX_A<1>	GPIO2	J11	NC_FPMU_GPIO2	35
66	P3V8AON_HS_ISENSE	G7	AMUX_A<2>	GPIO3	H13	NC_FPMU_GPIO3	35
66	WLBT_3V8_ISENSE	F12	AMUX_A<3>	GPIO4	J13	NC_FPMU_GPIO4	35
66	SPKRAMP_DEF_ISENSE	G6	AMUX_A<4>	GPIO5	J14	NC_FPMU_GPIO5	35
66	FPMU_3V8_ISENSE	F11	AMUX_A<5>	GPIO6	K15	NC_FPMU_GPIO6	35
66	FAN1_P5VS2_ISENSE	F8	AMUX_A<6>	GPIO7	K14	NC_FPMU_GPIO7	35
66	PCPU_SRAM_ISENSE	F10	AMUX_A<7>	GPIO8	K13	NC_FPMU_GPIO8	35
35	NC_FPMU_AMUX_AY	J9	AMUX_AY	GPIO9	L13	NC_FPMU_GPIO9	35
66	USB01_3V8_ISENSE	G9	AMUX_B<0>	GPIO10	L14	NC_FPMU_GPIO10	35
66	GPU_VSENSE	F9	AMUX_B<1>	GPIO11	M15	NC_FPMU_GPIO11	35
66	P5VUSB01_HS_ISENSE	G10	AMUX_B<2>	GPIO12	M14	NC_HDMI_CECFET_EN	OUT 141
66	TCON_3V8_ISENSE	G11	AMUX_B<3>	GPIO13	M13	NC_FPMU_GPIO13	35
66	BKLT_HS_ISENSE	G13	AMUX_B<4>	GPIO14	M12	NC_FPMU_GPIO14	OUT 35
66	SD_HS_ISENSE	G14	AMUX_B<5>	GPIO15	M7	NC_FPMU_GPIO15	35
66	ALSCAM_5V_ISENSE	H10	AMUX_B<6>	GPIO16	M6	NC_FPMU_GPIO16	35
66	BKLTCONN_3V8_ISENSE	H9	AMUX_B<7>	GPIO17	M5	NC_FPMU_GPIO17	35
35	NC_FPMU_AMUX_BY	J7	AMUX_BY	GPIO18	N4	NC_FPMU_GPIO18	35
				GPIO19	P4	NC_FPMU_GPIO19	35
66	GPU_PH5_THMSNS	H5	TDEV1	GPIO20	P6	NC_FPMU_GPIO20	35
66	AIRFLOW_C_THMSNS	H6	TDEV2	GPIO21	N6	NC_FPMU_GPIO21	35
66	FINSTACK_R_THMSNS	H7	TDEV3	GPIO22	N7	NC_FPMU_GPIO22	35
66	FINSTACK_L_THMSNS	J5	TDEV4	GPIO23	N8	NC_FPMU_GPIO23	35
66	PCPU_PH5_THMSNS	K5	TDEV5	GPIO24	N9	NC_FPMU_GPIO24	35
66	GPU_PH6_THMSNS	H8	TDEV6	(3V3AON/OD) GPIO25	N12	IPD_TOUCH_RESET_L	OUT 123
66	FPMU_THMSNS	J6	TDEV7	(3V3AON/OD) GPIO26	N13	IPD_MCU_RESET_L	OUT 123
66	WLBT_THMSNS	J8	TDEV8	GPIO27	L15	NC_FPMU_GPIO27	35
39	FPMU_TCAL	K6	TCAL	SLEEP_32K	R6	NC_FPMU_SLEEP_32K	
				OUT_32K_0	P8	NC_FPMU_OUT_32K_0	
				OUT_32K_1	P9	NC_FPMU_OUT_32K_1	
	NC_FPMU_BUTTON1	P12	BUTTON1	DBLCLICK_DET	U12	NC_FPMU_DBLCLICK_DET	
	NC_FPMU_BUTTON2	P11	BUTTON2				
	NC_FPMU_RESET_IN0	T9	RESET_IN0	FAULT_OUT_L	T13	NC_FPMU_FAULT_OUT_L	
	NC_FPMU_RESET_IN1	T8	RESET_IN1	(1V2AON) CRASH0_L	T12	FPMU_CRASH0_L	BI 35 129
	NC_FPMU_RESET_IN2	T7	RESET_IN2	(1V8AON) CRASH1_L	R11	FPMU_CRASH1_L	IN 35 129
	NC_FPMU_RESET_IN3	T6	RESET_IN3	CRASH2_L	R10	NC_FPMU_CRASH2_L	
	NC_FPMU_SHDN	U10	SHDN	OFF_REQ	N5	NC_FPMU_OFF_REQ	
	NC_FPMU_PSU_12V_PGOOD	T11	PSU_P12V_PGOOD	WAKE2LF	R12	NC_FPMU_WAKE2LF	
				ACTIVE_READY	U13	NC_FPMU_ACTIVE_READY	
50 47 43	IN SGPIO_READY_REQ	R14	SGPIO_READY_REQ (1V2AON)	SYS_ALIVE	R13	NC_FPMU_SYS_ALIVE	
35	BI SGPIO_FPMU_DATA	L11	SGPIO_SDATA (1V2AON)	RESET_L	T10	NC_FPMU_RESET_L	
35	IN SGPIO_FPMU_CLK	M11	SGPIO_SCLK_0 (1V2AON)	FORCE_DFU	P7	NC_FPMU_FORCE_DFU	
	NC_FPMU_SGPIO_SCLK_1	M10	SGPIO_SCLK_1				
12	IN SPMI_FPMU_CLK	K11	SPMI_SCLK (1V2S2)	(1V2S2/OD) THROTTLE0_L	R9	FABRIC_ILIMIT_L	OUT 5
12	BI SPMI_FPMU_DATA	L12	SPMI_SDATA (1V2S2)	THROTTLE1_L	R8	NC_FPMU_THROTTLE1_L	
12	IN SWD_FPMU_SWDIO	M8	SWD_TMS (1V2S2)	THROTTLE2_L	R7	NC_FPMU_THROTTLE2_L	
12	IN SWD_FPMU_SWCLK	L10	DFT_CTRL1 (1V2S2)	UVWARN_L	U11	NC_FPMU_UVWARN_L	
				VPP	E11	GND	39
	T15		CFG_EXT_CLK	CFG_OTP	L6	GND	39
	T20		XOUT	DFT_CTRL0	K10		
	U20		XIN	DFT_CTRL2	J10	GND	39

HDMI CEC FET is planned to be deprecated
Its parts are NOSTUFF and bypassed, and this IO is not configured

138 136 45 40 37 35 PP3V8_AON_FPMU

R7972 1 2 10K NOSTUFF
PACK_IGNORE=TRUE 5% 1/20W 0201 TK
PACK_OPTION=PMU_CFGOTP:R

39 GND

R7971 1 2 10K
PACK_IGNORE=TRUE 5% 1/20W 0201 TK
PACK_OPTION=PMU_CFGOTP:R

PACK_OPTION=PMU_CFGOTP:GND MAKE_BASE=TRUE

39 GND

R7970 1 2 10K
PACK_IGNORE=TRUE 5% 1/20W 0201 TK
PACK_OPTION=VPP:R

PACK_OPTION=VPP:GND MAKE_BASE=TRUE

39 GND

R7973 1 2 10K
PACK_IGNORE=TRUE 5% 1/20W 0201 TK
PACK_OPTION=VPP:R

PACK_OPTION=VPP:GND MAKE_BASE=TRUE

FPMU_TCAL 39

103S00584
R7911
3.92K
0.1% 1/20W TK 0201

131S0805
C7911
100PF
5% 25V C0G 0201

OMIT_TABLE

U7700
CHAPEL-PMU
WLCSP

SYM 3 OF 6

L19 FPMU_BUCK8_LX0
BUCK8_LX L20
SWITCH_NODE=TRUE
DIDT=TRUE

PP7980 SM P4MM 1

L7980
0.47UH-20%-6.9A-0.022OHM
1 2
MEMK2520-SM
CRITICAL
152S01325

PP1V2_AWAKE 36 40 138

PLACE_NEAR=C8080:3MM
NO_XNET_CONNECTION=1
XW7980
SHORT-20L-0.1MM-SM

R7980
0
TK 0201 0% 1/20W

BUCK8_FB L17 FPMU_BUCK8_FB
BUCK8_VSS_FB L18

FPMU_BUCK8_FB_R

PP1V2_AWAKE 138

L19 FPMU_BUCK8_LX0
BUCK8_LX L20
SWITCH_NODE=TRUE
DIDT=TRUE

PP7990 SM P4MM 1

L7990
0.47UH-20%-6.9A-0.022OHM
1 2
MEMK2520-SM
CRITICAL
152S01325

PPVDD_AMPH0_S2SW 36 40 138

PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
XW7990
SHORT-20L-0.1MM-SM

R7990
0
TK 0201 0% 1/20W

BUCK9_FB H4 FPMU_BUCK9_FB
BUCK9_VSS_FB H3

FPMU_BUCK9_FB_R

PPVDD_AMPH0_S2SW 138

BOM_COST_GROUP=SOC POWER

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FPMU GPIO & BUCKS 8-9

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OMIT_TABLE

U7700
CHAPEL-PMU
WLCSP

SYM 1 OF 6

BUCK2

A1 B1 C1 D1 — VSS_BUCK2
A2 B2 C2 D2 — VDD_BUCK0_2_4_8_9
PH1
A4 B4 C4 D4 — VSS_BUCK2
PH3
A6 B6 C6 D6 — VDD_BUCK0_2_4_8_9
PH2
A8 B8 C8 D8 — VSS_BUCK2
PH4
A10 B10 C10 D10 — VDD_BUCK0_2_4_8_9
PH1
A12 B12 C12 — VSS_BUCK4
PH0
A14 B14 — VDD_BUCK0_2_4_8_9
PH0
A16 B16 — VSS_BUCK0
A17 A18 A19 A20 — VSS_BUCK0
B17 B18 B19 B20 — VDD_BUCK0_2_4_8_9
PH1
D17 D18 D19 D20 — VSS_BUCK0
PH3
F17 F18 F19 F20 — VDD_BUCK0_2_4_8_9
PH2
H17 H18 H19 H20 — VSS_BUCK0
PH4
K17 K18 K19 K20 — VDD_BUCK0_2_4_8_9
PH0
M19 M20 — VSS_BUCK8

C80AA 2.2UF 20% 6.3V X6S 0201
C80A0 1UF 20% 6.3V X6S-CERM 0201
C80AC 2.2UF 20% 6.3V X6S 0201
C80A2 1UF 20% 6.3V X6S-CERM 0201
C80AD 2.2UF 20% 6.3V X6S 0201
C80A3 1UF 20% 6.3V X6S-CERM 0201
C80AE 2.2UF 20% 6.3V X6S 0201
C80A4 1UF 20% 6.3V X6S-CERM 0201
C80AF 2.2UF 20% 6.3V X6S 0201
C80A5 1UF 20% 6.3V X6S-CERM 0201
C80AG 2.2UF 20% 6.3V X6S 0201
C80A6 1UF 20% 6.3V X6S-CERM 0201
C80BA 2.2UF 20% 6.3V X6S 0201
C80B0 1UF 20% 6.3V X6S-CERM 0201
C80BB 2.2UF 20% 6.3V X6S 0201
C80B1 1UF 20% 6.3V X6S-CERM 0201
C80BC 2.2UF 20% 6.3V X6S 0201
C80B2 1UF 20% 6.3V X6S-CERM 0201
C80BD 2.2UF 20% 6.3V X6S 0201
C80B3 1UF 20% 6.3V X6S-CERM 0201
C80BE 2.2UF 20% 6.3V X6S 0201
C80B4 1UF 20% 6.3V X6S-CERM 0201

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK4_2PH

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK0_5PH

Place 0201 VDD+BUCK caps surrounding PMU near relevant pins

VSS_BUCK2 — E1 E2 — PH0
VDD_BUCK0_2_4_8_9 — G1 G2 — BUCK9 — PH0
VSS_BUCK9_5 — J1 J2 — BUCK5 — PH0
VDD_BUCK1_5_6_7 — L1 L2 — PH1
VSS_BUCK9_5 — N1 N2 — PH2
VDD_BUCK1_5_6_7 — R1 R2 — BUCK1 — PH0
VSS_BUCK1 — U1 U2

C80C0 1UF 20% 6.3V X6S-CERM 0201
C80CA 2.2UF 20% 6.3V X6S 0201
C80C1 1UF 20% 6.3V X6S-CERM 0201
C80CB 2.2UF 20% 6.3V X6S 0201
C80C2 1UF 20% 6.3V X6S-CERM 0201
C80CC 2.2UF 20% 6.3V X6S 0201
C80C3 1UF 20% 6.3V X6S-CERM 0201
C80CD 2.2UF 20% 6.3V X6S 0201
C80C4 1UF 20% 6.3V X6S-CERM 0201
C80CE 2.2UF 20% 6.3V X6S 0201
C80C5 1UF 20% 6.3V X6S-CERM 0201
C80CF 2.2UF 20% 6.3V X6S 0201

PACK_OPTION=FBUCK5:Y

VSS_BUCK1 — V1 W1 Y1 AA1 — VDD_BUCK1_5_6_7 — V2 W2 Y2 AA2 — PH1
VSS_BUCK1 — V4 W4 Y4 AA4 — PH3
VDD_BUCK1_5_6_7 — V6 W6 Y6 AA6 — PH2
VSS_BUCK1 — V8 W8 Y8 AA8 — PH4
VDD_BUCK1_5_6_7 — V10 W10 Y10 AA10 — BUCK6 — PH1
VSS_BUCK6 — W12 Y12 AA12 — PH0
VDD_BUCK1_5_6_7 — Y14 AA14 — BUCK7 — PH0
VSS_BUCK3_7 — Y16 AA16 — BUCK3 — PH0
VDD_BUCK3 — Y18 AA18

C80D0 1UF 20% 6.3V X6S-CERM 0201
C80DA 2.2UF 20% 6.3V X6S 0201
C80D1 1UF 20% 6.3V X6S-CERM 0201
C80DB 2.2UF 20% 6.3V X6S 0201
C80D2 1UF 20% 6.3V X6S-CERM 0201
C80DC 2.2UF 20% 6.3V X6S 0201
C80D3 1UF 20% 6.3V X6S-CERM 0201
C80DD 2.2UF 20% 6.3V X6S 0201
C80D4 1UF 20% 6.3V X6S-CERM 0201
C80DE 2.2UF 20% 6.3V X6S 0201
C80D5 1UF 20% 6.3V X6S-CERM 0201
C80DF 2.2UF 20% 6.3V X6S 0201
C80D6 1UF 20% 6.3V X6S-CERM 0201
C80DG 2.2UF 20% 6.3V X6S 0201
C80D7 1UF 20% 6.3V X6S-CERM 0201
C80DH 2.2UF 20% 6.3V X6S 0201

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK6_2PH

PP3V8_AON_FPMU 35 37 39 45 136 138

C80F0 C80F1 C80F2 C80F3 C80F4 C80F5 C80F6 C80F7 C80F8 C80F9
C80FA C80FB C80FC C80FD C80FE C80FF C80FG C80FH C80FI
10UF 20% 6.3V CERM-X6S 0402

C5895 150uF
This cap is drawn on ref_vr_iceman_hp CSA58
Place near FPMU's input Rsns

Place 0402 VDD_BUCK caps on opposite side of PMU

Buck Output Caps (near PMU)

1x 2.2uF 0402 per inductor, rounded up to even number to mirror
2x 0201 per CL pair
More 0402 caps on Bucks that serve system loads, for local bulk/FB

138 38 36 PPVDD_DCS_S1

0
C8000 2.2UF 10% 10V X6S-CERM 0402
C8001 2.2UF 10% 10V X6S-CERM 0402
C8002 2.2UF 10% 10V X6S-CERM 0402
C8003 2.2UF 10% 10V X6S-CERM 0402
C8004 0.22UF 20% 6.3V X6S-CERM 0201
C8005 0.22UF 20% 6.3V X6S-CERM 0201
C8006 0.22UF 20% 6.3V X6S-CERM 0201
C8007 0.22UF 20% 6.3V X6S-CERM 0201

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK0_5PH

PACK_IGNORE=TRUE
PACK_OPTION=FBUCK0_5PH

138 38 36 PPVDD_FABRIC_S1

1
C8010 2.2UF 10% 10V X6S-CERM 0402
C8011 2.2UF 10% 10V X6S-CERM 0402
C8012 2.2UF 10% 10V X6S-CERM 0402
C8013 2.2UF 10% 10V X6S-CERM 0402
C8014 0.22UF 20% 6.3V X6S-CERM 0201
C8015 0.22UF 20% 6.3V X6S-CERM 0201
C8016 0.22UF 20% 6.3V X6S-CERM 0201
C8017 0.22UF 20% 6.3V X6S-CERM 0201

138 38 36 PPVDD_DISP_S1

2
C8020 2.2UF 10% 10V X6S-CERM 0402
C8021 2.2UF 10% 10V X6S-CERM 0402
C8022 2.2UF 10% 10V X6S-CERM 0402
C8023 2.2UF 10% 10V X6S-CERM 0402
C8024 0.22UF 20% 6.3V X6S-CERM 0201
C8025 0.22UF 20% 6.3V X6S-CERM 0201

138 38 36 PP1V8_S2

NOSTUFF

3
C8030 2.2UF 10% 10V X6S-CERM 0402
C8031 2.2UF 10% 10V X6S-CERM 0402
C8034 20UF 20% 2.5V X6S 0402-3
C8035 20UF 20% 2.5V X6S 0402-3
C8036 20UF 20% 2.5V X6S 0402-3
C8037 20UF 20% 2.5V X6S 0402-3
C8038 20UF 20% 2.5V X6S 0402-3
C8039 20UF 20% 2.5V X6S 0402-3

BOMSWAP=138800035

138 38 36 PPVDDQ0_S1

4
C8040 2.2UF 10% 10V X6S-CERM 0402
C8041 2.2UF 10% 10V X6S-CERM 0402

138 38 36 PPVDD2H_S2SW

5
C8050 2.2UF 10% 10V X6S-CERM 0402
C8051 2.2UF 10% 10V X6S-CERM 0402
C8054 0.22UF 20% 6.3V X6S-CERM 0201
C8055 0.22UF 20% 6.3V X6S-CERM 0201

PACK_OPTION=FBUCK5:Y

138 133 38 36 PPVDD_CIO_S2SW

6
C8060 2.2UF 10% 10V X6S-CERM 0402
C8061 2.2UF 10% 10V X6S-CERM 0402

138 38 36 PPVDD_FIXED_S1

7
C8070 2.2UF 10% 10V X6S-CERM 0402
C8071 2.2UF 10% 10V X6S-CERM 0402

138 39 36 PP1V2_AWAKE

8
C8080 2.2UF 10% 10V X6S-CERM 0402
C8081 2.2UF 10% 10V X6S-CERM 0402
C8084 15UF 20% 2.5V X6S 0402-4
C8085 15UF 20% 2.5V X6S 0402-4
C8086 15UF 20% 2.5V X6S 0402-4
C8087 15UF 20% 2.5V X6S 0402-4
C8088 15UF 20% 2.5V X6S 0402-4
C8089 15UF 20% 2.5V X6S 0402-4

BOMSWAP=138800392

138 39 36 PPVDD_AMPH0_S2SW

9
C8090 2.2UF 10% 10V X6S-CERM 0402
C8091 2.2UF 10% 10V X6S-CERM 0402

1x 10uF input per inductor

Place under LX pins of each single-inductor phase
Place under shared VSS_BUCK pins of each CL-inductor pair

BOM_COST_GROUP=SOC POWER

PAGE TITLE
FPMU BUCK IN/OUT CAPS

Apple Inc.

DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
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SHEET 40 OF 156

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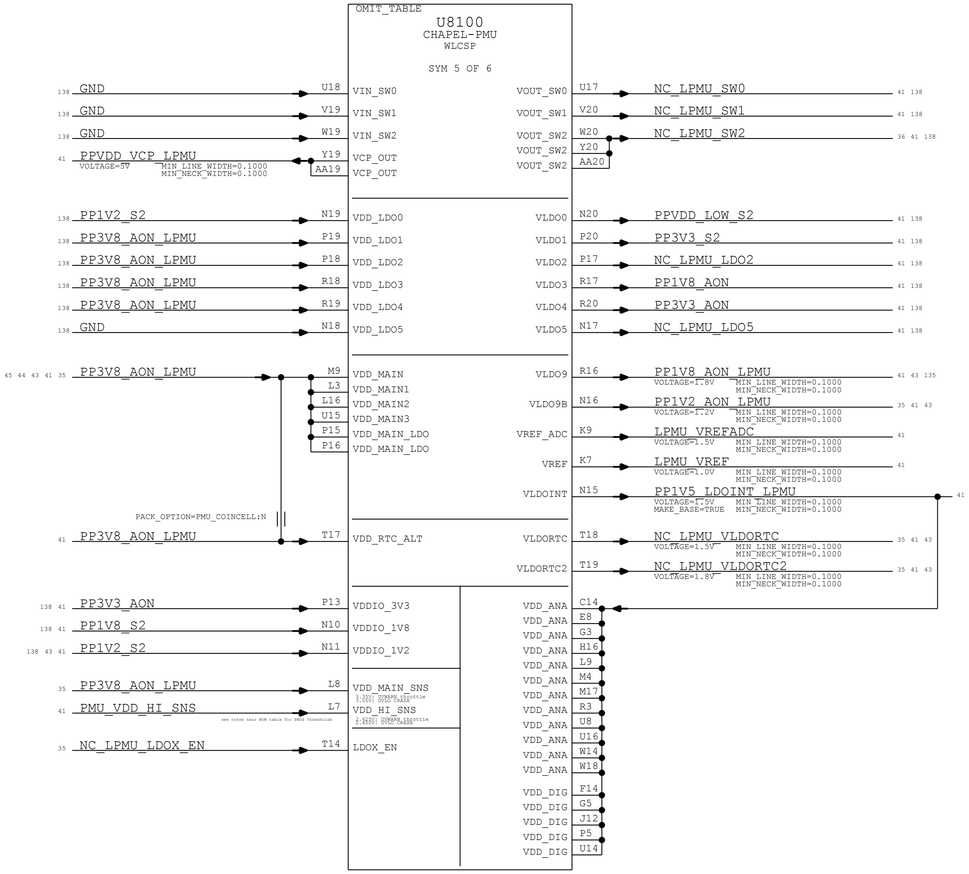

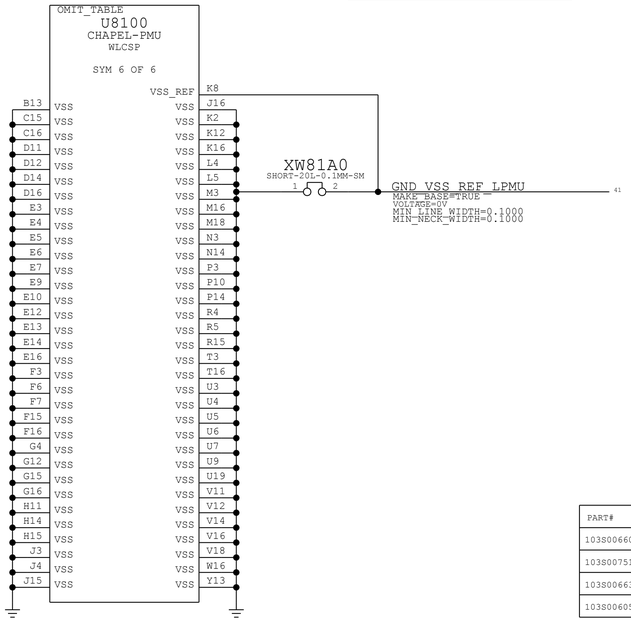

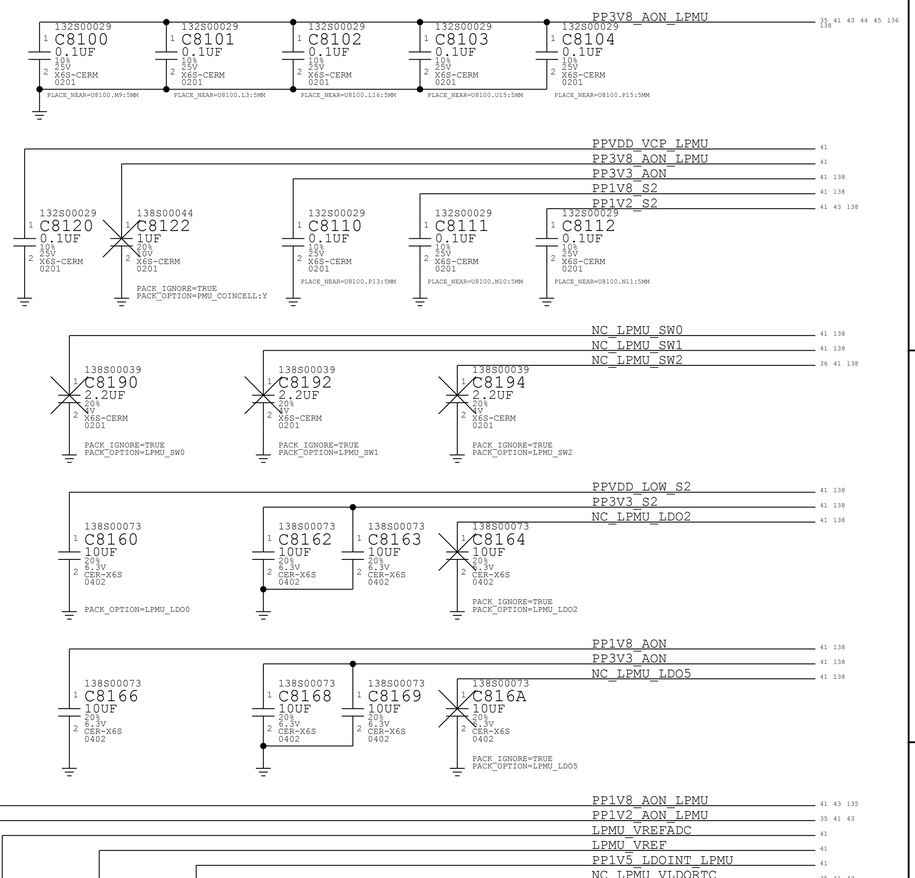

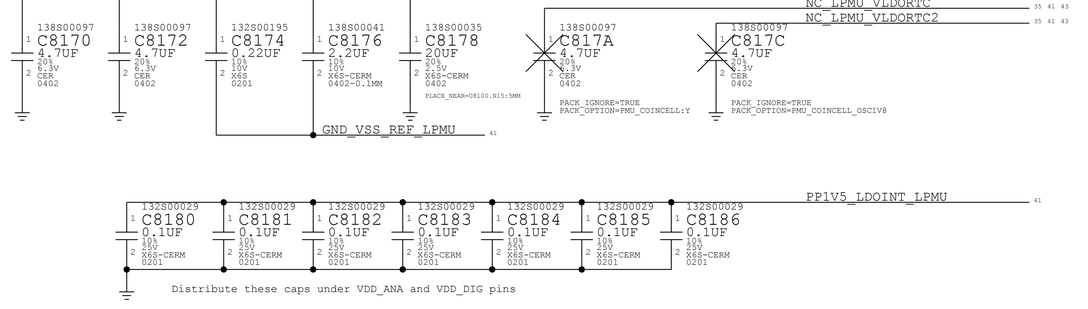

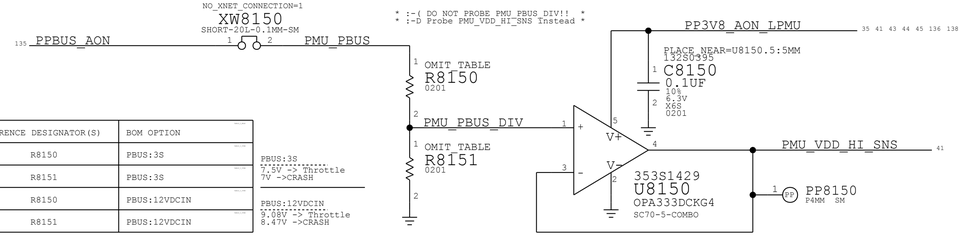

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
103S00660	1	RES,0201,0.1%,1/16W,1.07M	R8150	PBUS:3S
103S00751	1	RES,0201,0.1%,1/16W,576K	R8151	PBUS:3S
103S00663	1	RES,0201,0.1%,1/16W,715K	R8150	PBUS:12VDCIN
103S00605	1	RES,0201,0.1%,1/16W,291K	R8151	PBUS:12VDCIN

PBUS:3S
7.5V -> Throttle
7V ->CRASH

PBUS:12VDCIN
9.18V -> Throttle
8.47V ->CRASH

BOM_COST_GROUP=SOC POWER

PAGE TITLE
LPMU VIN/LDO/SW/GND

Apple Inc.

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DRAWING NUMBER	051-08242
SIZE	D
REVISION	4.0.0
BRANCH	dvt-2
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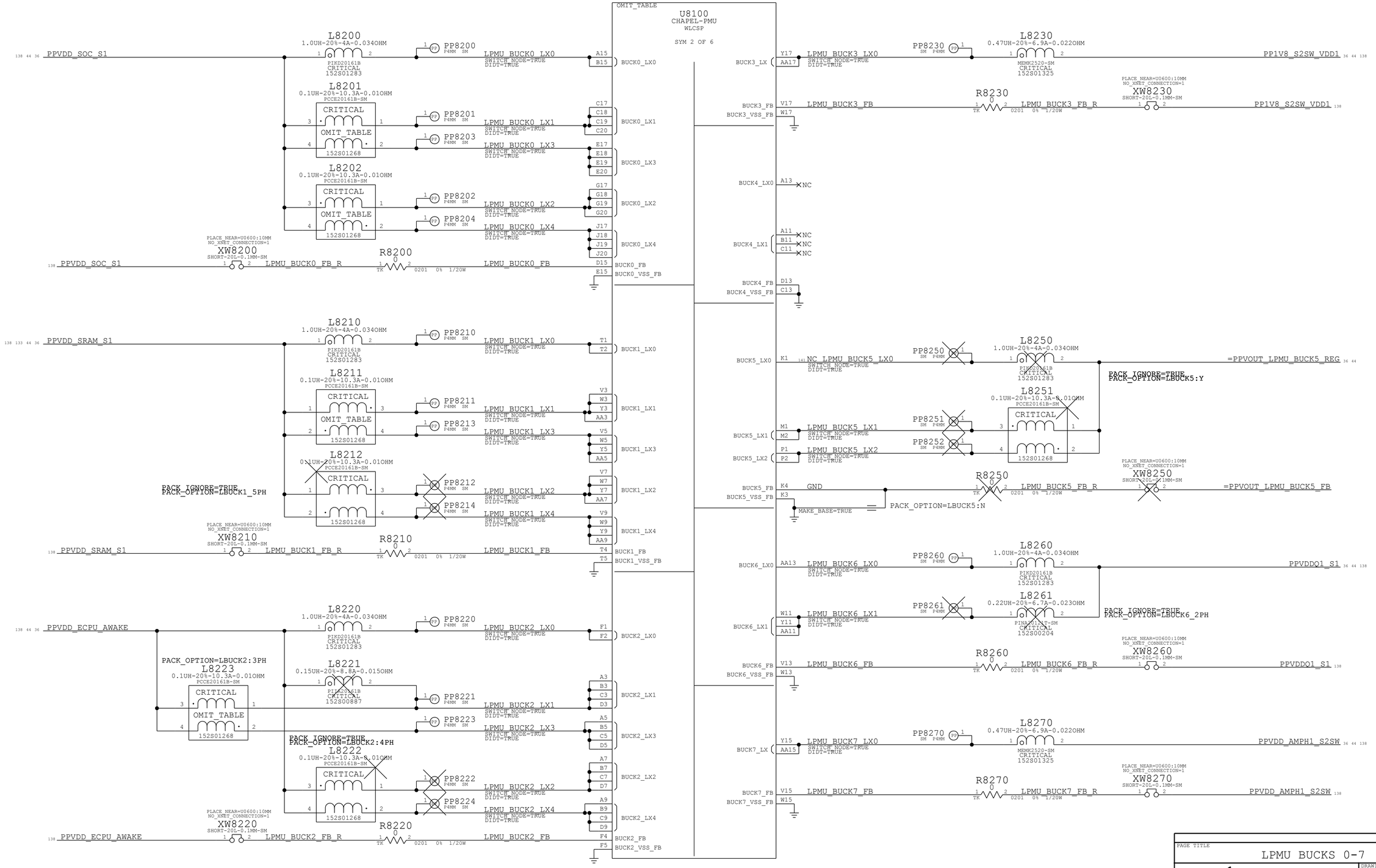

PAGE TITLE

LPMU BUCKS 0-7

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D

REVISION 4.0.0

BRANCH dvt-2

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SHEET 42 OF 156

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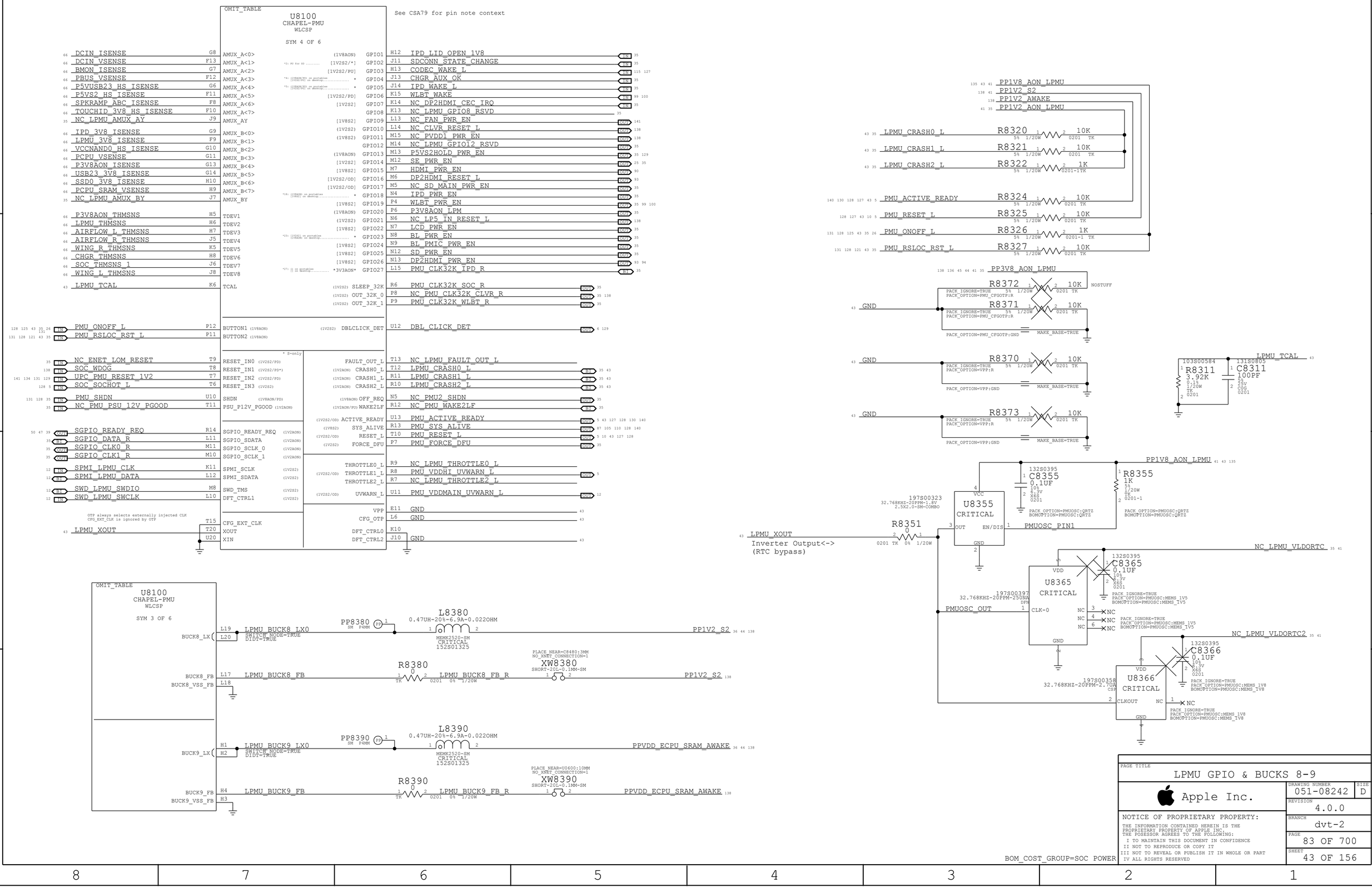
OMIT_TABLE
U8100
CHAPEL-PMU
WLCSP
SYM 4 OF 6
See CSA79 for pin note context
DCIN_ISENSE G8
DCIN_VSENSE F13
BMON_ISENSE G7
PBUS_VSENSE F12
P5VUSB23_HS_ISENSE G6
P5VS2_HS_ISENSE F11
SPKRAMP_ABC_ISENSE F8
TOUCHID_3V8_HS_ISENSE F10
NC_LPMU_AMUX_AY J9
IPD_3V8_ISENSE G9
LPMU_3V8_ISENSE F9
VCCNAND0_HS_ISENSE G10
PCPU_VSENSE G11
P3V8AON_ISENSE G13
USB23_3V8_ISENSE G14
SSD0_3V8_ISENSE H10
PCPU_SRAM_VSENSE H9
NC_LPMU_AMUX_BY J7
P3V8AON_THMSNS H5
LPMU_THMSNS H6
AIRFLOW_L_THMSNS H7
AIRFLOW_R_THMSNS J5
WING_R_THMSNS K5
CHGR_THMSNS H8
SOC_THMSNS_1 J6
WING_L_THMSNS J8
LPMU_TCAL K6
PMU_ONOFF_L P12
PMU_RSLOC_RST_L P11
NC_ENET_LOM_RESET T9
SOC_WDOG T8
UPC_PMU_RESET_1V2 T7
SOC_SOCHOT_L T6
PMU_SHDN U10
NC_PMU_PSU_12V_PGOOD T11
SGPIO_READY_REQ R14
SGPIO_DATA_R L11
SGPIO_CLK0_R M11
SGPIO_CLK1_R M10
SPMI_LPMU_CLK K11
SPMI_LPMU_DATA L12
SWD_LPMU_SWDIO M8
SWD_LPMU_SWCLK L10
OTP always selects externally injected CLK
CFG_EXT_CLK is ignored by OTP
LPMU_XOUT T20
CFG_EXT_CLK T15
XOUT T20
XIN U20
AMUX_A<0> AMUX_A<1> AMUX_A<2> AMUX_A<3> AMUX_A<4> AMUX_A<5> AMUX_A<6> AMUX_A<7> AMUX_AY
AMUX_B<0> AMUX_B<1> AMUX_B<2> AMUX_B<3> AMUX_B<4> AMUX_B<5> AMUX_B<6> AMUX_B<7> AMUX_BY
TDEV1 TDEV2 TDEV3 TDEV4 TDEV5 TDEV6 TDEV7 TDEV8
TCAL
BUTTON1 (1V8AON)
BUTTON2 (1V8AON)
RESET_IN0 (1V2S2/PD)
RESET_IN1 (1V2S2/PD*)
RESET_IN2 (1V2S2/PD)
RESET_IN3 (1V2S2)
SHDN (1V8AON/PD)
PSU_P12V_PGOOD (1V2AON)
SGPIO_READY_REQ (1V2AON)
SGPIO_SDATA (1V2AON)
SGPIO_SCLK_0 (1V2AON)
SGPIO_SCLK_1 (1V2AON)
SPMI_SCLK (1V2S2)
SPMI_SDATA (1V2S2)
SWD_TMS (1V2S2)
DFT_CTRL1 (1V2S2)
* B-only
GPIO1 IPD_LID_OPEN_1V8
GPIO2 SDCONN_STATE_CHANGE
GPIO3 CODEC_WAKE_L
GPIO4 CHGR_AUX_OK
GPIO5 IPD_WAKE_L
GPIO6 WLBT_WAKE
GPIO7 NC_DP2HDMI_CEC_IRQ
GPIO8 NC_LPMU_GPIO8_RSVD
GPIO9 NC_FAN_PWR_EN
GPIO10 NC_CLVR_RESET_L
GPIO11 NC_PVDD1_PWR_EN
GPIO12 NC_LPMU_GPIO12_RSVD
GPIO13 P5VS2HOLD_PWR_EN
GPIO14 SE_PWR_EN
GPIO15 HDMI_PWR_EN
GPIO16 DP2HDMI_RESET_L
GPIO17 NC_SD_MAIN_PWR_EN
GPIO18 IPD_PWR_EN
GPIO19 WLBT_PWR_EN
GPIO20 P3V8AON_LPM
GPIO21 NC_LP5_IN_RESET_L
GPIO22 LCD_PWR_EN
GPIO23 BL_PWR_EN
GPIO24 BL_PMIC_PWR_EN
GPIO25 SD_PWR_EN
GPIO26 DP2HDMI_PWR_EN
GPIO27 *3V3AON*
SLEEP_32K
OUT_32K_0
OUT_32K_1
DBLCLICK_DET
FAULT_OUT_L
CRASH0_L
CRASH1_L
CRASH2_L
OFF_REQ
WAKE2LF
ACTIVE_READY
SYS_ALIVE
RESET_L
FORCE_DFU
THROTTLE0_L
THROTTLE1_L
THROTTLE2_L
UVWARN_L
VPP
CFG_OTP
DFT_CTRL0
DFT_CTRL2
NC_LPMU_THROTTLE0_L
PMU_VDDHI_UVWARN_L
NC_LPMU_THROTTLE2_L
PMU_VDDMAIN_UVWARN_L
GND
PMU_CLK32K_SOC_R
NC_PMU_CLK32K_CLVR_R
PMU_CLK32K_WLBT_R
NC_LPMU_FAULT_OUT_L
LPMU_CRASH0_L
LPMU_CRASH1_L
LPMU_CRASH2_L
NC_PMU2_SHDN
NC_PMU_WAKE2LF
PMU_ACTIVE_READY
PMU_SYS_ALIVE
PMU_RESET_L
PMU_FORCE_DFU
IPD_LID_OPEN_1V8
SDCONN_STATE_CHANGE
CODEC_WAKE_L
CHGR_AUX_OK
IPD_WAKE_L
WLBT_WAKE
NC_DP2HDMI_CEC_IRQ
NC_LPMU_GPIO8_RSVD
NC_FAN_PWR_EN
NC_CLVR_RESET_L
NC_PVDD1_PWR_EN
NC_LPMU_GPIO12_RSVD
P5VS2HOLD_PWR_EN
SE_PWR_EN
HDMI_PWR_EN
DP2HDMI_RESET_L
NC_SD_MAIN_PWR_EN
IPD_PWR_EN
WLBT_PWR_EN
P3V8AON_LPM
NC_LP5_IN_RESET_L
LCD_PWR_EN
BL_PWR_EN
BL_PMIC_PWR_EN
SD_PWR_EN
DP2HDMI_PWR_EN
PMU_CLK32K_IPD_R
PMU_CLK32K_SOC_R
NC_PMU_CLK32K_CLVR_R
PMU_CLK32K_WLBT_R
DBLCLICK_DET
LPMU_CRASH0_L
LPMU_CRASH1_L
LPMU_CRASH2_L
NC_PMU2_SHDN
NC_PMU_WAKE2LF
PMU_ACTIVE_READY
PMU_SYS_ALIVE
PMU_RESET_L
PMU_FORCE_DFU
NC_LPMU_THROTTLE0_L
PMU_VDDHI_UVWARN_L
NC_LPMU_THROTTLE2_L
PMU_VDDMAIN_UVWARN_L
GND
GND
PP1V8_AON_LPMU
PP1V2_S2
PP1V2_AWAKE
PP1V2_AON_LPMU
LPMU_CRASH0_L
LPMU_CRASH1_L
LPMU_CRASH2_L
PMU_ACTIVE_READY
PMU_RESET_L
PMU_ONOFF_L
PMU_RSLOC_RST_L
R8320 10K 5% 1/20W 0201 TK
R8321 10K 5% 1/20W 0201 TK
R8322 1K 5% 1/20W 0201-1TK
R8324 10K 5% 1/20W 0201 TK
R8325 10K 5% 1/20W 0201 TK
R8326 1K 5% 1/20W 0201-1 TK
R8327 10K 5% 1/20W 0201 TK
PP3V8_AON_LPMU
R8372 10K NOSTUFF
R8371 10K
R8370 10K
R8373 10K
GND
PACK_IGNORE=TRUE
PACK_OPTION=PMU_CFGOTP:R
PACK_OPTION=PMU_CFGOTP:GND
PACK_OPTION=VPP:R
PACK_OPTION=VPP:GND
MAKE_BASE=TRUE
103S00584 R8311 3.92K 0.1% 1/20W TK 0201
131S0805 C8311 100PF 5% 25V C0G 0201
LPMU_TCAL
PP1V8_AON_LPMU
R8355 1K 5% 1/20W TK 0201-1
C8355 0.1UF 10% 6.3V X6S 0201
197S00323 32.768KHZ-20PPM-1.8V 2.5X2.0-SM-COMBO
U8355 CRITICAL VCC OUT EN/DIS GND
PMUOSC_PIN1
R8351 0 0% 1/20W 0201 TK
LPMU_XOUT
Inverter Output<-> (RTC bypass)
PACK_OPTION=PMUOSC:QRTZ
BOMOPTION=PMUOSC:QRTZ
NC_LPMU_VLDORTC
C8365 0.1UF 10% 6.3V X6S 0201
197S00397 32.768KHZ-20PPM-250NA DFN
U8365 CRITICAL VDD CLK-0 NC GND
PMUOSC_OUT
PACK_OPTION=PMUOSC:MEMS_1V5
BOMOPTION=PMUOSC:MEMS_1V5
NC_LPMU_VLDORTC2
C8366 0.1UF 10% 6.3V X6S 0201
197S00358 32.768KHZ-20PPM-2.7UA CSP
U8366 CRITICAL VDD CLKOUT NC GND
PACK_OPTION=PMUOSC:MEMS_1V8
BOMOPTION=PMUOSC:MEMS_1V8
OMIT_TABLE
U8100
CHAPEL-PMU
WLCSP
SYM 3 OF 6
BUCK8_LX L19 L20
BUCK8_FB L17
BUCK8_VSS_FB L18
BUCK9_LX H1 H2
BUCK9_FB H4
BUCK9_VSS_FB H3
LPMU_BUCK8_LX0
LPMU_BUCK8_FB
LPMU_BUCK9_LX0
LPMU_BUCK9_FB
SWITCH_NODE=TRUE
DIDT=TRUE
PP8380 SM P4MM
L8380 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM CRITICAL 152S01325
PP1V2_S2
R8380 0 0% 1/20W 0201 TK
LPMU_BUCK8_FB_R
XW8380 SHORT-201-0.1MM-SM
PLACE_NEAR=C8480:3MM
NO_XNET_CONNECTION=1
PP8390 SM P4MM
L8390 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM CRITICAL 152S01325
PPVDD_ECPU_SRAM_AWAKE
R8390 0 0% 1/20W 0201 TK
LPMU_BUCK9_FB_R
XW8390 SHORT-201-0.1MM-SM
PLACE_NEAR=U0600:10MM
NO_XNET_CONNECTION=1
BOM_COST_GROUP=SOC POWER
PAGE TITLE
LPMU GPIO & BUCKS 8-9
Apple Inc.
DRAWING NUMBER 051-08242
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BRANCH dvt-2
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Buck Output Caps (near PMU)

1x 2.2uF 0402 per inductor, rounded up to even number to mirror
2x 0201 per CL pair
More 0402 caps on Bucks that serve system loads, for local bulk/FB

Place 0201 VDD+BUCK caps surrounding PMU near relevant pins

OMIT_TABLE

U8100
CHAPEL-PMU
WLCSP

SYM 1 OF 6

BUCK2
PH0: VSS_BUCK2 (A1, B1, C1, D1)
PH1: VDD_BUCK0_2_4_8_9 (A2, B2, C2, D2); VSS_BUCK2 (A4, B4, C4, D4)
PH3: VDD_BUCK0_2_4_8_9 (A6, B6, C6, D6)
PH2: VSS_BUCK2 (A8, B8, C8, D8)
PH4: VDD_BUCK0_2_4_8_9 (A10, B10, C10, D10)
PACK_OPTION=LBUCK2:3PH
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK2:4PH

BUCK4
PH1: VSS_BUCK4 (A12, B12, C12)
PH0: VDD_BUCK0_2_4_8_9 (A14, B14)

BUCK0
PH0: VSS_BUCK0 (A16, B16)
PH1: VSS_BUCK0 (A17, A18, A19, A20)
PH3: VDD_BUCK0_2_4_8_9 (B17, B18, B19, B20)
PH1: VSS_BUCK0 (D17, D18, D19, D20)
PH3: VDD_BUCK0_2_4_8_9 (F17, F18, F19, F20)
PH2: VSS_BUCK0 (H17, H18, H19, H20)
PH4: VDD_BUCK0_2_4_8_9 (K17, K19, K20)

BUCK8
PH0: VSS_BUCK8 (M19, M20)

BUCK9
PH0: VDD_BUCK0_2_4_8_9 (G2); VSS_BUCK2 (E2)
PH0: VSS_BUCK9_5 (J2); VDD_BUCK0_2_4_8_9 (G1)
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK5:Y

BUCK5
PH0: VDD_BUCK1_5_6_7 (L2); VSS_BUCK9_5 (J1)
PH1: VSS_BUCK9_5 (N2); VDD_BUCK1_5_6_7 (L1)
PH2: VDD_BUCK1_5_6_7 (R2); VSS_BUCK9_5 (N1)
PH0: VSS_BUCK1 (U2); VDD_BUCK1_5_6_7 (R1)

BUCK1
PH0: VSS_BUCK1 (V1, W1, Y1, AA1); VDD_BUCK1_5_6_7 (V2, W2, Y2, AA2)
PH1: VSS_BUCK1 (V4, W4, Y4, AA4); VDD_BUCK1_5_6_7 (V6, W6, Y6, AA6)
PH2: VSS_BUCK1 (V8, W8, Y8, AA8); VDD_BUCK1_5_6_7 (V10, W10, Y10, AA10)
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK1_5PH
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK6_2PH
PH1: VSS_BUCK6 (W12, Y12, AA12); VDD_BUCK1_5_6_7 (Y14, AA14)

BUCK6
PH0: VSS_BUCK6 (W12, Y12, AA12); VDD_BUCK1_5_6_7 (Y14, AA14)

BUCK7
PH0: VDD_BUCK1_5_6_7 (Y16, AA16); VSS_BUCK3_7 (Y18, AA18)

BUCK3
PH0: VSS_BUCK3_7 (AA16); VDD_BUCK3 (AA18)

PP3V8_AON_LPMU 35 41 43 45 136 138

0 — PPVDD_SOC_S1 138 42 36
C8400 2.2UF 20% 6.3V X6S-CERM 0402 1
C8401 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8400)
C8402 2.2UF 10% 10V X6S-CERM 0402 1
C8403 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8402)
C8404 0.22UF 20% 6.3V X6S-CERM 0201 1
C8405 0.22UF 20% 6.3V X6S-CERM 0201 1
C8406 0.22UF 20% 6.3V X6S-CERM 0201 1
C8407 0.22UF 20% 6.3V X6S-CERM 0201 1

1 — PPVDD_SRAM_S1 138 133 42 36
C8410 2.2UF 20% 6.3V X6S-CERM 0402 1
C8411 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8410)
C8412 2.2UF 10% 10V X6S-CERM 0402 1
C8413 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8412)
C8414 0.22UF 20% 6.3V X6S-CERM 0201 1
C8415 0.22UF 20% 6.3V X6S-CERM 0201 1
C8416 0.22UF 20% 6.3V X6S-CERM 0201 1
C8417 0.22UF 20% 6.3V X6S-CERM 0201 1
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK1_5PH
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK1_5PH

2 — PPVDD_ECPU_AWAKE 138 42 36
C8420 2.2UF 20% 6.3V X6S-CERM 0402 1
C8421 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8420)
C8422 2.2UF 10% 10V X6S-CERM 0402 1
C8423 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8422)
C8424 0.22UF 20% 6.3V X6S-CERM 0201 1
C8425 0.22UF 20% 6.3V X6S-CERM 0201 1
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK2:4PH

3 — PP1V8_S2SW_VDD1 138 42 36
C8430 2.2UF 20% 6.3V X6S-CERM 0402 1
C8431 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8430)

4 <Unused>

5 — =PPVOUT_LPMU_BUCK5_REG 42 36
C8450 2.2UF 20% 6.3V X6S-CERM 0402 1
C8451 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8450)
C8454 0.22UF 20% 6.3V X6S-CERM 0201 1
C8455 0.22UF 20% 6.3V X6S-CERM 0201 1
PACK_IGNORE=TRUE
PACK_OPTION=LBUCK5:Y

6 — PPVDDQ1_S1 138 42 36
C8460 2.2UF 20% 6.3V X6S-CERM 0402 1
C8461 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8460)

7 — PPVDD_AMPH1_S2SW 138 42 36
C8470 2.2UF 20% 6.3V X6S-CERM 0402 1
C8471 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8470)

8 — PP1V2_S2 138 43 36
C8480 2.2UF 20% 6.3V X6S-CERM 0402 1
C8481 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8480)
C8484 15UF 20% 2.5V X6S 0402-4 1 (BOMSWAP=138800392)
C8485 15UF 20% 2.5V X6S 0402-4 1 (MIRROR WITH=C8484; BOMSWAP=138800392)
C8486 15UF 20% 2.5V X6S 0402-4 1 (MIRROR WITH=C8484; BOMSWAP=138800392)
C8487 15UF 20% 2.5V X6S 0402-4 1 (MIRROR WITH=C8484; BOMSWAP=138800392)
C8488 15UF 20% 2.5V X6S 0402-4 1 (MIRROR WITH=C8484; BOMSWAP=138800392)
C8489 15UF 20% 2.5V X6S 0402-4 1 (MIRROR WITH=C8484; BOMSWAP=138800392)

9 — PPVDD_ECPU_SRAM_AWAKE 138 43 36
C8490 2.2UF 20% 6.3V X6S-CERM 0402 1
C8491 2.2UF 10% 10V X6S-CERM 0402 1 (MIRROR WITH=C8490)

C84A0–C84A3, C84AA–C84AD, C84B0–C84B4, C84BA–C84BE, C84C0–C84C5, C84CA–C84CF, C84D0–C84D7, C84DA–C84DH: 1UF 20% 6.3V X6S-CERM 0201 (138S00040) / 2.2UF 20% 6.3V X6S 0201 (138S00377)

C84A6, C84AG, C84B6, C84BG: 1UF 20% 6.3V X6S-CERM 0201 (138S00040) / 2.2UF 20% 6.3V X6S 0201 (138S00377)

C84F0–C84F9, C84FA–C84FG: 10UF 20% 6.3V CERM-X6S 0402 (138S00858)

1x 10uF input per inductor

Place under LX pins of each single-inductor phase
Place under shared VSS_BUCK pins of each CL-inductor pair

TBD whether we want to use PACK OPTIONS for unused phases

BOM_COST_GROUP=SOC POWER

PAGE TITLE: LPMU BUCK IN/OUT CAPS

Apple Inc.

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Input desense caps are shared across portables, until further notice

LPMU

138 136 44 43 41 35 PP3V8_AON_LPMU

131S0445 C8500 12PF 5% 25V NPO-C0G 0201	131S0439 C8501 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C8502 12PF 5% 25V NPO-C0G 0201	131S0445 C8503 12PF 5% 25V NPO-C0G 0201	131S0439 C8504 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C8505 12PF 5% 25V NPO-C0G 0201	131S0198 C8506 1.8PF +/-0.1PF 25V C0G 201	131S0198 C8507 1.8PF +/-0.1PF 25V C0G 201	131S0439 C8508 3.0PF +/-0.1PF 25V NPO-C0G 0201
131S0445 C8509 12PF 5% 25V NPO-C0G 0201	131S0439 C850A 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0198 C850B 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850C 12PF 5% 25V NPO-C0G 0201	131S0439 C850D 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0198 C850E 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850F 12PF 5% 25V NPO-C0G 0201	131S0198 C850G 1.8PF +/-0.1PF 25V C0G 201	131S0439 C850H 3.0PF +/-0.1PF 25V NPO-C0G 0201
131S0439 C850I 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0198 C850J 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850K 12PF 5% 25V NPO-C0G 0201	131S0198 C850L 1.8PF +/-0.1PF 25V C0G 201	131S0198 C850M 1.8PF +/-0.1PF 25V C0G 201	131S0198 C850N 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850O 12PF 5% 25V NPO-C0G 0201	131S0439 C850P 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C850Q 12PF 5% 25V NPO-C0G 0201
131S0439 C850R 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0198 C850S 1.8PF +/-0.1PF 25V C0G 201	131S0439 C850T 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C850U 12PF 5% 25V NPO-C0G 0201	131S0198 C850V 1.8PF +/-0.1PF 25V C0G 201	131S0445 C850W 12PF 5% 25V NPO-C0G 0201	131S0439 C850X 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C850Y 12PF 5% 25V NPO-C0G 0201	131S0439 C850Z 3.0PF +/-0.1PF 25V NPO-C0G 0201
131S0445 C8511 12PF 5% 25V NPO-C0G 0201	131S0198 C8512 1.8PF +/-0.1PF 25V C0G 201	131S0445 C8513 12PF 5% 25V NPO-C0G 0201	131S0439 C8514 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0439 C8515 3.0PF +/-0.1PF 25V NPO-C0G 0201				

FPMU

138 136 40 39 37 35 PP3V8_AON_FPMU

131S0445 C8550 12PF 5% 25V NPO-C0G 0201	131S0439 C8551 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C8552 12PF 5% 25V NPO-C0G 0201	131S0198 C8553 1.8PF +/-0.1PF 25V C0G 201	131S0439 C8554 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C8555 12PF 5% 25V NPO-C0G 0201	131S0445 C8556 12PF 5% 25V NPO-C0G 0201	131S0439 C8557 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0439 C8558 3.0PF +/-0.1PF 25V NPO-C0G 0201
131S0198 C8559 1.8PF +/-0.1PF 25V C0G 201	131S0198 C855A 1.8PF +/-0.1PF 25V C0G 201	131S0439 C855B 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C855C 12PF 5% 25V NPO-C0G 0201	131S0445 C855D 12PF 5% 25V NPO-C0G 0201	131S0198 C855E 1.8PF +/-0.1PF 25V C0G 201	131S0198 C855F 1.8PF +/-0.1PF 25V C0G 201	131S0439 C855G 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C855H 12PF 5% 25V NPO-C0G 0201
131S0445 C855I 12PF 5% 25V NPO-C0G 0201	131S0198 C855J 1.8PF +/-0.1PF 25V C0G 201	131S0439 C855K 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C855L 12PF 5% 25V NPO-C0G 0201	131S0439 C855M 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C855N 12PF 5% 25V NPO-C0G 0201	131S0445 C855O 12PF 5% 25V NPO-C0G 0201	131S0198 C855P 1.8PF +/-0.1PF 25V C0G 201	131S0439 C855Q 3.0PF +/-0.1PF 25V NPO-C0G 0201
131S0445 C855R 12PF 5% 25V NPO-C0G 0201	131S0439 C855S 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C855T 12PF 5% 25V NPO-C0G 0201	131S0445 C855U 12PF 5% 25V NPO-C0G 0201	131S0439 C855V 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0198 C855W 1.8PF +/-0.1PF 25V C0G 201	131S0198 C855X 1.8PF +/-0.1PF 25V C0G 201	131S0439 C855Y 3.0PF +/-0.1PF 25V NPO-C0G 0201	131S0445 C855Z 12PF 5% 25V NPO-C0G 0201

BOM_COST_GROUP=SOC POWER

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Desense Caps for Spitfire PMU

@U9300 PCPU

47 PP3V8_AON_VDDMAIN_PCPUVR
- C9210 12PF 25V NP0-C0G 5% 0201
- C9211 3PF 25V C0G +/-0.1PF 0201
- C9212 1.8PF 25V C0G +/-0.1PF 201

47 PP1V5_AON_DIG_PCPUVR
- C9213 12PF 25V NP0-C0G 5% 0201

47 PP1V5_AON_ANA_PCPUVR
- C9214 12PF 25V NP0-C0G 5% 0201
- C9215 3PF 25V C0G +/-0.1PF 0201
- C9216 1.8PF 25V C0G +/-0.1PF 201

48 PCPU_LX1
- C9217 12PF 25V NP0-C0G 5% 0201
- C9218 3PF 25V C0G +/-0.1PF 0201

48 PCPUSRAM_LX0
- C9219 12PF 25V NP0-C0G 5% 0201
- C921A 3PF 25V C0G +/-0.1PF 0201

1x Triplet per Bulk

137 129 63 46 PPVDD_PCPU_AWAKE
- C921B 12PF 25V NP0-C0G 5% 0201 — 1
- C921C 3PF 25V C0G +/-0.1PF 0201
- C921D 1.8PF 25V C0G +/-0.1PF 201
- C921E 12PF 25V NP0-C0G 5% 0201 — 2
- C921F 3PF 25V C0G +/-0.1PF 0201
- C921G 1.8PF 25V C0G +/-0.1PF 201
- C921H 12PF 25V NP0-C0G 5% 0201 — 3
- C921I 3PF 25V C0G +/-0.1PF 0201
- C921J 1.8PF 25V C0G +/-0.1PF 201
- C921K 12PF 25V NP0-C0G 5% 0201 — 4
- C921L 3PF 25V C0G +/-0.1PF 0201
- C921M 1.8PF 25V C0G +/-0.1PF 201

@U0600 SOC

137 129 63 46 PPVDD_PCPU_AWAKE
- C9220 12PF 25V NP0-C0G 5% 0201 — 1
- C9221 3PF 25V C0G +/-0.1PF 0201
- C9222 1.8PF 25V C0G +/-0.1PF 201
- C9223 12PF 25V NP0-C0G 5% 0201 — 2
- C9224 3PF 25V C0G +/-0.1PF 0201
- C9225 1.8PF 25V C0G +/-0.1PF 201
- C9226 12PF 25V NP0-C0G 5% 0201 — 3
- C9227 3PF 25V C0G +/-0.1PF 0201
- C9228 1.8PF 25V C0G +/-0.1PF 201

3x Triplets
@SOC PCPU

137 129 63 46 PPVDD_GPU_AWAKESW
- C9229 12PF 25V NP0-C0G 5% 0201 — 1
- C922A 3PF 25V C0G +/-0.1PF 0201
- C922B 1.8PF 25V C0G +/-0.1PF 201
- C922C 12PF 25V NP0-C0G 5% 0201 — 2
- C922D 3PF 25V C0G +/-0.1PF 0201
- C922E 1.8PF 25V C0G +/-0.1PF 201
- C922F 12PF 25V NP0-C0G 5% 0201 — 3
- C922G 3PF 25V C0G +/-0.1PF 0201
- C922H 1.8PF 25V C0G +/-0.1PF 201
- C922I 12PF 25V NP0-C0G 5% 0201 — 4
- C922J 3PF 25V C0G +/-0.1PF 0201
- C922K 1.8PF 25V C0G +/-0.1PF 201

4x Triplets
@SOC GPU

137 129 63 46 PPVDD_PCPU_SRAM_AWAKE
- C922L 12PF 25V NP0-C0G 5% 0201 — 1
- C922M 3PF 25V C0G +/-0.1PF 0201
- C922N 1.8PF 25V C0G +/-0.1PF 201
- C922P 12PF 25V NP0-C0G 5% 0201 — 2
- C922R 3PF 25V C0G +/-0.1PF 0201
- C922Q 1.8PF 25V C0G +/-0.1PF 201

2x Triplets
@SOC SRAM

@U9600 GPU

50 PP3V8_AON_VDDMAIN_GPUVR
- C9230 12PF 25V NP0-C0G 5% 0201
- C9231 3PF 25V C0G +/-0.1PF 0201
- C9232 1.8PF 25V C0G +/-0.1PF 201

50 PP1V5_AON_DIG_GPUVR
- C9233 12PF 25V NP0-C0G 5% 0201

50 PP1V5_AON_ANA_GPUVR
- C9234 12PF 25V NP0-C0G 5% 0201
- C9235 3PF 25V C0G +/-0.1PF 0201
- C9236 1.8PF 25V C0G +/-0.1PF 201

51 GPU_LX1
- C9237 12PF 25V NP0-C0G 5% 0201
- C9238 3PF 25V C0G +/-0.1PF 0201

129 63 46 137 PPVDD_GPU_AWAKESW
- C9239 12PF 25V NP0-C0G 5% 0201 — 1
- C923A 3PF 25V C0G +/-0.1PF 0201
- C923B 1.8PF 25V C0G +/-0.1PF 201
- C923C 12PF 25V NP0-C0G 5% 0201 — 2
- C923D 3PF 25V C0G +/-0.1PF 0201
- C923E 1.8PF 25V C0G +/-0.1PF 201
- C923F 12PF 25V NP0-C0G 5% 0201 — 3
- C923G 3PF 25V C0G +/-0.1PF 0201
- C923H 1.8PF 25V C0G +/-0.1PF 201
- C923I 12PF 25V NP0-C0G 5% 0201 — 4
- C923J 3PF 25V C0G +/-0.1PF 0201
- C923K 1.8PF 25V C0G +/-0.1PF 201
- C923L 12PF 25V NP0-C0G 5% 0201 — 5
- C923M 3PF 25V C0G +/-0.1PF 0201
- C923N 1.8PF 25V C0G +/-0.1PF 201
- C923P 12PF 25V NP0-C0G 5% 0201 — 6
- C923R 3PF 25V C0G +/-0.1PF 0201
- C923Q 1.8PF 25V C0G +/-0.1PF 201

1x Triplet per Bulk

@EKARA

135 128 55 46 PPBUS_AON
- C9240 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9500.27:10MM
- C9241 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9500.27:10MM
- C9242 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9500.27:10MM

@PCPU Ekara

49 PP5V_S2_PCPU_SPS5
- C9243 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9500.2:10MM
- C9244 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9500.2:10MM
- C9245 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9500.2:10MM

49 PCPU_LX5
- C9246 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9500.9:10MM
- C9247 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9500.9:10MM
- C9248 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9500.9:10MM

139 PPVDD_PCPU_AWAKE_REGEXT5
- C924Y 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=L9500.2:10MM
- C924X 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=L9500.2:10MM
- C925Y 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=L9500.2:10MM

1

128 55 46 135 PPBUS_AON
- C9249 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9800.27:10MM
- C924A 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9800.27:10MM
- C924B 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9800.27:10MM

@GPU Ekara Phase5

2 52 PP5V_S2_GPU_SPS5
- C924C 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9800.2:10MM
- C924D 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9800.2:10MM
- C924E 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9800.2:10MM

3 52 GPU_LX5
- C924F 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9800.9:10MM
- C924G 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9800.9:10MM
- C924H 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9800.9:10MM

4 137 PPVDD_GPU_AWAKESW_REGEXT5
- C924I 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=L9800.2:10MM
- C924J 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=L9800.2:10MM
- C924K 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=L9800.2:10MM

5

135 128 55 46 PPBUS_AON
- C924L 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9850.27:10MM
- C924M 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9850.27:10MM
- C924N 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9850.27:10MM

@GPU Ekara Phase6

6 52 PP5V_S2_GPU_SPS6
- C924P 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9850.2:10MM
- C924R 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9850.2:10MM
- C924Q 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9850.2:10MM

52 GPU_LX6
- C925Z 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9850.9:10MM
- C924S 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9850.9:10MM
- C924T 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9850.9:10MM

137 PPVDD_GPU_AWAKESW_REGEXT6
- C924U 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=U9850.2:10MM
- C924V 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=U9850.2:10MM
- C924W 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=U9850.2:10MM

@Rsense

137 129 63 46 PPVDD_PCPU_AWAKE
- C921N 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=RE063.2:10MM
- C921O 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=RE063.2:10MM
- C921P 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=RE063.2:10MM

137 129 63 46 PPVDD_PCPU_AWAKE
- C921Q 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=RE064.2:10MM
- C921R 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=RE064.2:10MM
- C921S 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=RE064.2:10MM

137 129 63 46 PPVDD_PCPU_SRAM_AWAKE
- C921T 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=RE065.2:10MM
- C921U 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=RE065.2:10MM
- C921V 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=RE065.2:10MM

@Rsense

PLACE_NEAR=RE060.2:10MM

137 129 63 46 PPVDD_GPU_AWAKESW
- C924Z 12PF 25V NP0-C0G 5% 0201
- C923S 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=RE060.2:10MM
- C923T 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=RE060.2:10MM

137 129 63 46 PPVDD_GPU_AWAKESW
- C923U 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=RE061.2:10MM
- C923V 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=RE061.2:10MM
- C923W 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=RE061.2:10MM

137 129 63 46 PPVDD_GPU_AWAKESW
- C923X 12PF 25V NP0-C0G 5% 0201 PLACE_NEAR=RE062.2:10MM
- C923Y 3PF 25V C0G +/-0.1PF 0201 PLACE_NEAR=RE062.2:10MM
- C923Z 1.8PF 25V C0G +/-0.1PF 201 PLACE_NEAR=RE062.2:10MM

BOM_COST_GROUP=SOC POWER

PAGE TITLE: PCPU GPU VR: Desense Caps

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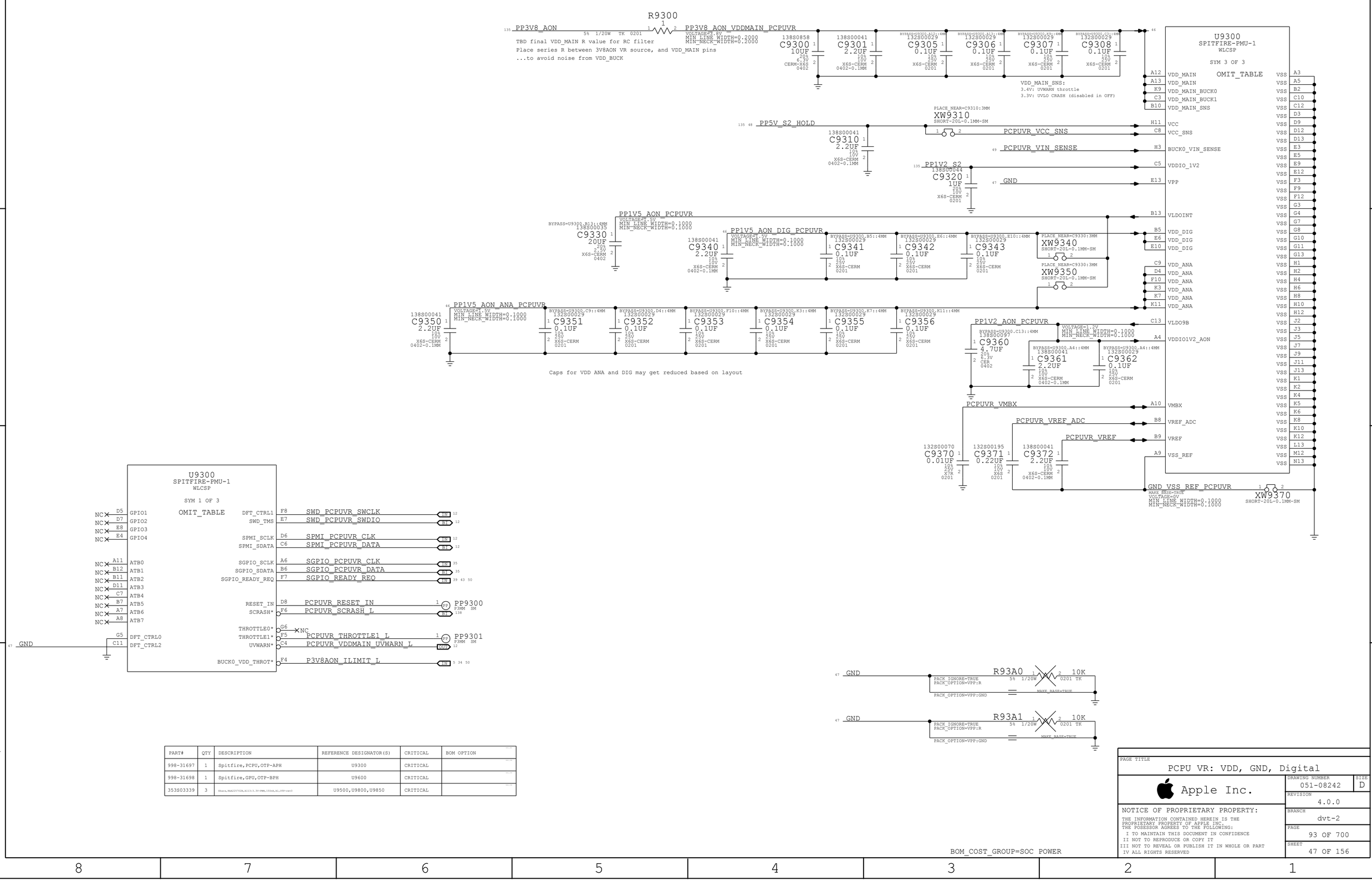

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-31697	1	Spitfire,PCPU,OTP-APH	U9300	CRITICAL	
998-31698	1	Spitfire,GPU,OTP-BPH	U9600	CRITICAL	
353S03339	3	Diara,BAA2257028,A1S3:3.3V-PWM,150nH,X1,OTP-rev3	U9500,U9800,U9850	CRITICAL	

PAGE TITLE

PCPU VR: VDD, GND, Digital

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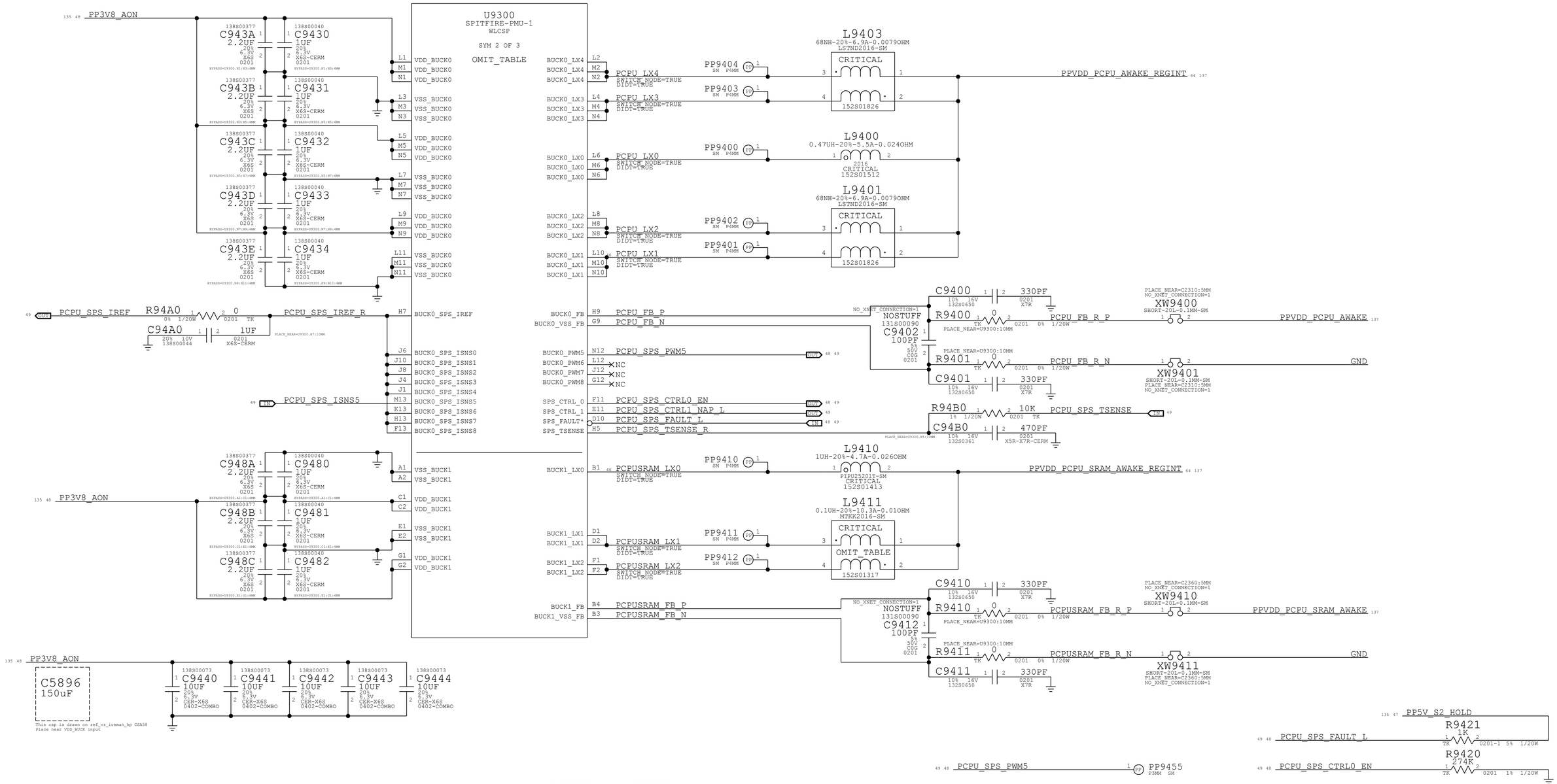

rdar://103076975 rdar://104334933

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S01837	1	IND,CPLD,100NH,20%,9.5A,10.5MO,2218,1.0M	L9411	CRITICAL	
152S01837	9	IND,CPLD,100NH,20%,9.5A,10.5MO,2218,1.0M	L9403,L9401,L9410,L9400,L9404,L9402,L9405,L9406,L9407	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE
PCPU VR: Internal Phases (Core, SRAM)

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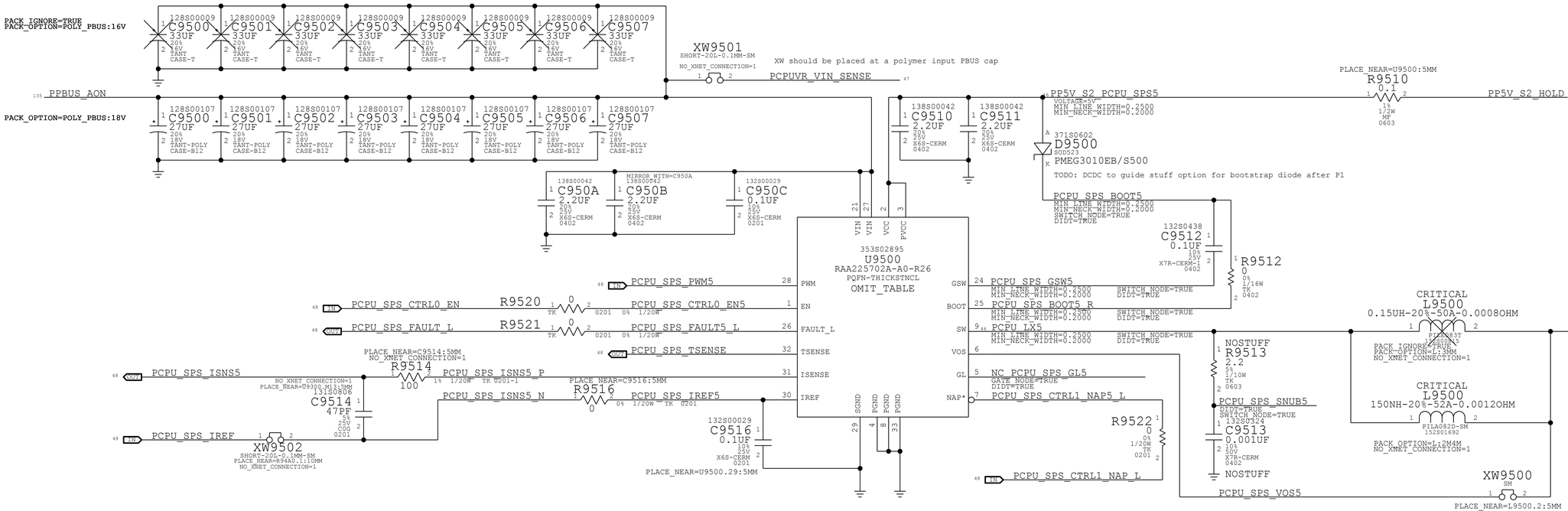

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PAGE TITLE
PCPU VR: External Phase (Core)

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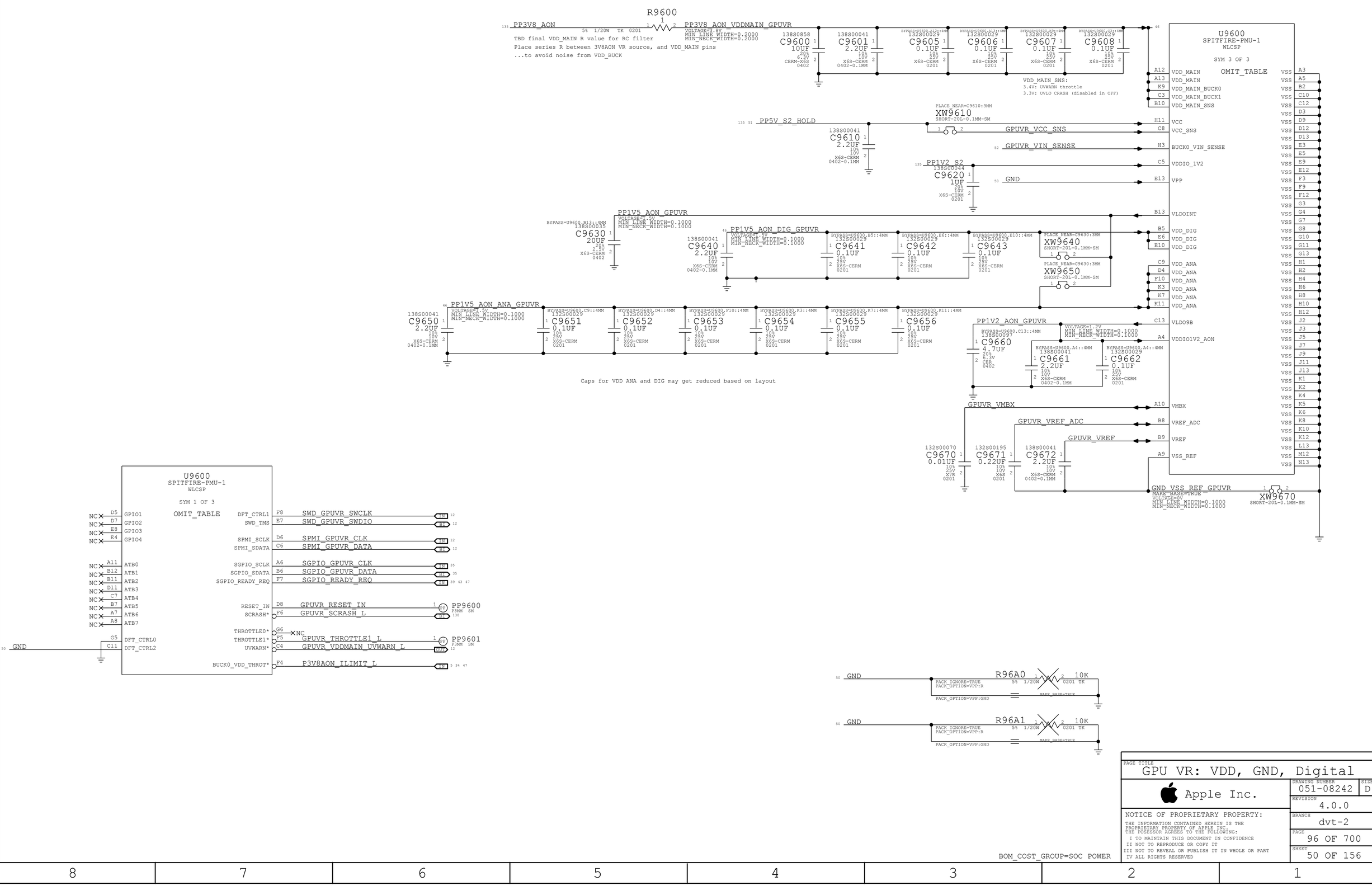
R9600
PP3V8_AON
PP3V8_AON_VDDMAIN_GPUVR
TBD final VDD_MAIN R value for RC filter
Place series R between 3V8AON VR source, and VDD_MAIN pins
...to avoid noise from VDD_BUCK
U9600
SPITFIRE-PMU-1
WLCSP
SYM 3 OF 3
OMIT_TABLE
VDD_MAIN_SNS:
3.4V: UVWARN throttle
3.3V: UVLO CRASH (disabled in OFF)
PP5V_S2_HOLD
XW9610
GPUVR_VCC_SNS
GPUVR_VIN_SENSE
PP1V2_S2
GND
PP1V5_AON_GPUVR
PP1V5_AON_DIG_GPUVR
XW9640
XW9650
PP1V5_AON_ANA_GPUVR
Caps for VDD ANA and DIG may get reduced based on layout
PP1V2_AON_GPUVR
GPUVR_VMBX
GPUVR_VREF_ADC
GPUVR_VREF
GND_VSS_REF_GPUVR
XW9670
U9600
SPITFIRE-PMU-1
WLCSP
SYM 1 OF 3
OMIT_TABLE
GND
R96A0
R96A1
10K
PAGE TITLE
GPU VR: VDD, GND, Digital
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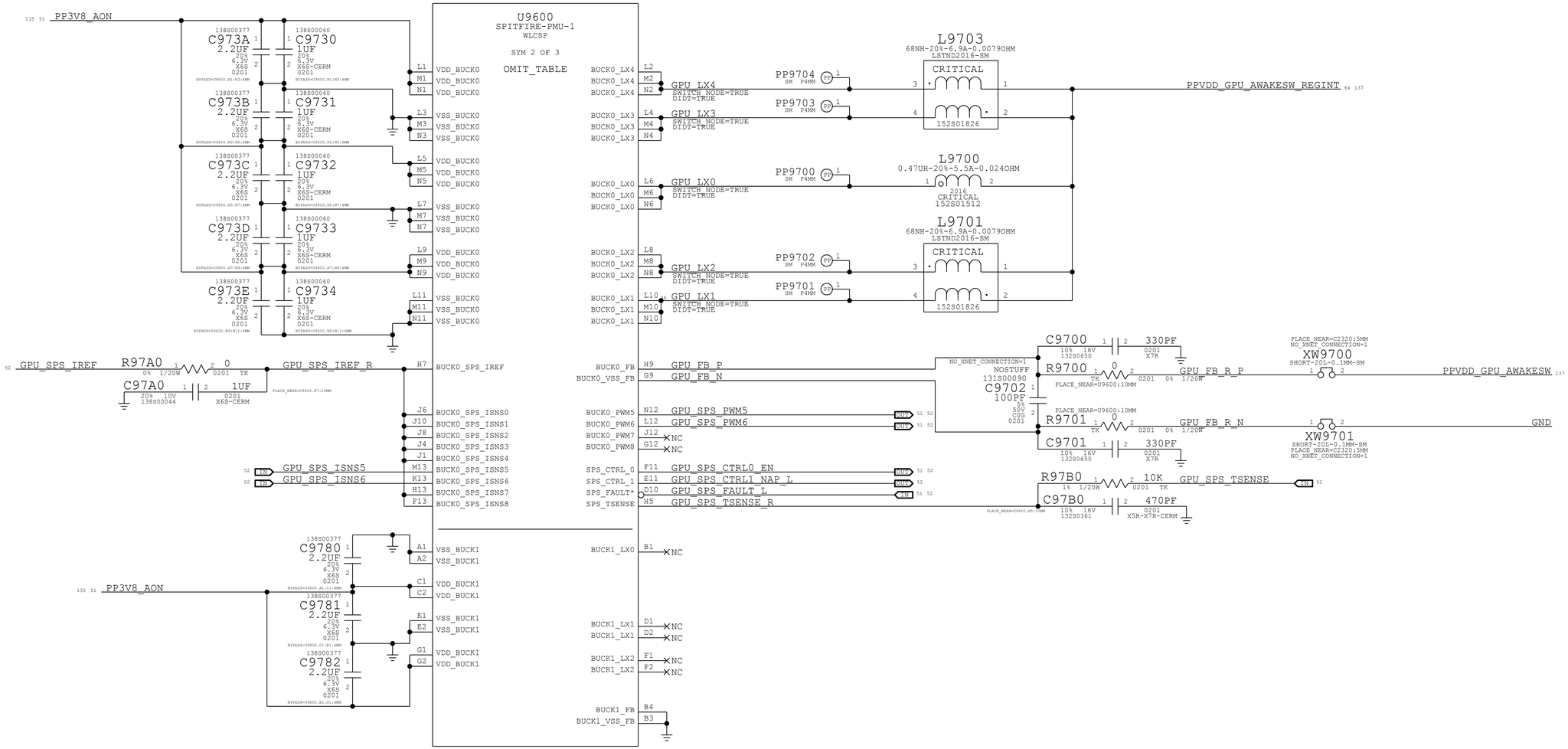

PAGE TITLE: GPU VR: Internal Phases

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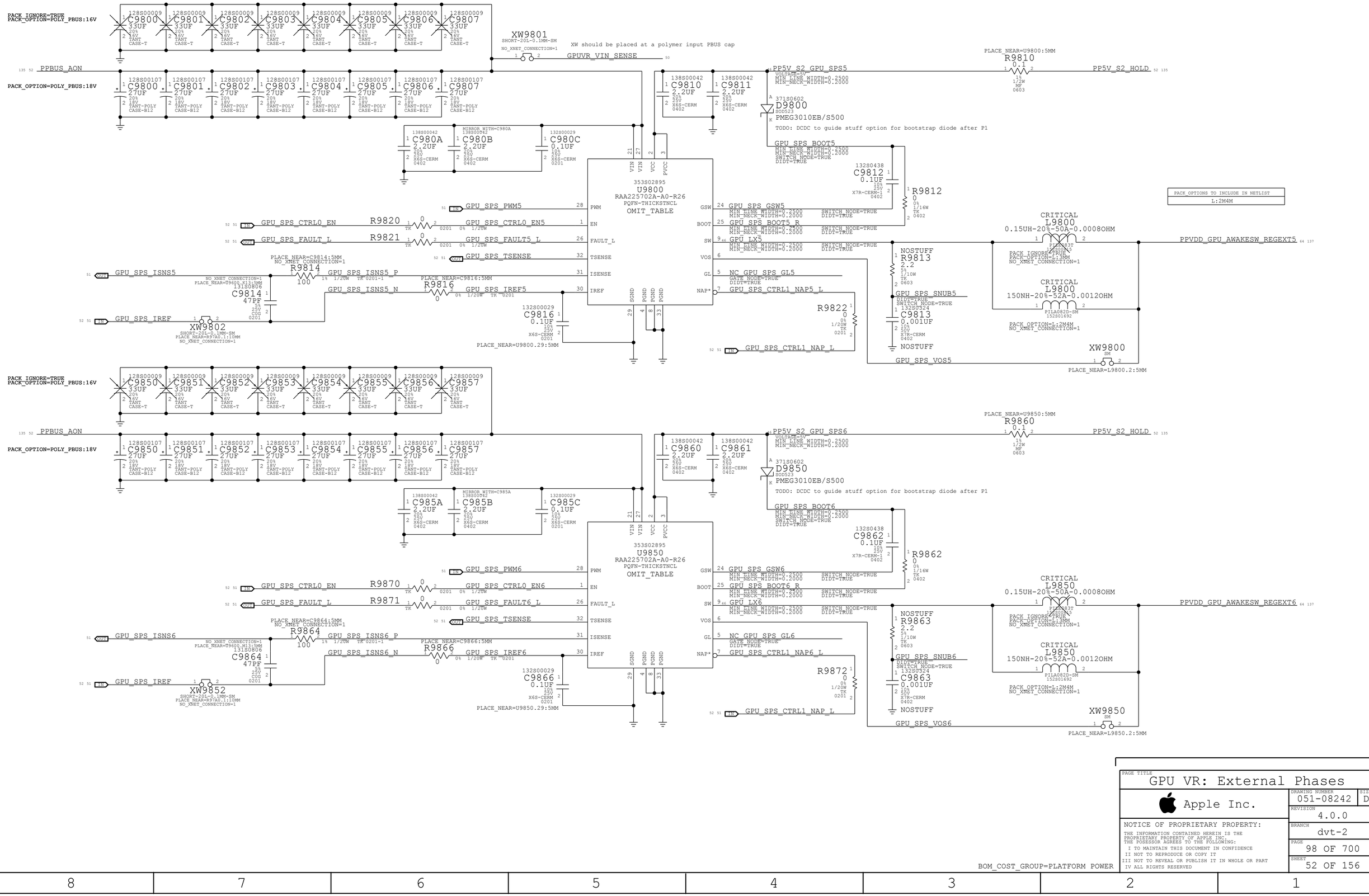

PAGE TITLE: GPU VR: External Phases

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These Caps are placed near the PMU, but AFTER any output Rsense

VR-side Output Caps (U9300)

137 64 PPVDD_PCPU_AWAKE

C9900 180UF 20% 2.5V POLY-AL SM	C9901 180UF 20% 2.5V POLY-AL SM	C9904 180UF 20% 2.5V POLY-AL SM	C9902 470UF 20% 2.5V POLY-AL D-SM	C9903 470UF 20% 2.5V POLY-AL D-SM					
C9910 20UF 20% 2.5V X6S 0402-3	C9911 20UF 20% 2.5V X6S 0402-3	C9912 20UF 20% 2.5V X6S 0402-3	C9913 20UF 20% 2.5V X6S 0402-3	C9914 20UF 20% 2.5V X6S 0402-3	C9915 20UF 20% 2.5V X6S 0402-3	C9916 20UF 20% 2.5V X6S 0402-3	C9917 20UF 20% 2.5V X6S 0402-3	C9918 20UF 20% 2.5V X6S 0402-3	C9919 20UF 20% 2.5V X6S 0402-3
C9920 20UF 20% 2.5V X6S 0402-3	C9921 20UF 20% 2.5V X6S 0402-3	C9922 20UF 20% 2.5V X6S 0402-3	C9923 20UF 20% 2.5V X6S 0402-3	C9924 20UF 20% 2.5V X6S 0402-3	C9925 20UF 20% 2.5V X6S 0402-3	C9926 20UF 20% 2.5V X6S 0402-3	C9927 20UF 20% 2.5V X6S 0402-3	C9928 20UF 20% 2.5V X6S 0402-3	C9929 20UF 20% 2.5V X6S 0402-3
C9930 20UF 20% 2.5V X6S 0402-3	C9931 20UF 20% 2.5V X6S 0402-3	C9932 20UF 20% 2.5V X6S 0402-3	C9933 20UF 20% 2.5V X6S 0402-3	C9934 20UF 20% 2.5V X6S 0402-3	C9935 20UF 20% 2.5V X6S 0402-3	C9936 20UF 20% 2.5V X6S 0402-3	C9937 20UF 20% 2.5V X6S 0402-3	C9938 20UF 20% 2.5V X6S 0402-3	C9939 20UF 20% 2.5V X6S 0402-3
C9940 20UF 20% 2.5V X6S 0402-3	C9941 20UF 20% 2.5V X6S 0402-3	C9942 20UF 20% 2.5V X6S 0402-3	C9943 20UF 20% 2.5V X6S 0402-3	C9944 20UF 20% 2.5V X6S 0402-3	C9945 20UF 20% 2.5V X6S 0402-3	C9946 20UF 20% 2.5V X6S 0402-3	C9947 20UF 20% 2.5V X6S 0402-3	C9948 20UF 20% 2.5V X6S 0402-3	C9949 20UF 20% 2.5V X6S 0402-3
C990A 2.2UF 10% 10V X6S 0402	C990B 2.2UF 10% 10V X6S 0402	C990C 2.2UF 10% 10V X6S 0402	C990E 0.22UF 20% 6.3V X6S-CERM 0201	C990F 0.22UF 20% 6.3V X6S-CERM 0201	C990G 0.22UF 20% 6.3V X6S-CERM 0201	C990H 0.22UF 20% 6.3V X6S-CERM 0201			

137 64 PPVDD_PCPU_SRAM_AWAKE

C99A0 20UF 20% 2.5V X6S 0402-3	C99A1 20UF 20% 2.5V X6S 0402-3	C99A2 20UF 20% 2.5V X6S 0402-3	C99A3 20UF 20% 2.5V X6S 0402-3	C99A4 20UF 20% 2.5V X6S 0402-3	C99A5 20UF 20% 2.5V X6S 0402-3	C99A6 20UF 20% 2.5V X6S 0402-3	C99A7 20UF 20% 2.5V X6S 0402-3	
C99BA 2.2UF 10% 10V X6S 0402	C99BB 2.2UF 10% 10V X6S 0402	C99BE 0.22UF 20% 6.3V X6S-CERM 0201	C99BF 0.22UF 20% 6.3V X6S-CERM 0201					

VR-side Output Caps (U9600)

137 64 PPVDD_GPU_AWAKESW

C9950 180UF 20% 2.5V POLY-AL SM	C9951 180UF 20% 2.5V POLY-AL SM	C9953 180UF 20% 2.5V POLY-AL SM	C9954 180UF 20% 2.5V POLY-AL SM	C9956 180UF 20% 2.5V POLY-AL SM	C9952 470UF 20% 2.5V POLY-AL D-SM	C9955 470UF 20% 2.5V POLY-AL D-SM	C9957 470UF 20% 2.5V POLY-AL D-SM		
C9960 20UF 20% 2.5V X6S 0402-3	C9961 20UF 20% 2.5V X6S 0402-3	C9962 20UF 20% 2.5V X6S 0402-3	C9963 20UF 20% 2.5V X6S 0402-3	C9964 20UF 20% 2.5V X6S 0402-3	C9965 20UF 20% 2.5V X6S 0402-3	C9966 20UF 20% 2.5V X6S 0402-3	C9967 20UF 20% 2.5V X6S 0402-3	C9968 20UF 20% 2.5V X6S 0402-3	C9969 20UF 20% 2.5V X6S 0402-3
C9970 20UF 20% 2.5V X6S 0402-3	C9971 20UF 20% 2.5V X6S 0402-3	C9972 20UF 20% 2.5V X6S 0402-3	C9973 20UF 20% 2.5V X6S 0402-3	C9974 20UF 20% 2.5V X6S 0402-3	C9975 20UF 20% 2.5V X6S 0402-3	C9976 20UF 20% 2.5V X6S 0402-3	C9977 20UF 20% 2.5V X6S 0402-3	C9978 20UF 20% 2.5V X6S 0402-3	C9979 20UF 20% 2.5V X6S 0402-3
C9980 20UF 20% 2.5V X6S 0402-3	C9981 20UF 20% 2.5V X6S 0402-3	C9982 20UF 20% 2.5V X6S 0402-3	C9983 20UF 20% 2.5V X6S 0402-3	C9984 20UF 20% 2.5V X6S 0402-3	C9985 20UF 20% 2.5V X6S 0402-3	C9986 20UF 20% 2.5V X6S 0402-3	C9987 20UF 20% 2.5V X6S 0402-3	C9988 20UF 20% 2.5V X6S 0402-3	C9989 20UF 20% 2.5V X6S 0402-3
C9990 20UF 20% 2.5V X6S 0402-3	C9991 20UF 20% 2.5V X6S 0402-3	C9992 20UF 20% 2.5V X6S 0402-3	C9993 20UF 20% 2.5V X6S 0402-3	C9994 20UF 20% 2.5V X6S 0402-3	C9995 20UF 20% 2.5V X6S 0402-3	C9996 20UF 20% 2.5V X6S 0402-3	C9997 20UF 20% 2.5V X6S 0402-3	C9998 20UF 20% 2.5V X6S 0402-3	C9999 20UF 20% 2.5V X6S 0402-3
C999A 20UF 20% 2.5V X6S 0402-3	C999B 20UF 20% 2.5V X6S 0402-3	C999C 20UF 20% 2.5V X6S 0402-3	C999D 20UF 20% 2.5V X6S 0402-3	C999E 20UF 20% 2.5V X6S 0402-3					
C995A 2.2UF 10% 10V X6S 0402	C995B 2.2UF 10% 10V X6S 0402	C995C 2.2UF 10% 10V X6S 0402	C995E 0.22UF 20% 6.3V X6S-CERM 0201	C995F 0.22UF 20% 6.3V X6S-CERM 0201	C995G 0.22UF 20% 6.3V X6S-CERM 0201	C995H 0.22UF 20% 6.3V X6S-CERM 0201			

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PCPU/GPU VRs: Output Caps

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5V_S2 VR

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5V_S2_PBUS-18V
PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12
PACK_OPTION=5V_S2_PBUS-25V_D2

136 PPVIN_P5VS2

CAPDERATE POLY-TANT CRITICAL
CC220 27UF 20% 18V TANT-POLY CASE-B12 128S00107
PACK_OPTION=5V_S2_PBUS-18V

CAPDERATE POLY-TANT CRITICAL
CC221 27UF 20% 18V TANT-POLY CASE-B12 128S00107

CAPDERATE POLY-TANT CRITICAL
CC220 33UF 20% 16V TANT CASE-T 128S00009
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-B12

CAPDERATE POLY-TANT CRITICAL
CC221 33UF 20% 16V TANT CASE-T 128S00009

CAPDERATE POLY-TANT CRITICAL
CC220 68UF 20% 6.3V POLY-TANT CASE-D2E-SM-1 128S0364
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-D2

CAPDERATE POLY-TANT CRITICAL
CC220 33UF 20% 16V TANT CASED12-SM 128S0436
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-D12

CAPDERATE POLY-TANT CRITICAL
CC220 22UF 20% 25V POLY-TANT CASED2-SM 128S0385
PACK_IGNORE=TRUE
PACK_OPTION=5V_S2_PBUS-25V_D2

CRITICAL CC261 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL CC262 2.2UF 20% 25V X6S-CERM 0402 138S00042

UC260 SN621371 VQFN CRITICAL 353S02228
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
DIDT=TRUE
SWITCH_NODE=TRUE

VIN	1	2	SW
EN	8	6	VOS
SS/TR	9	5	FB
VSEL	11	7	PG
MODE	10	4	FB2
GND		3	

141 54 EN P5VS2HOLD_PWR_EN
RC260 0 0% 1/20W TK 0201 117S00073
P5VS2_EN
P5VS2_SS
CC268 0.022UF 10% 50V X7R 0402 132S0423
XWC260 SM
54 P5VS2_AGND

P5VS2_SW
P5VS2_VOS
P5VS2_FB
P5VS2HOLD_PGOOD OUT 54 141

CRITICAL LC260 2.2UH-20%-4.5A-0.043OHM PIMA042T-SM 152S00182
XWC270 SM
P5VS2_FB_XW
RC290 15 5% 1/20W TK 0201 117S00111
P5VS2_FB_LPF
CC290 0.022UF 10% 50V X7R 0402 132S0423
RC270 0 0% 1/20W TK 0201 117S00073
RC271 5.49K 1% 1/20W TK 0201 118S00411
P5VS2_FB_R
CC269 220PF 5% 50V C0G 0201-1 131S00464
CRITICAL RC273 191K 0.1% 1/20W TK 0201 103S00630
CRITICAL RC272 30.9K 0.1% 1/20W TK 0201 103S00594
54 P5VS2_AGND

PP5V_S2_HOLD 54 135
CRITICAL CC270 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL CC271 2.2UF 20% 25V X6S-CERM 0402 138S00042
CAPDERATE POLY-TANT CRITICAL CC272 150UF 20% 6.3V TANT CASE-B-SM 128S00038
CAPDERATE POLY-TANT CRITICAL CC273 150UF 20% 6.3V TANT CASE-B-SM 128S00038

141 54 P5VS2HOLD_PGOOD — RC267 100K 5% 1/20W TK 0201 117S00095 — PP5V_S2_HOLD 135

Start up time
min=4.3ms
typ=6.4ms
max=8.81ms

VOUT=5.15V
EDC=3.0A
F=1.5MHz

Decay time to 0.1V
min=100ms
typ=132ms
max=166ms

141 54 IN P5VS2HOLD_PWR_EN
RC280 0 0% 1/20W TK 0201 117S00073
P5VS2_DSCHG_EN_L

135 PP3V8_AON
RC281 100K 5% 1/20W TK 0201 117S00095
P5VS2_DSCHG_EN
CRITICAL QC280 SSM6N15AFEAP SOT563 376S00074
VER-2
CC280 27PF 5% 25V C0G 0201 131S0804 NOSTUFF

135 54 PP5V_S2_HOLD
RC282 220 5% 1/16W TK 0402 116S00028
RC283 220 5% 1/16W TK 0402 116S00028
P5VS2_DSCHG
CRITICAL QC280 SSM6N15AFEAP SOT563 376S00074
VER-2

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: 5V S2

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
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BRANCH: dvt-2
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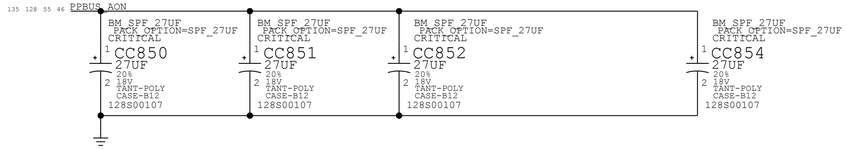
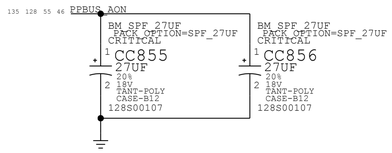
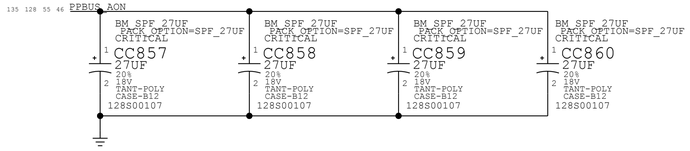
rdar://107394268 (EVTs: Delete CC853 to accommodate L5230 stiffener)







BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
SPF 27UF Caps

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REVISION 4.0.0
BRANCH dvt-2
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AP_I2C0 (unused)

ATC0,1,2 and Magsafe SPMI/I2C ADDRESSES

rdar://101044821 (s: Add SPMI/I2C addresses text in schematic to ATC0,1,2 and Magsafe)

UPC5: CSA 55

pins N25/M24 (SPMI_I2C2_DATA/CLK)
SMC SPMI: 0x7
AP SPMI: 0x6
I2C: 0x3C

UPC1: CSA 155

pins N25/M24 (SPMI_I2C2_DATA/CLK)
SMC SPMI: 0xB
AP SPMI: 0xA
I2C: 0x3F

UPC0: CSA 154

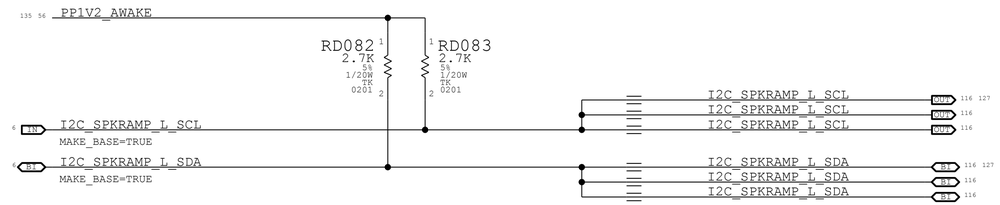
pins N25/M24 (SPMI_I2C2_DATA/CLK)
SMC SPMI: 0xD
AP SPMI: 0xC
I2C: 0x38

UPC2: CSA 164

pins N25/M24 (SPMI_I2C2_DATA/CLK)
SMC SPMI: 0x9
AP SPMI: 0x8
I2C: 0x3B

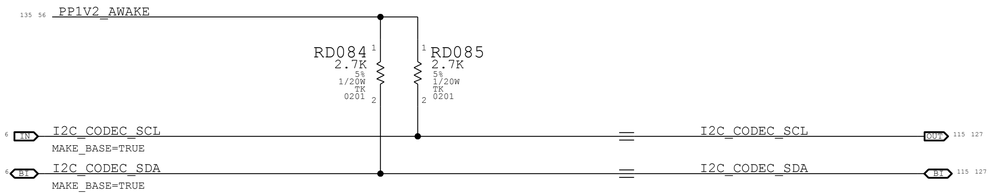
AP_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400kHz	0x38	0x70	SPKRAMP_TAWANG_A
AP	1	400kHz	0x39	0x72	SPKRAMP_TAWANG_B
AP	1	400kHz	0x3A	0x74	SPKRAMP_TAWANG_C



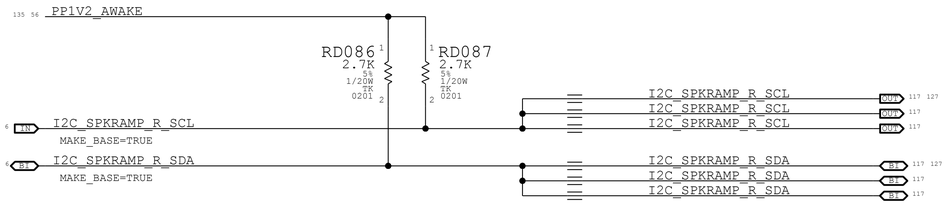
AP_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	400kHz	0x4B	0x95	CODEC - CARLOW (POR)



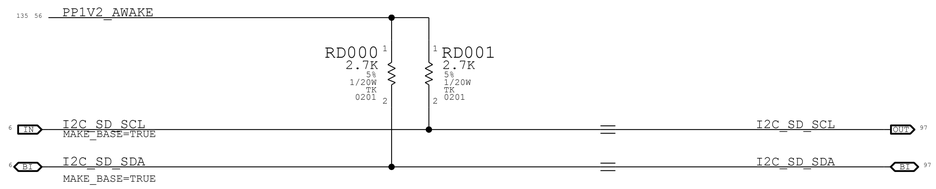
AP_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400kHz	0x3B	0x76	SPKRAMP_TAWANG_D
AP	3	400kHz	0x3C	0x78	SPKRAMP_TAWANG_E
AP	3	400kHz	0x3D	0x7A	SPKRAMP_TAWANG_F



AP_I2C4

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	4	100kHz	0x20	0x40	SDCARD



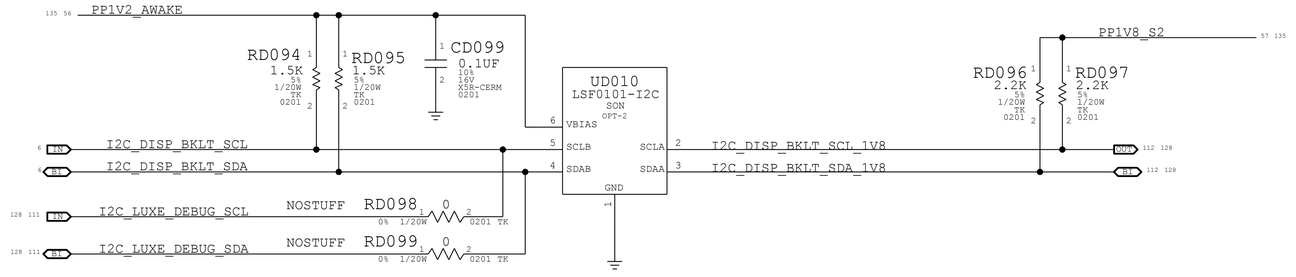
UNUSED:

AOP_I2C1
ISP_I2C0
ISP_I2C1
ISP_I2C3

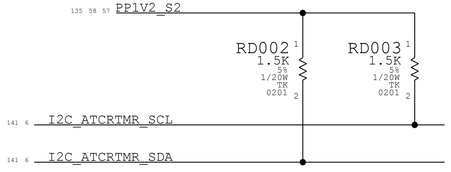
AP_I2C7

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	7	400kHz	0X44	0X88	Aveillino PMIC

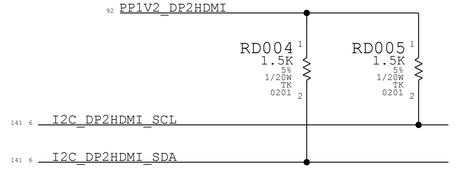
I2C is hooked up to testpoints on BCON brd



AP_I2C6



AP_I2C8



PAGE TITLE: I2C Connections - AP

Apple Inc.

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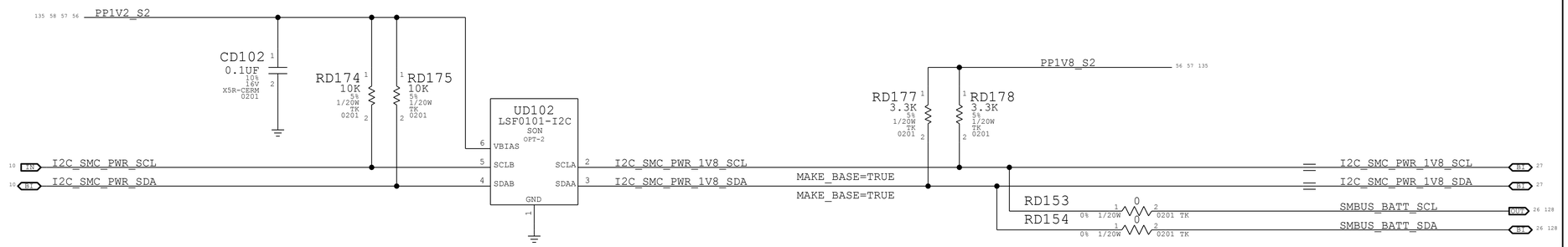
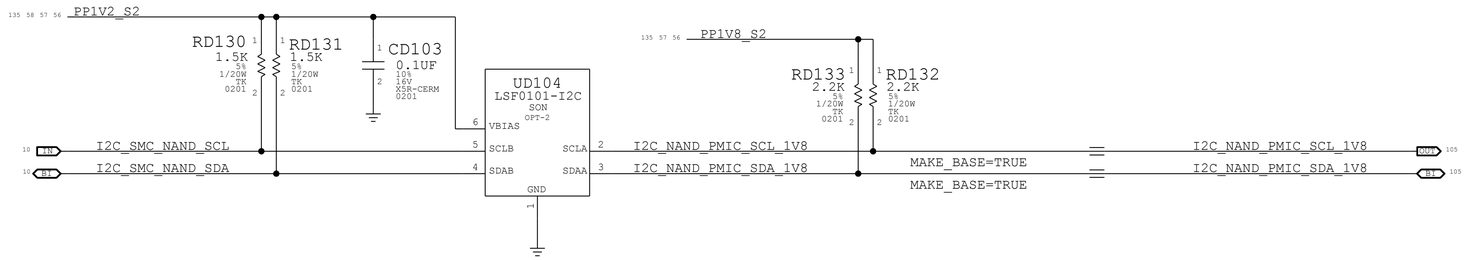
SMC_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	0	100kHz	0X09	0X12	CHARGER - MANDOLA
SMC	0	100kHz	0X0B	0X16	BMU



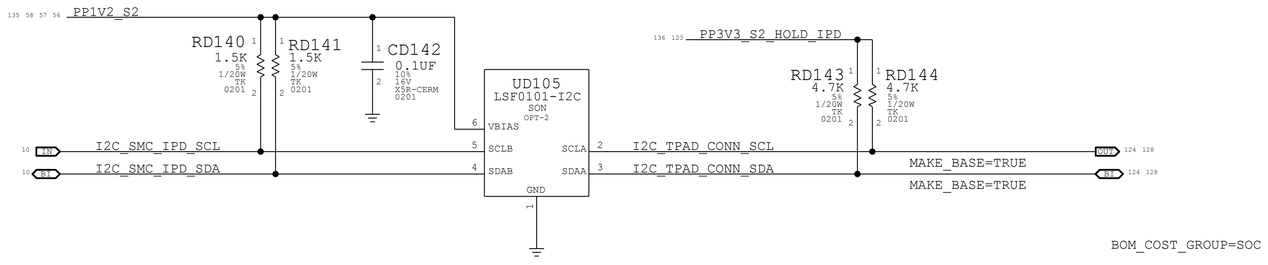
SMC_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100kHz	0X79	0XF2	NAND PMIC 0
SMC	2	100kHz	0X78	0XF0	NAND PMIC 1



SMC_I2C3

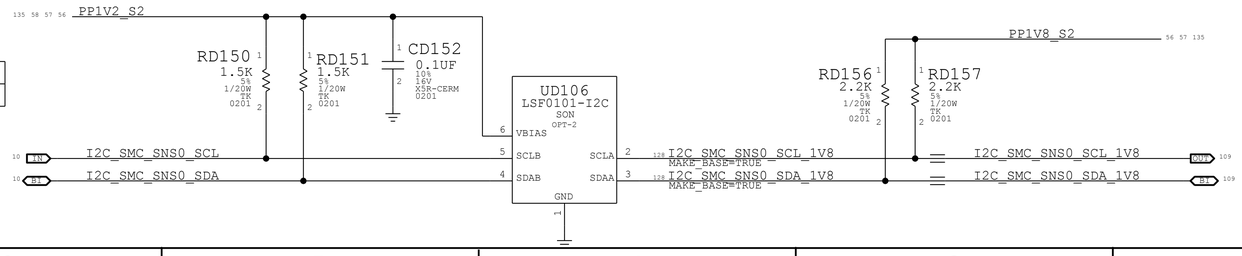
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100kHz	0X4C	0X98	PALM REST TEMP



BOM_COST_GROUP=SOC

SMC_I2C4

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	4	100kHz	0X48	0X90	Temp Sensors



PAGE TITLE: I2C Connections - SMC

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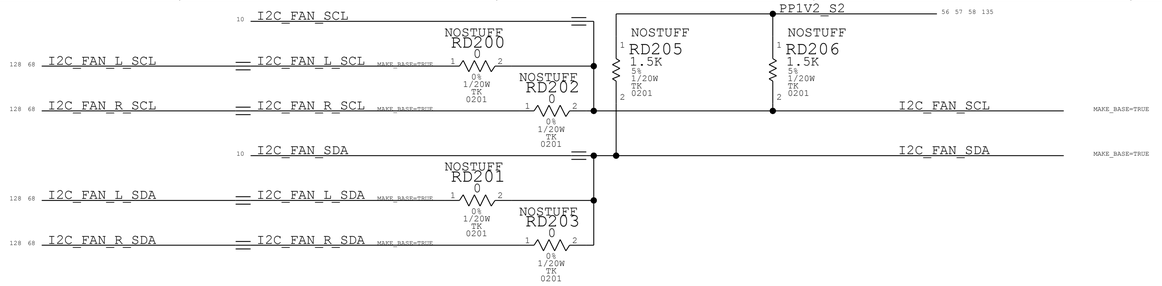
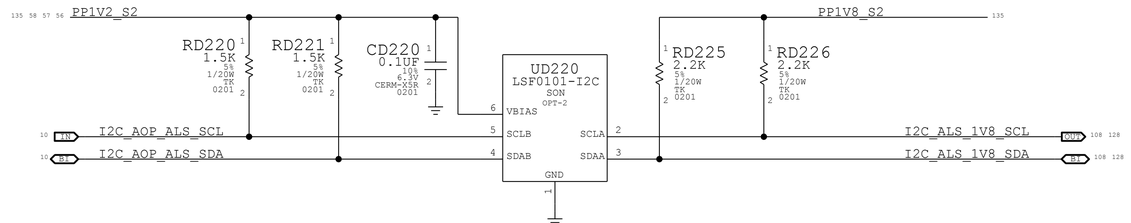
SMC_I2C0,6 (unused)



SMC_I2C5 (SNS1)

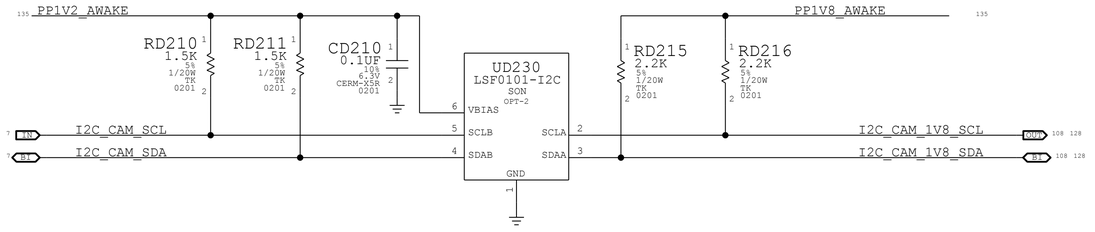
AOP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400kHz	0X29	0X52	ALS
AOP	0	400kHz	0X24	0X48	ALS Temp



ISP_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	2	400kHz	0X10	0X20	FHS1+
ISP	2	400kHz	0X6C	0XD8	Camera Sensor



UNUSED and already aliased
ISP_I2C0 SMC_I2C6
ISP_I2C1
ISP_I2C3
AOP_I2C1

SI2C

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
S	0	400kHz	0XXX	0XX	SEP EEPROM

Need to confirm if this needs/has pull-ups

MISSING WLAN/BT, R1, CELL - VENDOR CARDS

BOM_COST_GROUP=SOC

PAGE TITLE: I2C Connections - Other

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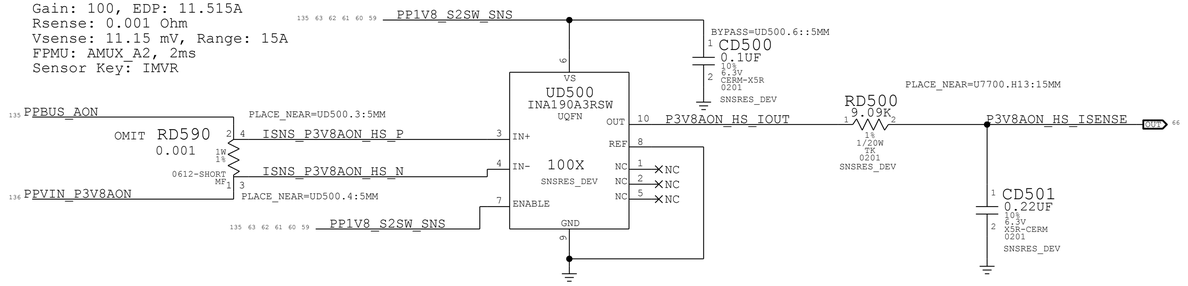
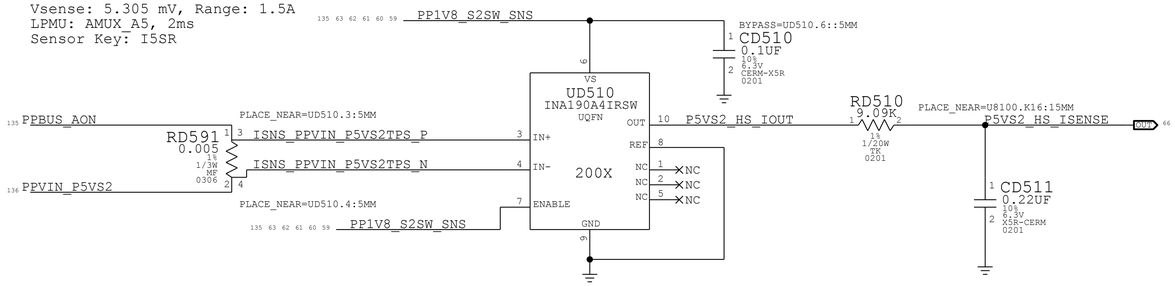
P3V8 AON HIGH SIDE ISENSE

Gain: 100, EDP: 11.515A
Rsense: 0.001 Ohm
Vsense: 11.15 mV, Range: 15A
FPMU: AMUX_A2, 2ms
Sensor Key: IMVR



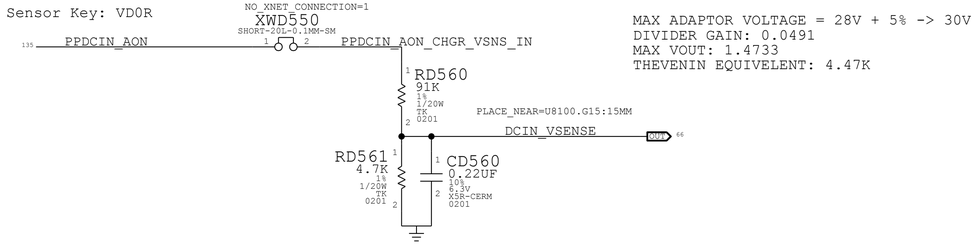
5V S2 VR HIGH SIDE ISENSE

Gain: 200, EDP: 1.061A
Rsense: 0.005 Ohm
Vsense: 5.305 mV, Range: 1.5A
LPMU: AMUX_A5, 2ms
Sensor Key: I5SR



DCIN VOLTAGE SENSE

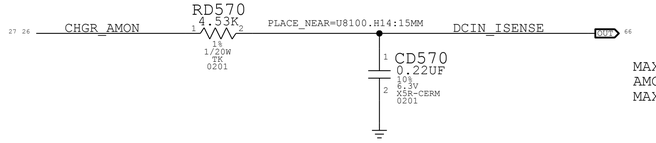
LPMU: AMUX_A1, 1ms
Sensor Key: VD0R



MAX ADAPTOR VOLTAGE = 28V + 5% -> 30V
DIVIDER GAIN: 0.0491
MAX VOUT: 1.4733
THEVENIN EQUIVELENT: 4.47K

DCIN ISENSE AMON

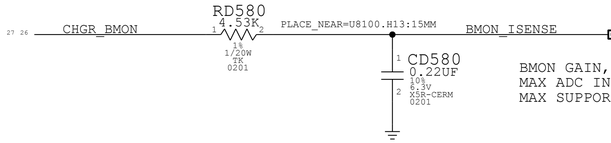
LPMU: AMUX_A0, 1ms
Sensor Key: ID0R



MAX ADAPTOR CURRENT: 5A
AMON GAIN, RSENSE: 20X, 10m
MAX AMON OUTPUT VOLTAGE: 1V

BATTERY ISENSE BMON

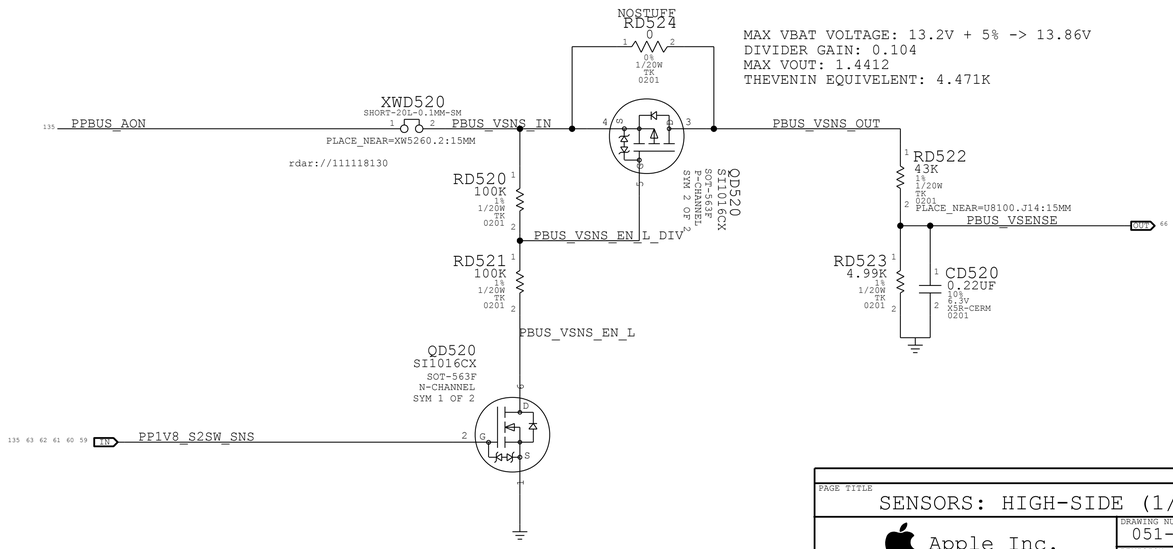
LPMU: AMUX_A2, 1ms
Sensor Key: IPBR



BMON GAIN, RSENSE: 7.9X, 5m
MAX ADC INPUT VOLTAGE: 1.5V (G=1)
MAX SUPPORTED BATTERY CURRENT SENSE: 37.97A

PBUS VOLTAGE SENSE (VP0R)

LPMU: AMUX_A3, 1ms



MAX VBAT VOLTAGE: 13.2V + 5% -> 13.86V
DIVIDER GAIN: 0.104
MAX VOUT: 1.4412
THEVENIN EQUIVELENT: 4.471K

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: HIGH-SIDE (1/3)

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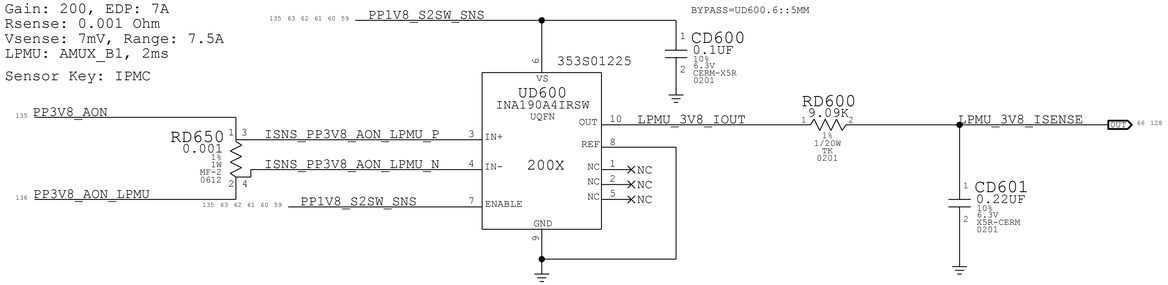
LPMU HIGH SIDE 3V8 ISENSE

Gain: 200, EDP: 7A
Rsense: 0.001 Ohm
Vsense: 7mV, Range: 7.5A
LPMU: AMUX_B1, 2ms

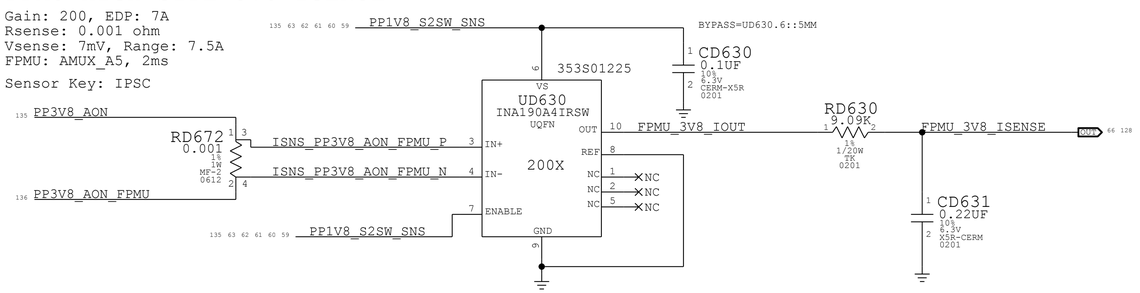
Sensor Key: IPMC



FPMU HIGH SIDE 3V8 ISENSE

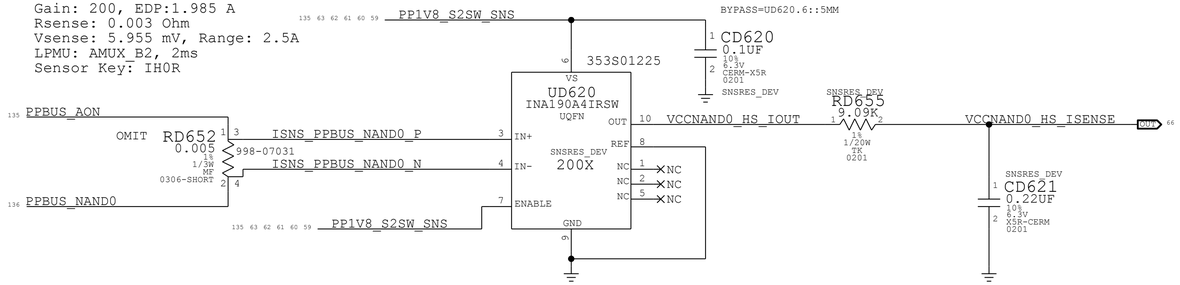
Gain: 200, EDP: 7A
Rsense: 0.001 ohm
Vsense: 7mV, Range: 7.5A
FPMU: AMUX_A5, 2ms

Sensor Key: IPSC



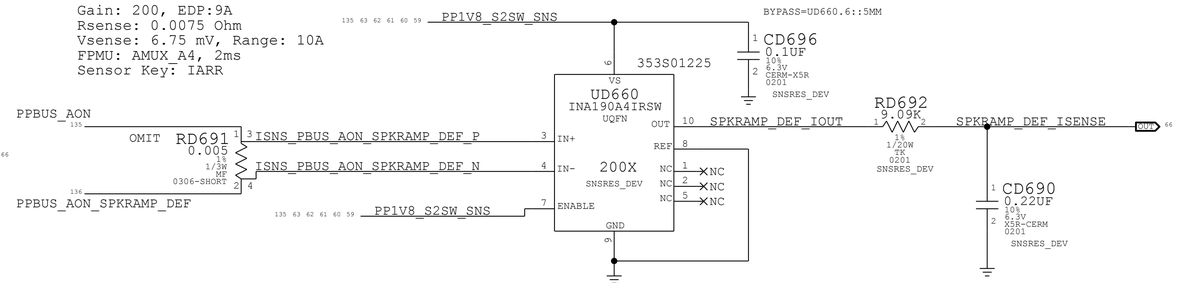
NAND 0 PBUS ISENSE

Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
LPMU: AMUX_B2, 2ms
Sensor Key: IH0R



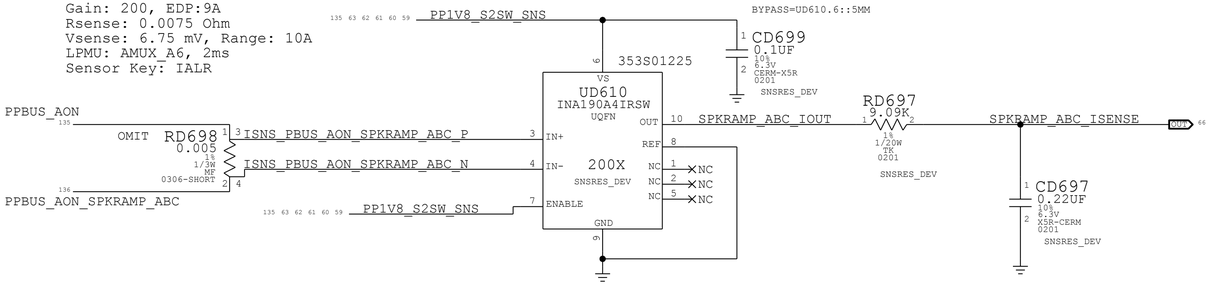
RIGHT SPKRAMP PBUS ISENSE

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
FPMU: AMUX_A4, 2ms
Sensor Key: IARR



LEFT SPKRAMP PBUS ISENSE

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
LPMU: AMUX_A6, 2ms
Sensor Key: IALR



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: HIGH-SIDE (2/3)

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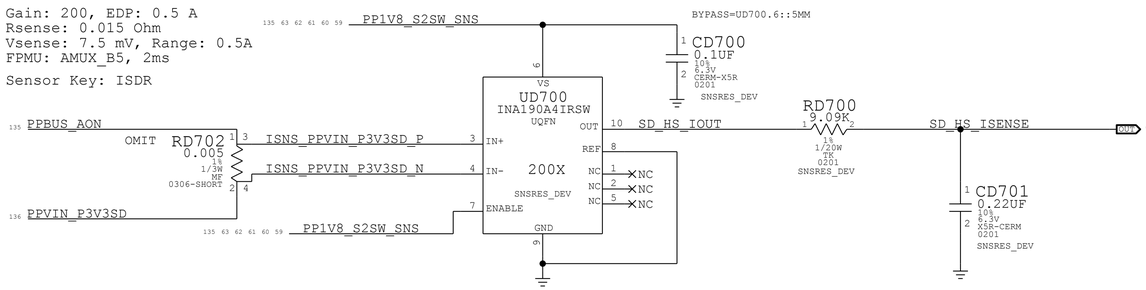
SD PBUS ISENSE

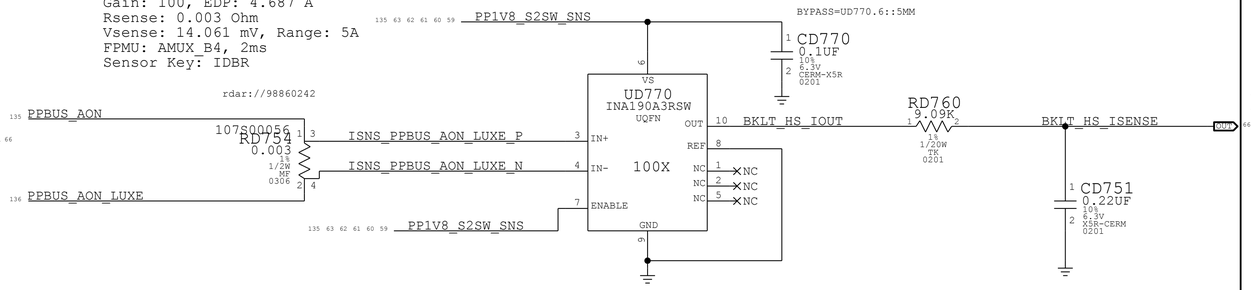
Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
FPMU: AMUX_B5, 2ms

Sensor Key: ISDR



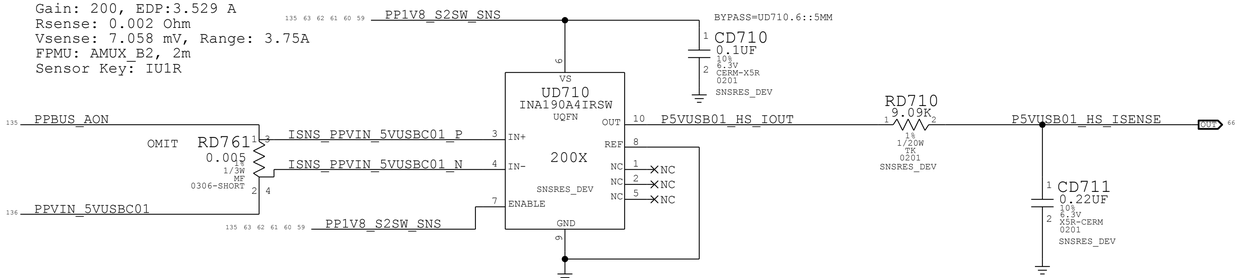
LCD BKLT (LUXE) ISENSE

Gain: 100, EDP: 4.687 A
Rsense: 0.003 Ohm
Vsense: 14.061 mV, Range: 5A
FPMU: AMUX_B4, 2ms
Sensor Key: IDBR



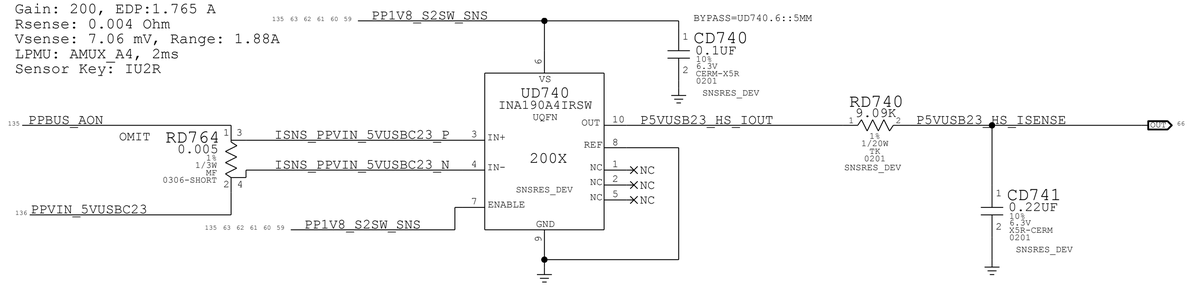
USB 5V OUT LEFT ISENSE

Gain: 200, EDP:3.529 A
Rsense: 0.002 Ohm
Vsense: 7.058 mV, Range: 3.75A
FPMU: AMUX_B2, 2m
Sensor Key: IU1R



USB 5V OUT RIGHT ISENSE

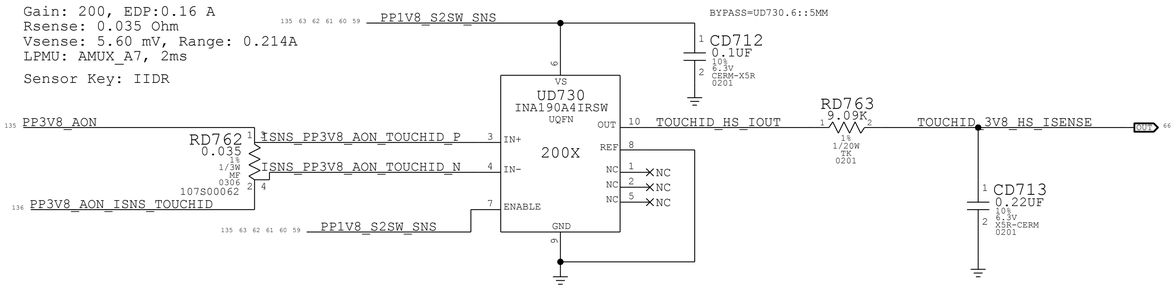
Gain: 200, EDP:1.765 A
Rsense: 0.004 Ohm
Vsense: 7.06 mV, Range: 1.88A
LPMU: AMUX_A4, 2ms
Sensor Key: IU2R



TOUCHID 3V8 ISENSE

Gain: 200, EDP:0.16 A
Rsense: 0.035 Ohm
Vsense: 5.60 mV, Range: 0.214A
LPMU: AMUX_A7, 2ms

Sensor Key: IIDR



PAGE TITLE
SENSORS: HIGH-SIDE(3/3)

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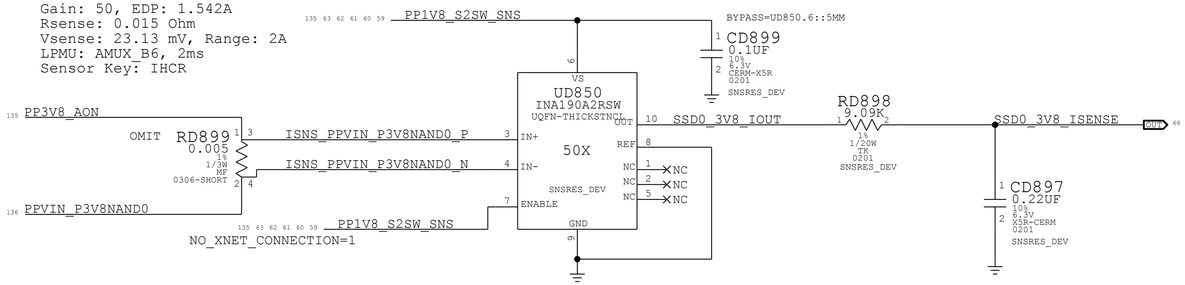
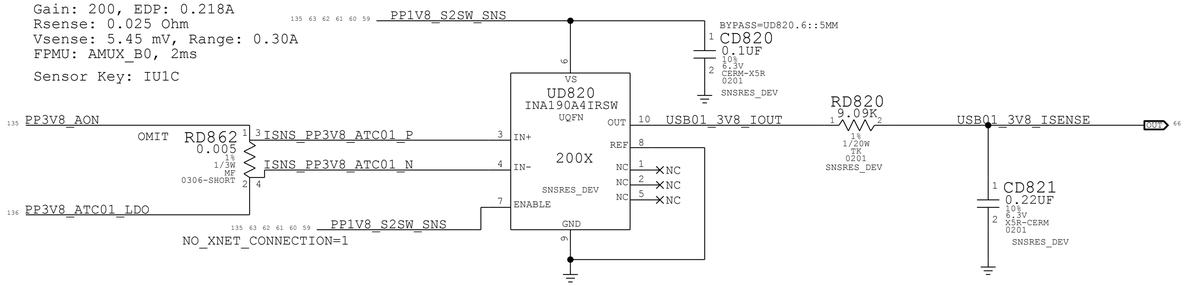
OCARINA 0 ISENSE

Gain: 50, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
LPMU: AMUX_B6, 2ms
Sensor Key: IHCR



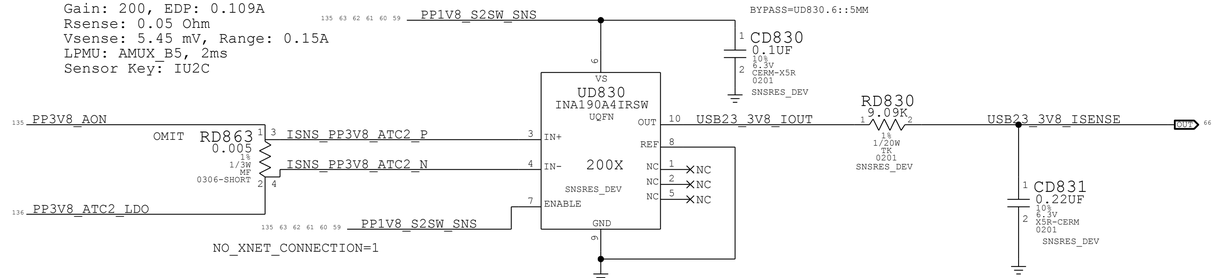
USB 3V8 LEFT ISENSE

Gain: 200, EDP: 0.218A
Rsense: 0.025 Ohm
Vsense: 5.45 mV, Range: 0.30A
FPMU: AMUX_B0, 2ms
Sensor Key: IU1C



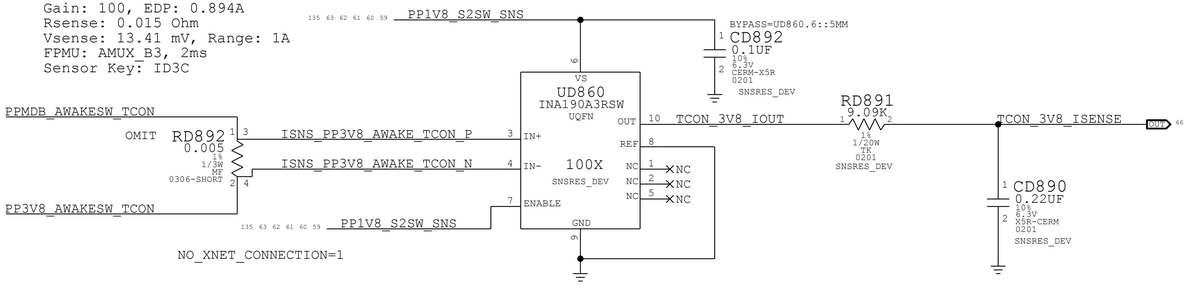
USB 3V8 RIGHT ISENSE

Gain: 200, EDP: 0.109A
Rsense: 0.05 Ohm
Vsense: 5.45 mV, Range: 0.15A
LPMU: AMUX_B5, 2ms
Sensor Key: IU2C



DISPLAY (TCON) 3V8 ISENSE

Gain: 100, EDP: 0.894A
Rsense: 0.015 Ohm
Vsense: 13.41 mV, Range: 1A
FPMU: AMUX_B3, 2ms
Sensor Key: ID3C



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: LOW-SIDE (1/3)

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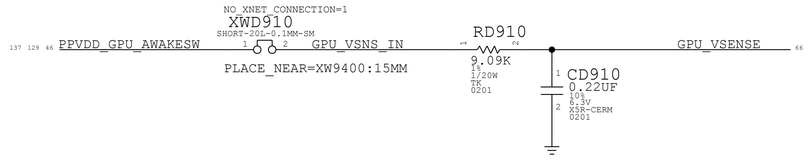
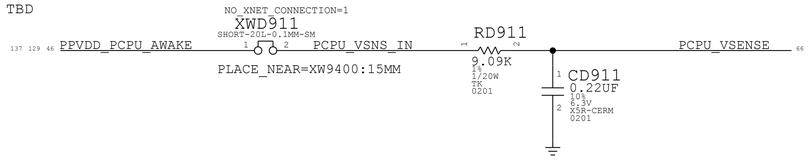
GPU VSENSE

FPMU:AMUX_B1,2ms
RANGE:0.4V - 1.3V
Sensor Key: TBD



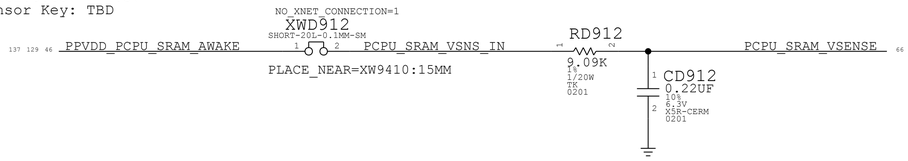
PCPU VSENSE

LPMU:AMUX_B3,2ms
RANGE:0.4V - 1.3V
Sensor Key: TBD



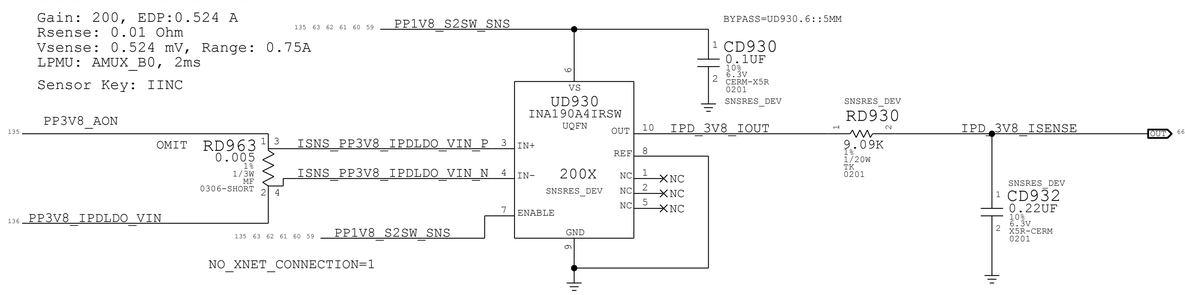
PCPU SRAM VSENSE

LPMU:AMUX_B7,2ms
RANGE:0.65V - 1.3V
Sensor Key: TBD



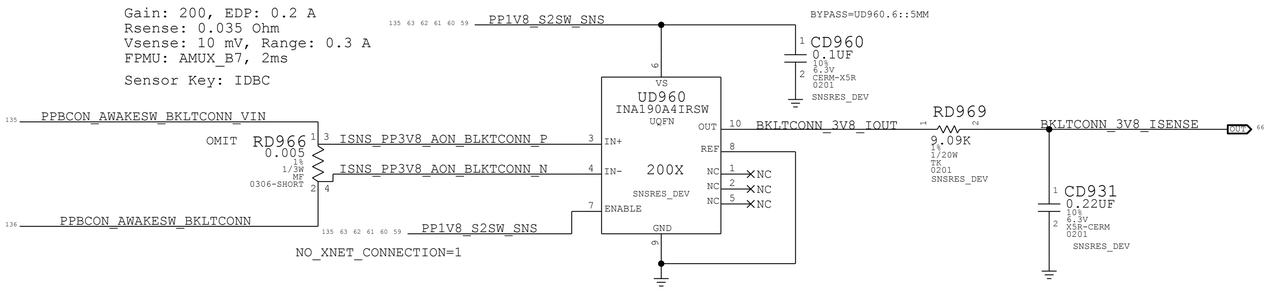
IPD 3V8 ISENSE

Gain: 200, EDP:0.524 A
Rsense: 0.01 Ohm
Vsense: 0.524 mV, Range: 0.75A
LPMU: AMUX_B0, 2ms
Sensor Key: IINC



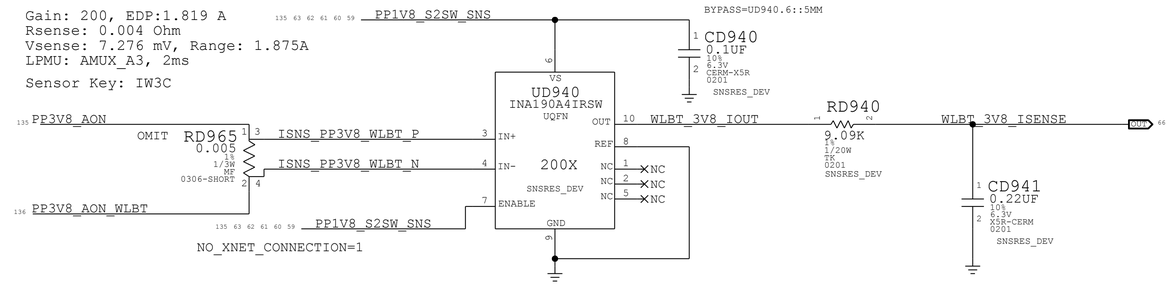
DISPLAY BACKLIGHT 3V8 ISENSE

Gain: 200, EDP: 0.2 A
Rsense: 0.035 Ohm
Vsense: 10 mV, Range: 0.3 A
FPMU: AMUX_B7, 2ms
Sensor Key: IDBC



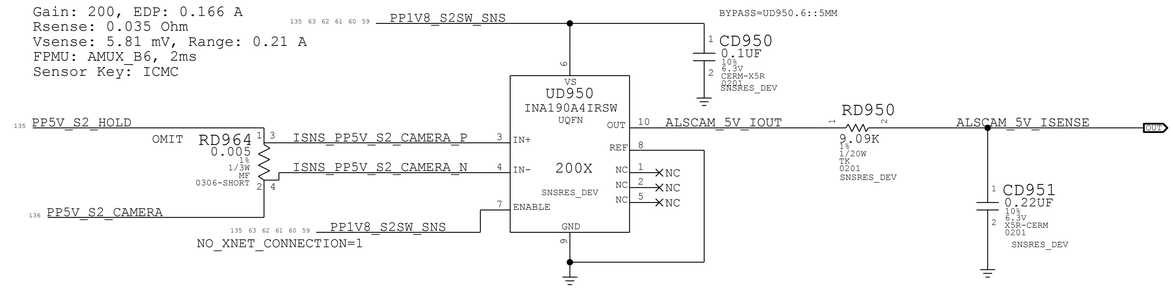
WLAN BT 3V8 ISENSE

Gain: 200, EDP:1.819 A
Rsense: 0.004 Ohm
Vsense: 7.276 mV, Range: 1.875A
LPMU: AMUX_A3, 2ms
Sensor Key: IW3C



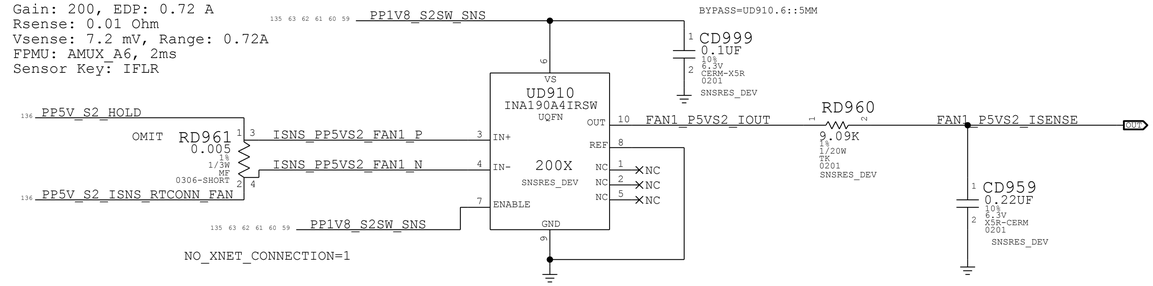
CAMERA/ALS 5V ISENSE

Gain: 200, EDP: 0.166 A
Rsense: 0.035 Ohm
Vsense: 5.81 mV, Range: 0.21 A
FPMU: AMUX_B6, 2ms
Sensor Key: ICMC



Right Fan (FAN1) ISENSE

Gain: 200, EDP: 0.72 A
Rsense: 0.01 Ohm
Vsense: 7.2 mV, Range: 0.72A
FPMU: AMUX_A6, 2ms
Sensor Key: IFLR



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: LOW-SIDE (2/3)

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GPU phase sense resistors

PPVDD_GPU_AWAKESW LOW SIDE ISENSE (SUMMING AMP FOR 3 PHASES)

EDP: 80A, 30A/P0-P4, 25A/P5, 25A/P6

Gain:113
FPMU: AMUX_A1, 2ms

PPVDD_GPU_AWAKESW_REGINT
PPVDD_GPU_AWAKESW_REGEXT5
PPVDD_GPU_AWAKESW_REGEXT6
PPVDD_GPU_AWAKESW

RE060 0.0005 0612-2 MF 1W 1% NO_XNET_CONNECTION=1
RE061 0.0005 0612-2 MF 1W 1% NO_XNET_CONNECTION=1
RE062 0.0005 0612-2 MF 1W 1% NO_XNET_CONNECTION=1

GPU_RISNS1_P → RE017 10K → GPU_RISNS_IN_P_R
GPU_RISNS2_P → RE018 10K
GPU_RISNS3_P → RE019 10K
RE020 2K → GPU_RISNS_IN_P
RE021 604K NO_XNET_CONNECTION=1

PP3V8_AON → UE022 353S1429 OPA333DCKG4 SC70-5-COMBO (V+, V-)
BYPASS=UE022.5::5MM
CE023 0.1UF 10% 6.3V CERM-X5R 0201

GPU_ISENSE_EXT
GPU_RISNS1_N → RE024 10K → GPU_RISNS_IN_N_R
RE025 2K → GPU_RISNS_IN_N
RE026 604K NO_XNET_CONNECTION=1
RE048 9.09K → GPU_ISENSE_EXT_R
RE051 0 → GPU_ISENSE
CE029 0.22UF 10% 6.3V X5R-CERM 0201
GPU_RISNS2_N → RE030 10K
GPU_RISNS3_N → RE031 10K

PPVDD_PCPU_AWAKESW LOW SIDE ISENSE (SUMMING AMP FOR 2 PHASES)

EDP: 70A, 30A/P0-P4, 25A/P5

PCPU phase sense resistors

PPVDD_PCPU_AWAKE_REGINT
PPVDD_PCPU_AWAKE_REGEXT5
PPVDD_PCPU_AWAKE

RE063 0.0005 0612-2 MF 1W 1% NO_XNET_CONNECTION=1
RE064 0.0005 0612-2 MF 1W 1% NO_XNET_CONNECTION=1

PCPU_RISNS1_P → RE070 12.6K → PCPU_RISNS_IN_P_R
PCPU_RISNS2_P → RE071 12.6K
RE075 750 → PCPU_RISNS_IN_P
RE079 604K NO_XNET_CONNECTION=1

PP3V8_AON → UE070 353S1429 OPA333DCKG4 SC70-5-COMBO (V+, V-)
BYPASS=UE070.5::5MM
CE070 0.1UF 10% 6.3V CERM-X5R 0201

Gain: 85.7
SPMU:AMUX_A0,2ms
SENSOR KEY: TBD

PCPU_ISENSE_EXT
PCPU_RISNS1_N → RE072 12.6K → PCPU_RISNS_IN_N_R
PCPU_RISNS2_N → RE073 12.6K
RE074 750 → PCPU_RISNS_IN_N
RE076 604K NO_XNET_CONNECTION=1
RE077 9.09K → PCPU_ISENSE_EXT_R
RE078 0 → PCPU_ISENSE
CE078 0.22UF 10% 6.3V X5R-CERM 0201

PCPU SRAM sense resistor

PPVDD_PCPU_SRAM_AWAKE_REGINT
PPVDD_PCPU_SRAM_AWAKE

RE065 0.002 0612 TFT 1W 1%

PCPU_SRAM_RISNS3_P → RE095 6.19K → PCPU_SRAM_RISNS_IN_P
RE099 604K NO_XNET_CONNECTION=1

PP3V8_AON → UE090 353S1429 OPA333DCKG4 SC70-5-COMBO (V+, V-)
BYPASS=UE090.5::5MM
CE090 0.1UF 10% 6.3V CERM-X5R 0201

PCPU_SRAM_ISENSE_EXT
PCPU_SRAM_RISNS3_N → RE094 6.19K → PCPU_SRAM_RISNS_IN_N
RE096 604K NO_XNET_CONNECTION=1
RE097 9.09K → PCPU_SRAM_ISENSE_EXT_R
RE098 0 → PCPU_SRAM_ISENSE
CE098 0.22UF 10% 6.3V X5R-CERM 0201

PCPU SRAM ISENSE

Gain: 97.57, EDP:7 A
Rsense: 0.002 Ohm
Vsense: 14 mV
SPMU:AMUX_A7,2ms

P3V8AON_ISENSE_EXT → RE053 9.09K → P3V8AON_ISENSE_EXT_R
RE056 0 → P3V8AON_ISENSE
CE030 0.22UF 10% 6.3V X5R-CERM 0201
PLACE_NEAR=U8100.N14:15MM

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (3/3)

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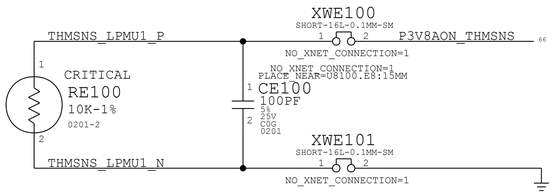
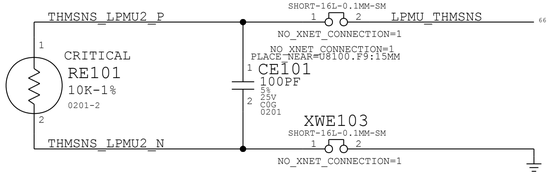
LPMU TDEV1

Sensor Key: TMVR
Location: Iceman Prox



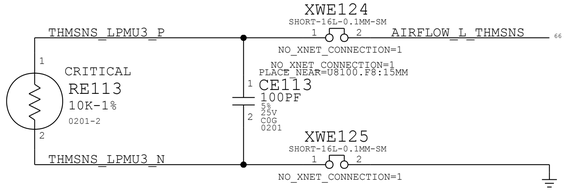
LPMU TDEV2

Sensor Key: TPMP
Location: Main PMU Prox



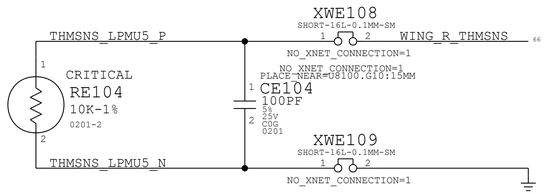
LPMU TDEV3

Sensor Key: TaLW
Location:Left Wing Airflow Prox



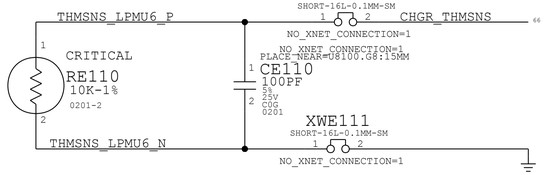
LPMU TDEV5

Sensor Key: TaRT
Location: Right Wingtip Prox



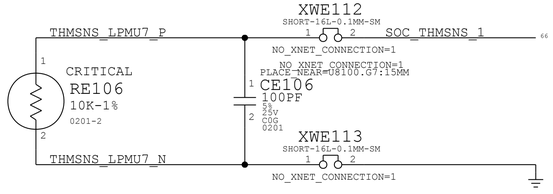
LPMU TDEV6

Sensor Key: TCHP
Location: Charger IC Prox



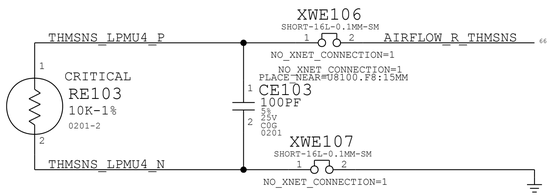
LPMU TDEV7

Sensor Key: TS0P
Location: SoC Prox



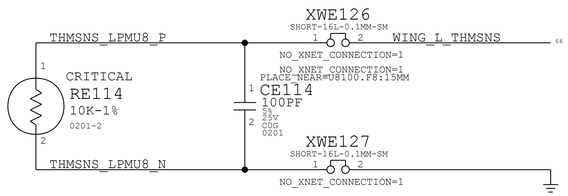
LPMU TDEV3

Sensor Key: TaLW
Location:Left Wing Airflow Prox



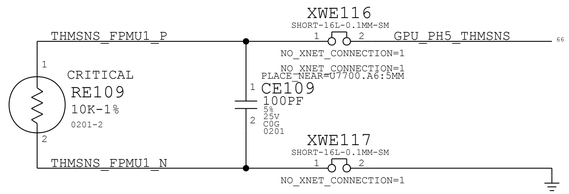
LPMU TDEV7

Sensor Key: TS0P
Location: SoC Prox



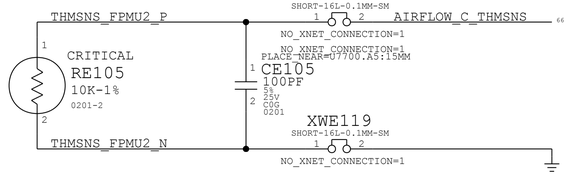
FPMU TDEV1

Sensor Key: TBD
Location: GPU Ekara #1 Prox



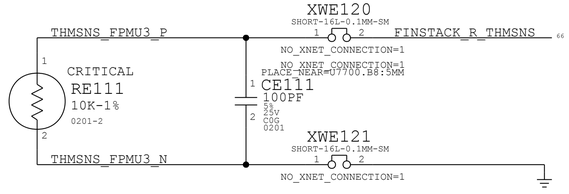
FPMU TDEV2

Sensor Key: TaTP
Location: Spitfire GPU Internal phases Prox



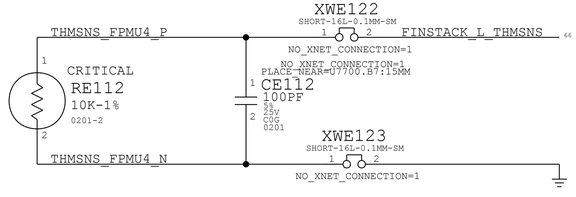
FPMU TDEV3

Sensor Key: TaRF
Location: Right Fan Intake Prox



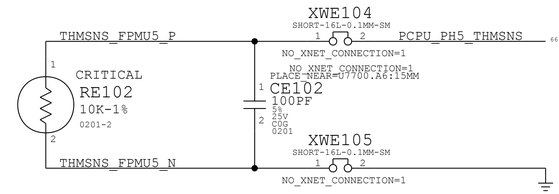
FPMU TDEV3

Sensor Key: TaRF
Location: Right Fan Intake Prox



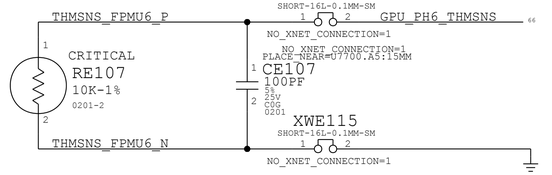
FPMU TDEV5

Sensor Key: TBD
Location: CPU Spitfire Ekara Prox



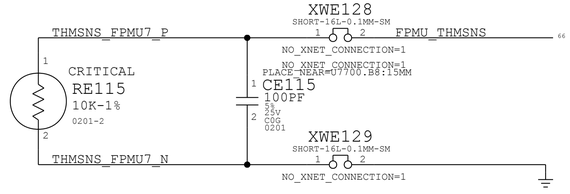
FPMU TDEV6

Sensor Key: TBD
Location: GPU Ekara #2 Prox



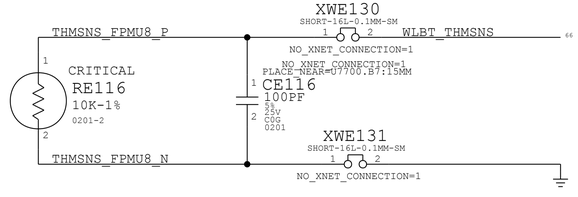
FPMU TDEV7

Sensor Key: TPSP
Location: Secondary PMU Prox



FPMU TDEV7

Sensor Key: TPSP
Location: Secondary PMU Prox



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: THERMAL

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
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SHEET 65 OF 156

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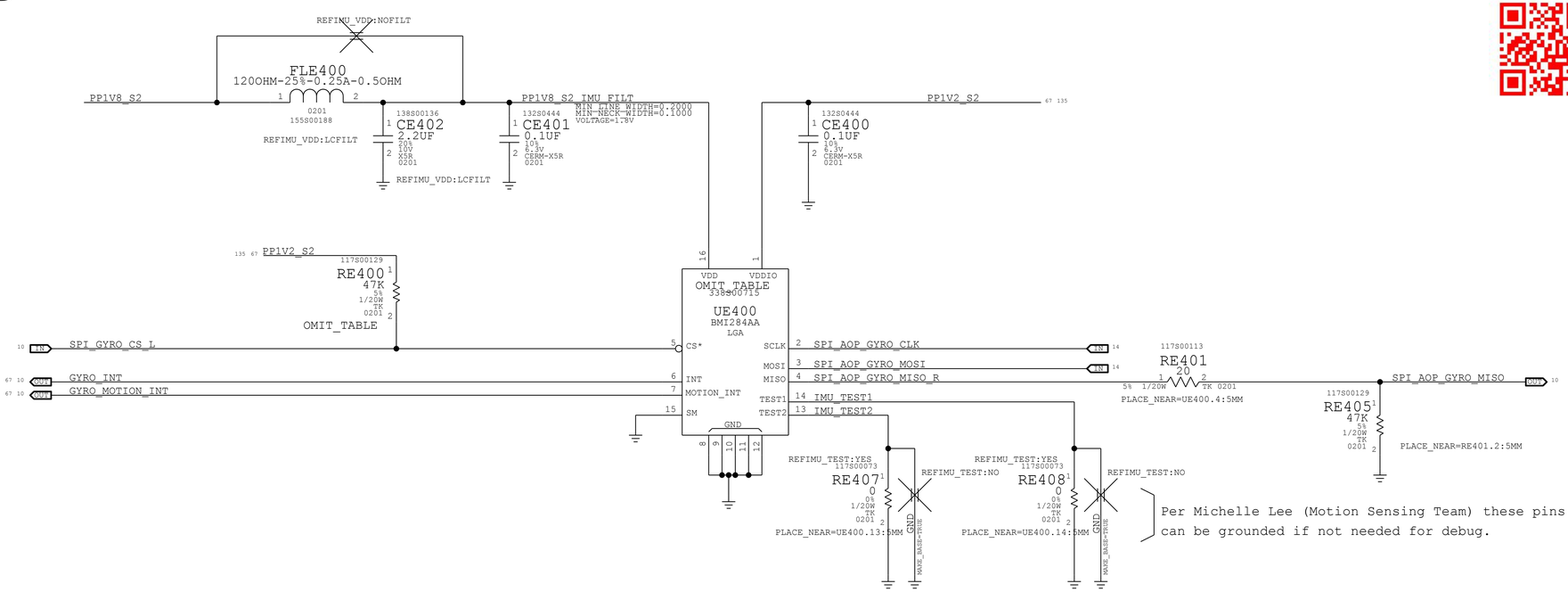
| | | |

*** OK2INTEGRATE ***

A Sovereign Accelerometer and Gyroscope

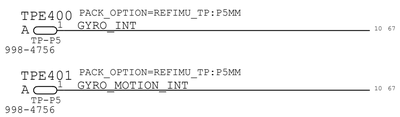
Datasheet Radar:



Per Michelle Lee (Motion Sensing Team) these pins can be grounded if not needed for debug.

MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points



C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI286
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400:30K

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: MOTION

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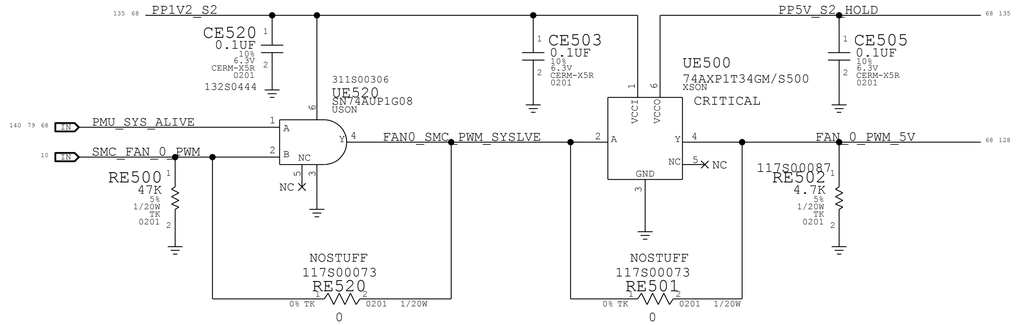
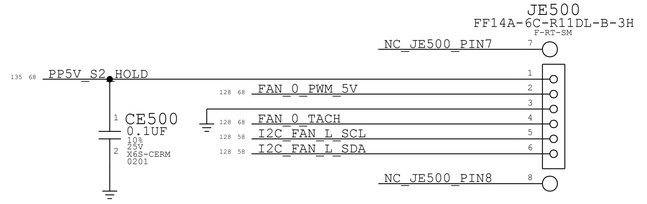
FAN CONTROLLERS

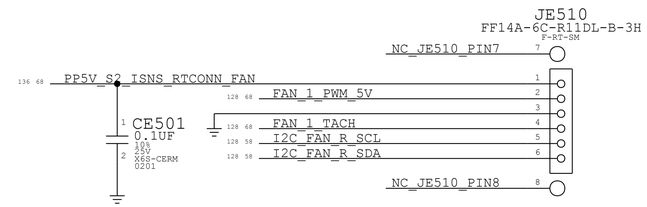
FAN PWM LEVEL SHIFTER

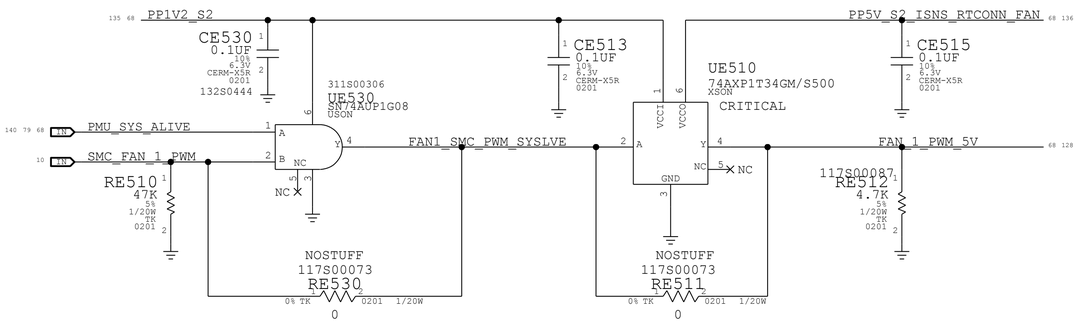


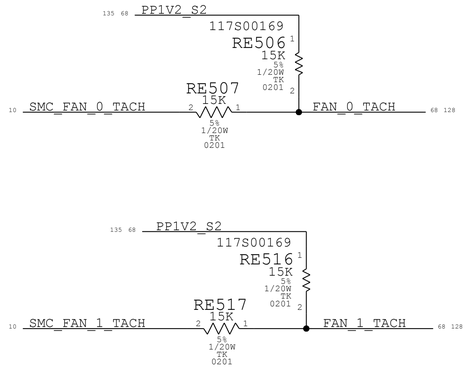
PWM FAN0(LEFT) CONNECTOR



PWM FAN1(RIGHT) CONNECTOR







*DUMMY FAN TO PLUG INTO EITHER POR FAN CONNECTORS JE500 OR JE510

BOM_COST_GROUP=FANS

PAGE TITLE: Fans

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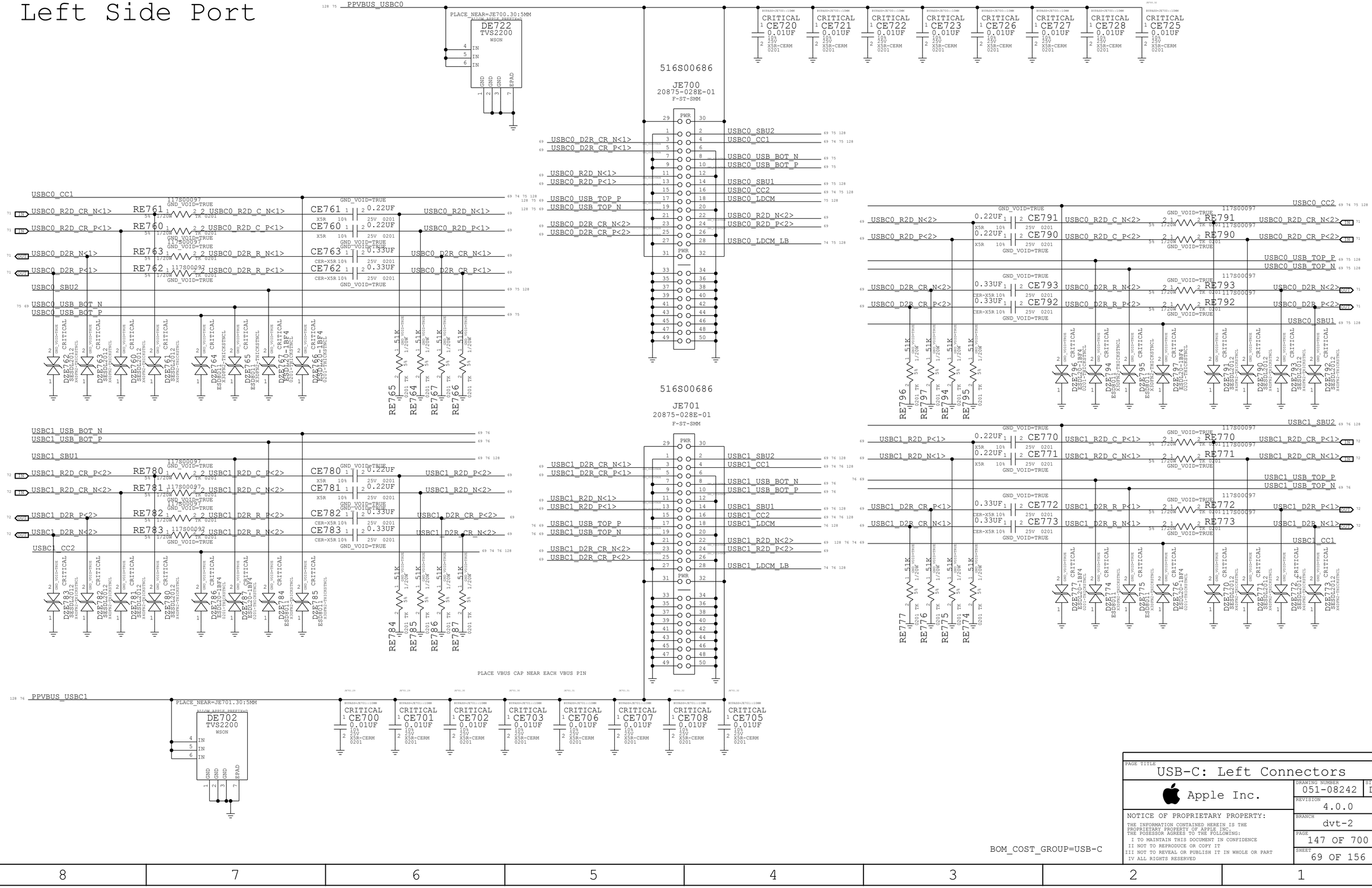
Left Side Port



PAGE TITLE	USB-C: Left Connectors
	Apple Inc.
DRAWING NUMBER	051-08242
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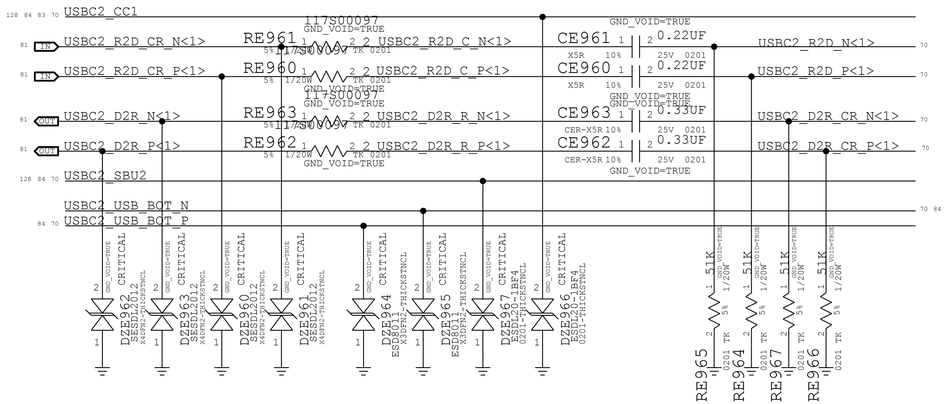
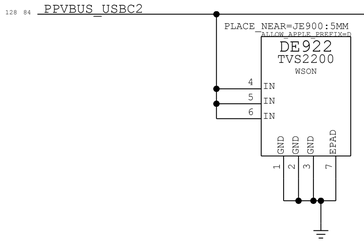
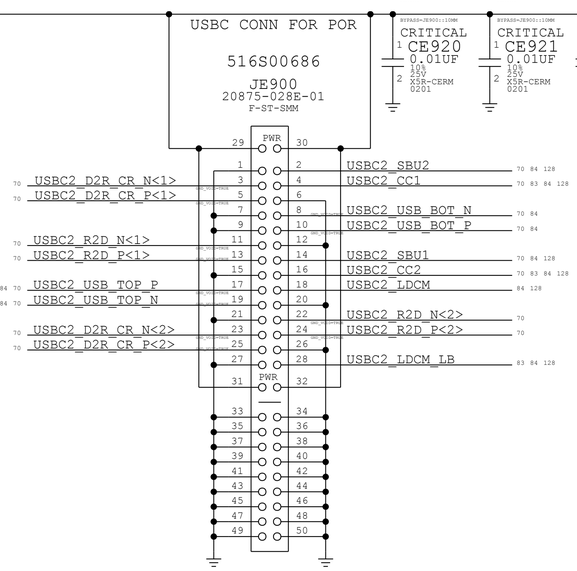
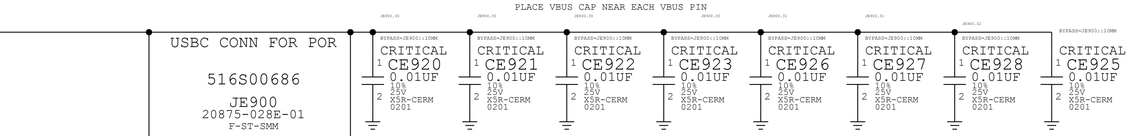
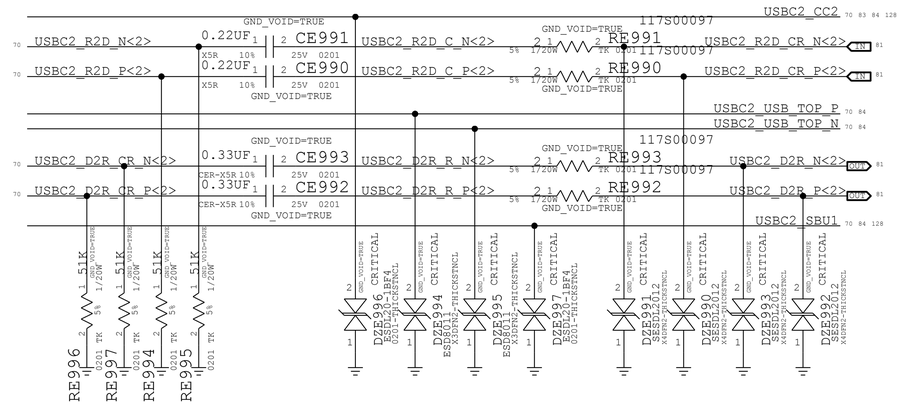
Right Side Port











BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Right Connector

Apple Inc.

DRAWING NUMBER: 051-08242 | SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

PP1V2_S2

RF062 1.5K 0201 TK 5% 1/20W — I2C_UPC0_ATCRTMR0_SCL
RF063 1.5K 0201 TK 5% 1/20W — I2C_UPC0_ATCRTMR0_SDA

RF043 1/20W 5% 47K TK 0201 — CIO_ATC0_LSTX
RF044 1/20W 5% 47K TK 0201 — CIO_ATC0_LSRX

CF011 10PF 5% 25V C0G 0201 — RF011 200 1% 1/20W TK 0201 — ATCRTMR0_CFP_RCAL_POS
CF010 10PF 5% 25V C0G 0201 — RF010 200 1% 1/20W TK 0201-1 — ATCRTMR0_SFP_RCAL_POS

ATCRTMR0_CFP_RCAL_NEG
ATCRTMR0_SFP_RCAL_NEG

USBC HIGH-SPEED AC COUPLING

USBC_ATC0_R2D_C_P<1>	CF020 0.22UF	USBC_ATC0_R2D_P<1>	GND_VOID=TRUE
USBC_ATC0_R2D_C_N<1>	CF021 0.22UF	USBC_ATC0_R2D_N<1>	GND_VOID=TRUE
USBC_ATC0_R2D_C_P<2>	CF024 0.22UF	USBC_ATC0_R2D_P<2>	GND_VOID=TRUE
USBC_ATC0_R2D_C_N<2>	CF025 0.22UF	USBC_ATC0_R2D_N<2>	GND_VOID=TRUE
USBC_ATC0_D2R_P<1>	CF022 0.22UF	USBC_ATC0_D2R_C_P<1>	GND_VOID=TRUE
USBC_ATC0_D2R_N<1>	CF023 0.22UF	USBC_ATC0_D2R_C_N<1>	GND_VOID=TRUE
USBC_ATC0_D2R_P<2>	CF026 0.22UF	USBC_ATC0_D2R_C_P<2>	GND_VOID=TRUE
USBC_ATC0_D2R_N<2>	CF027 0.22UF	USBC_ATC0_D2R_C_N<2>	GND_VOID=TRUE

All: 0.22UF 10% 6.3V X5R 0201

ATCRTMR0_XTAL24M_OUT — RF060 499 1% 1/20W TK 0201 — ATC0_24M_O_R — YF000 197S0591 CRITICAL 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM — ATCRTMR0_XTAL24M_IN
CF060 15PF 5% 50V C0G 0201
CF061 131S0831 CRITICAL 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR01_VDD_CIO
CF030 14UF 20% 4V X5R 0402-D2X-1
CF031 14UF 20% 4V X5R 0402-D2X-1
138S00149
CF032 0.1UF 10% 6.3V X6S 0201
CF033 0.1UF 10% 6.3V X6S 0201

UF000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 2 OF 2

VDD_CIO_0	J4	VDDIO12_CIO_0	K5
VDD_CIO_0	J6	VDDIO12_CIO_0	K7
VDD_CIO_0	J8	VDDIO12_CIO_0	L6
VDD_CIO_1	F4	VDDIO12_CIO_1	D6
VDD_CIO_1	F6	VDDIO12_CIO_1	E5
VDD_CIO_1	F8	VDDIO12_CIO_1	E7
		VDDIO12_PLL_SOC0	K8
		VDDIO12_PLL_SOC1	H8
		VDDIO12_XTAL	H9
		VDDIO12	E9
		VDDIO12	H3
		VDDIO12	K9
VDD_FIXED	G4		
VDD_FIXED	G5		
VDD_FIXED	H5		
VDD_FIXED	H6		
VDD_FIXED_PLL	G7	VDDIO12_EFUSE1	F3
VDD_FIXED_XTAL	G9	VDDIO12_AMUX	F7

OMIT_TABLE CRITICAL

VSS: A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8

VSS: H4, H7, J2, J3, J5, J7, J10, K4, K6, L1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11

PP1V2_ATCRTMR01_VDDIO
132S0395 CF034 0.1UF 10% 6.3V X6S 0201
138S00039 CF035 2.2UF 20% 4V X6S-CERM 0201
CF036 14UF 20% 4V X5R 0402-D2X-1
CF037 14UF 20% 4V X5R 0402-D2X-1

PP1V2_ATCRTMR01_VDDIO
138S00039 CF052 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF000.K8:5MM
PP1V2_ATCRTMR0_VDDIO_XTAL_R — VOLTAGE=1.2V — 155S0644 FLF000 240-OHM-0.2A-0.9-OHM — PP1V2_ATCRTMR01_VDDIO
CF062 0.1UF 10% 6.3V X6S 0201 — 132S0395
CF063 2.2UF 20% 4V X6S-CERM 0201 — 138S00039

PP0V805_ATCRTMR01_VDD_FIXED
CF040 0.1UF 10% 6.3V X6S 0201
CF041 0.1UF 10% 6.3V X6S 0201
CF042 2.2UF 20% 4V X6S-CERM 0201
CF043 2.2UF 20% 4V X6S-CERM 0201
CF044 2.2UF 20% 4V X6S-CERM 0201
CF045 14UF 20% 4V X5R 0402-D2X-1
CF046 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR01_VDD_FIXED
CF050 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF000.G7:5MM

Connect to GND directly or via a resistor
GND

PP1V2_ATCRTMR01_VDDIO
132S0395 CF064 0.1UF 10% 6.3V X6S 0201

PPVDD_FIXED_ATCRTMR0_XTAL_R
PP0V805_ATCRTMR01_VDD_FIXED
RF051 10 1/20W TK 0201 — VOLTAGE=0.805V
117S00094
CF051 4UF 20% 2.5V X6S 0201 — 138S00329

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF045 47K 1/20W TK 0201 — ATCRTMR0_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RF047 47K 1/20W TK 0201 — ATCRTMR0_JTAG_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF040 10K 5% 1/20W TK 0201 — ATCRTMR0_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

UF000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 1 OF 2 — OMIT_TABLE CRITICAL

USBC_ATC0_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP PHY	CFP_PHY_RXTX_0_P — USBC0_R2D_CR_P<1>
USBC_ATC0_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N			CFP_PHY_RXTX_0_N — USBC0_R2D_CR_N<1>
USBC_ATC0_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P			CFP_PHY_RXTX_2_P — USBC0_R2D_CR_P<2>
USBC_ATC0_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N			CFP_PHY_RXTX_2_N — USBC0_R2D_CR_N<2>
USBC_ATC0_R2D_P<1>	P7	SFP_PHY_RXTX_1_P			CFP_PHY_RXTX_1_P — USBC0_D2R_P<1>
USBC_ATC0_R2D_N<1>	N7	SFP_PHY_RXTX_1_N			CFP_PHY_RXTX_1_N — USBC0_D2R_N<1>
USBC_ATC0_R2D_P<2>	P3	SFP_PHY_RXTX_3_P			CFP_PHY_RXTX_3_P — USBC0_D2R_P<2>
USBC_ATC0_R2D_N<2>	N3	SFP_PHY_RXTX_3_N			CFP_PHY_RXTX_3_N — USBC0_D2R_N<2>
USBC_ATC0_AUX_C_P	L4	SFP_LPDP_AUX_P			CFP_LPDP_AUX_P — USBC0_AUX_P
USBC_ATC0_AUX_C_N	M4	SFP_LPDP_AUX_N			CFP_LPDP_AUX_N — USBC0_AUX_N
CIO_ATC0_LSTX	G1	USB4_SFP_SB_RX			USB4_CFP_SB_RX — USBC0_CIO_LSRX
CIO_ATC0_LSRX	G2	USB4_SFP_SB_TX			USB4_CFP_SB_TX — USBC0_CIO_LSTX
					USB4_CFP_SB_TX_DIR — ATCRTMR0_LSTX_DIR
ATCRTMR0_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P			CFP_PHY_RCAL_P — ATCRTMR0_CFP_RCAL_POS
ATCRTMR0_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N			CFP_PHY_RCAL_N — ATCRTMR0_CFP_RCAL_NEG
GND	M1	CHIP_ID_0	GPIO	PERIPHERAL	QSPI_CS* — SPI_ATCRTMR0_CS_L
GND	N1	CHIP_ID_1			QSPI_SCLK — SPI_ATCRTMR0_CLK
ATCRTMR0_BOOT_CONFIG0	H2	BOOT_CONFIG0			QSPI_DQ0 — SPI_ATCRTMR0_DIO<0>
ATCRTMR0_BOOT_CONFIG1	J1	BOOT_CONFIG1			QSPI_DQ1 — SPI_ATCRTMR0_DIO<1>
ATCRTMR0_BOOT_CONFIG2	K1	BOOT_CONFIG2			QSPI_DQ2 — SPI_ATCRTMR0_DIO<2>
ATCRTMR0_FORCE_DFU	C1	FORCE_DFU			QSPI_DQ3 — SPI_ATCRTMR0_DIO<3>
NC_ATCRTMR0_GPIO0	K2	GPIO0			I2C0_SCL — I2C_ATCRTMR_SCL
NC_ATCRTMR0_GPIO1 (NO_TEST=1)	L3	GPIO1			I2C0_SDA — I2C_ATCRTMR_SDA
NC_ATCRTMR0_GPIO2	K3	GPIO2			I2C1_SCL — I2C_UPC0_ATCRTMR0_SCL
TP_ATCRTMR0_GPIO3	L10	GPIO3			I2C1_SDA — I2C_UPC0_ATCRTMR0_SDA
					I2C1_INT — UPC0_ATCRTMR0_I2C_INT_L
ATCRTMR0_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET	TEST AND DEBUG	TESTMODE — ATCRTMR0_TESTMODE
	M2	CFSB			JTAG_SEL — ATCRTMR0_JTAG_SEL
ATCRTMR0_XTAL24M_IN	F11	XI0			JTAG_TCK — SWD_NUB_ATCRTMR01_SWCLK
ATCRTMR0_XTAL24M_OUT	E11	XO0			JTAG_TMS — SWD_NUB_ATCRTMR01_SWDIO
					JTAG_TDI — TP_ATCRTMR0_JTAG_TDI
					JTAG_TDO — ATCRTMR0_JTAG_TDO
					JTAG_TRST* — TP_ATCRTMR0_JTAG_TRESET
					ANALOGMUX_OUT — TP_ATCRTMR0_ANALOGMUX_OUT
					TST_CLKOUT — NC_ATCRTMR0_TST_CLKOUT
					TST_CLK_LVDS_0_P — NC_ATCRTMR0_CLK_LVDSP<0> (NO_TEST=1)
					TST_CLK_LVDS_0_N — NC_ATCRTMR0_CLK_LVDSN<0> (NO_TEST=1)
					TST_CLK_LVDS_1_P — NC_ATCRTMR0_CLK_LVDSP<1> (NO_TEST=1)
					TST_CLK_LVDS_1_N — NC_ATCRTMR0_CLK_LVDSN<1> (NO_TEST=1)

SPI_ATCRTMR0_DIO<0> — RF097 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_R_DIO<0>
SPI_ATCRTMR0_DIO<1> — RF098 33 1/20W 5% TK 0201 — SPI_ATCRTMR0_R_DIO<1>

PP1V2_ATCRTMR01_VDDIO
RF090 3.3K 5% 1/20W TK 0201
NOSTUFF RF091 3.3K 5% 1/20W TK 0201
NOSTUFF RF092 3.3K 5% 1/20W TK 0201
NOSTUFF RF093 3.3K 5% 1/20W TK 0201
CF090 1.0UF 20% 6.3V X5R 0201-1

OMIT_TABLE CRITICAL
VCC 338S00574
UF090 64MBIT-1.2V W25Q64NE XSON-1

SPI_ATCRTMR0_CLK	RF094 33 1/20W 5% TK 0201	SPI_ATCRTMR0_CLK_R — CLK
SPI_ATCRTMR0_CS_L		SPI_ATCRTMR0_CS_L — CS*
SPI_ATCRTMR0_DIO<2>	RF095 33 1/20W 5% TK 0201	SPI_ATCRTMR0_R_DIO<2> — WP*(IO2)
SPI_ATCRTMR0_DIO<3>	RF096 33 1/20W 5% TK 0201	SPI_ATCRTMR0_R_DIO<3> — HOLD*(IO3)

DI(IO0) — SPI_ATCRTMR0_R_DIO<0>
DO(IO1) — SPI_ATCRTMR0_R_DIO<1>
GND, EPAD
PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_ATCRTMR01_VDDIO
VCC CRITICAL
UF090 64MBIT-1.2V GD25UF64E WLCSP-COMBO
OMIT_TABLE 335S00638

SPI_ATCRTMR0_CLK_R	D2	SCLK	
SPI_ATCRTMR0_CS_L	B3	CS*	
SPI_ATCRTMR0_R_DIO<2>	D3	IO2	SO(IO1) — SPI_ATCRTMR0_R_DIO<0>
SPI_ATCRTMR0_R_DIO<3>	C2	IO3	SI(IO0) — SPI_ATCRTMR0_R_DIO<1>
			NC, NC, NC, NC
		VSS	

PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC0

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

Re-timer to connector connections are set

PP1V2_S2

RF162 1.5K 1% 1/20W TK 0201 — I2C_UPC1_ATCRTMR1_SCL
RF163 1.5K 1% 1/20W TK 0201 — I2C_UPC1_ATCRTMR1_SDA

RF143 47K 5% 1/20W TK 0201 — CIO_ATC1_LSTX
RF144 47K 5% 1/20W TK 0201 — CIO_ATC1_LSRX

ATCRTMR1_CFP_RCAL_NEG
CF111 10PF 5% 25V C0G 0201
RF111 200 1% 1/20W TK 0201-1 — ATCRTMR1_CFP_RCAL_POS

ATCRTMR1_SFP_RCAL_NEG
CF110 10PF 5% 25V C0G 0201
RF110 200 1% 1/20W TK 0201-1 — ATCRTMR1_SFP_RCAL_POS

USBC HIGH-SPEED AC COUPLING

IN	USBC_ATC1_R2D_C_P<1>	CF120 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_P<1>
IN	USBC_ATC1_R2D_C_N<1>	CF121 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_N<1>
IN	USBC_ATC1_R2D_C_P<2>	CF124 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_P<2>
IN	USBC_ATC1_R2D_C_N<2>	CF125 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_R2D_N<2>
BI	USBC_ATC1_D2R_P<1>	CF122 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_P<1>
BI	USBC_ATC1_D2R_N<1>	CF123 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_N<1>
BI	USBC_ATC1_D2R_P<2>	CF126 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_P<2>
BI	USBC_ATC1_D2R_N<2>	CF127 0.22UF 20% 6.3V X5R 0201	USBC_ATC1_D2R_C_N<2>

(GND_VOID=TRUE)

ATCRTMR1_XTAL24M_OUT
RF160 499 1% 1/20W TK 0201
197S0591 CRITICAL YF100 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC1_24M_O_R
CRITICAL CF160 15PF 5% 50V C0G 0201
ATCRTMR1_XTAL24M_IN
CRITICAL 131S0831 CF161 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR01_VDD_CIO
CF130 14UF 20% 4V X5R 0402-D2X-1
CF131 14UF 20% 4V X5R 0402-D2X-1
138S00149
CF132 0.1UF 10% 6.3V X6S 0201
CF133 0.1UF 10% 6.3V X6S 0201

UF100 TMNB25B1-K1S1 FCCSP 338S00888 SYM 2 OF 2

J4	VDD_CIO_0	OMIT_TABLE CRITICAL	
J6	VDD_CIO_0		
J8	VDD_CIO_0		
F4	VDD_CIO_1		
F6	VDD_CIO_1		
F8	VDD_CIO_1		
G4	VDD_FIXED		
G5	VDD_FIXED		
H5	VDD_FIXED		
H6	VDD_FIXED		
G7	VDD_FIXED_PLL		
G9	VDD_FIXED_XTAL		
K5	VDDIO12_CIO_0		
K7	VDDIO12_CIO_0		
L6	VDDIO12_CIO_0		
D6	VDDIO12_CIO_1		
E5	VDDIO12_CIO_1		
E7	VDDIO12_CIO_1		
K8	VDDIO12_PLL_SOC0		
H8	VDDIO12_PLL_SOC1		
H9	VDDIO12_XTAL		
E9	VDDIO12		
H3	VDDIO12		
K9	VDDIO12		
F3	VDDIO12_EFUSE1		
F7	VDDIO12_AMUX		
A1,A2,A4,A6,A8,A10,A11,B2,B4,B6,B8,B10,C3,C5,C6,C7,C9,D1,D5,D7,D11,E3,E4,E6,E8,F2,F5,F10,G3,G6,G8	VSS		
H4,H7,J2,J3,J5,J7,J10,K4,K6,L1,L5,L7,L11,M3,M5,M6,M7,M9,N2,N4,N6,N8,N10,P1,P2,P4,P6,P8,P10,P11	VSS		

PP1V2_ATCRTMR01_VDDIO
132S0395 CF134 0.1UF 10% 6.3V X6S 0201
138S00039 CF135 2.2UF 20% 4V X6S-CERM 0201
CF136 14UF 20% 4V X5R 0402-D2X-1
CF137 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR01_VDD_FIXED
CF140 0.1UF 10% 6.3V X6S 0201
CF141 0.1UF 10% 6.3V X6S 0201
CF142 2.2UF 20% 4V X6S-CERM 0201
CF143 2.2UF 20% 4V X6S-CERM 0201
CF144 2.2UF 20% 4V X6S-CERM 0201
CF145 14UF 20% 4V X5R 0402-D2X-1
CF146 14UF 20% 4V X5R 0402-D2X-1

138S00039 CF152 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF100.K8:5MM
PP1V2_ATCRTMR01_VDDIO_XTAL_R (VOLTAGE=1.2V)
155S0644 FLF100 240-OHM-0.2A-0.9-OHM 0201
CF162 0.1UF 10% 6.3V X6S 0201 — 132S0395
CF163 2.2UF 20% 4V X6S-CERM 0201 — 138S00039

Connect to GND directly or via a resistor
GND

PP0V805_ATCRTMR01_VDD_FIXED
CF150 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF100.G7:5MM
PPVDD_FIXED_ATCRTMR1_XTAL_R
RF151 10 5% 1/20W TK 0201 — VOLTAGE=0.805V
117S00094
CF151 4UF 20% 2.5V X6S 0201 — 138S00329

132S0395 CF164 0.1UF 10% 6.3V X6S 0201

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF145 47K 5% 1/20W TK 0201 — ATCRTMR1_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RF147 47K 5% 1/20W TK 0201 — ATCRTMR1_JTAG_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF140 1UK 5% 1/20W TK 0201 — ATCRTMR1_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

UF100 TMNB25B1-K1S1 FCCSP 338S00888 SYM 1 OF 2 — OMIT_TABLE CRITICAL

SFP PHY

USBC_ATC1_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	CFP_PHY_RXTX_0_P — USBC1_R2D_CR_P<1> (MUX)
USBC_ATC1_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N	CFP_PHY_RXTX_0_N — USBC1_R2D_CR_N<1> (MUX)
USBC_ATC1_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P	CFP_PHY_RXTX_2_P — USBC1_R2D_CR_P<2> (MUX)
USBC_ATC1_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N	CFP_PHY_RXTX_2_N — USBC1_R2D_CR_N<2> (MUX)
USBC_ATC1_R2D_P<1>	P7	SFP_PHY_RXTX_1_P	CFP_PHY_RXTX_1_P — USBC1_D2R_P<1> (BI)
USBC_ATC1_R2D_N<1>	N7	SFP_PHY_RXTX_1_N	CFP_PHY_RXTX_1_N — USBC1_D2R_N<1> (BI)
USBC_ATC1_R2D_P<2>	P3	SFP_PHY_RXTX_3_P	CFP_PHY_RXTX_3_P — USBC1_D2R_P<2> (BI)
USBC_ATC1_R2D_N<2>	N3	SFP_PHY_RXTX_3_N	CFP_PHY_RXTX_3_N — USBC1_D2R_N<2> (BI)
USBC_ATC1_AUX_C_P (BI)	L4	SFP_LPDP_AUX_P	CFP_LPDP_AUX_P — USBC1_AUX_P (BI)
USBC_ATC1_AUX_C_N (BI)	M4	SFP_LPDP_AUX_N	CFP_LPDP_AUX_N — USBC1_AUX_N (BI)
CIO_ATC1_LSTX (IN)	G1	USB4_SFP_SB_RX	USB4_CFP_SB_RX — USBC1_CIO_LSRX (IN)
CIO_ATC1_LSRX (OUT)	G2	USB4_SFP_SB_TX	USB4_CFP_SB_TX — USBC1_CIO_LSTX (BI)
			USB4_CFP_SB_TX_DIR — ATCRTMR1_LSTX_DIR (MUX)
ATCRTMR1_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P	CFP_PHY_RCAL_P — ATCRTMR1_CFP_RCAL_POS
ATCRTMR1_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N	CFP_PHY_RCAL_N — ATCRTMR1_CFP_RCAL_NEG

GPIO PERIPHERAL

ATCRTMR1_CHIPID_0 (IN)	M1	CHIP_ID_0	QSPI_CS* — SPI_ATCRTMR1_CS_L
GND (IN)	N1	CHIP_ID_1	QSPI_SCLK — SPI_ATCRTMR1_CLK
ATCRTMR1_BOOT_CONFIG0 (IN)	H2	BOOT_CONFIG0	QSPI_DQ0 — SPI_ATCRTMR1_DIO<0>
ATCRTMR1_BOOT_CONFIG1 (IN)	J1	BOOT_CONFIG1	QSPI_DQ1 — SPI_ATCRTMR1_DIO<1>
ATCRTMR1_BOOT_CONFIG2 (IN)	K1	BOOT_CONFIG2	QSPI_DQ2 — SPI_ATCRTMR1_DIO<2>
			QSPI_DQ3 — SPI_ATCRTMR1_DIO<3>
ATCRTMR1_FORCE_DFU (IN)	C1	FORCE_DFU	I2C0_SCL — I2C_ATCRTMR_SCL (IN)
NC_ATCRTMR1_GPIO0	K2	GPIO0	I2C0_SDA — I2C_ATCRTMR_SDA (BI)
NC_ATCRTMR1_GPIO1 NO_TEST=1	L3	GPIO1	I2C1_SCL — I2C_UPC1_ATCRTMR1_SCL (IN)
NC_ATCRTMR1_GPIO2	K3	GPIO2	I2C1_SDA — I2C_UPC1_ATCRTMR1_SDA (BI)
NC_ATCRTMR1_GPIO3	L10	GPIO3	I2C1_INT — UPC1_ATCRTMR1_I2C_INT_L (MUX)

CLOCKS AND RESET / TEST AND DEBUG

ATCRTMR1_RESET_L (IN)	L2	COLD_RESET*	TESTMODE — ATCRTMR1_TESTMODE
	M2	CFSB	JTAG_SEL — ATCRTMR1_JTAG_SEL
ATCRTMR1_XTAL24M_IN	F11	XI0	JTAG_TCK — SWD_NUB_ATCRTMR01_SWCLK (BI)
ATCRTMR1_XTAL24M_OUT	E11	XO0	JTAG_TMS — SWD_NUB_ATCRTMR01_SWDIO (BI)
			JTAG_TDI — TP_ATCRTMR1_JTAG_TDI
			JTAG_TDO — ATCRTMR1_JTAG_TDO
			JTAG_TRST* — TP_ATCRTMR1_JTAG_TRESET
			ANALOGMUX_OUT — NC_ATCRTMR1_ANALOGMUX_OUT
			TST_CLKOUT — NC_ATCRTMR1_TST_CLKOUT
			TST_CLK_LVDS_0_P — NC_ATCRTMR1_CLK_LVDSP<0> NO_TEST=1
			TST_CLK_LVDS_0_N — NC_ATCRTMR1_CLK_LVDSN<0> NO_TEST=1
			TST_CLK_LVDS_1_P — NC_ATCRTMR1_CLK_LVDSP<1> NO_TEST=1
			TST_CLK_LVDS_1_N — NC_ATCRTMR1_CLK_LVDSN<1> NO_TEST=1

SPI_ATCRTMR1_DIO<0> — RF197 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<0>
SPI_ATCRTMR1_DIO<1> — RF198 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<1>

PP1V2_ATCRTMR01_VDDIO
RF190 3.3K 5% 1/20W TK 0201
NOSTUFF RF191 3.3K 5% 1/20W TK 0201
NOSTUFF RF192 3.3K 5% 1/20W TK 0201
NOSTUFF RF193 3.3K 5% 1/20W TK 0201
CF190 1.0UF 20% 6.3V X5R 0201-1

OMIT_TABLE CRITICAL 335S00574
UF190 64MBIT-1.2V W25Q64NE XSON-1

SPI_ATCRTMR1_CLK	RF194 33 1/20W 5% TK 0201	SPI_ATCRTMR1_CLK_R — CLK
SPI_ATCRTMR1_CS_L		SPI_ATCRTMR1_CS_L — CS*
SPI_ATCRTMR1_DIO<2>	RF195 33 1/20W 5% TK 0201	SPI_ATCRTMR1_R_DIO<2> — WP*(IO2)
SPI_ATCRTMR1_DIO<3>	RF196 33 1/20W 5% TK 0201	SPI_ATCRTMR1_R_DIO<3> — HOLD*(IO3)
		DI(IO0) — SPI_ATCRTMR1_R_DIO<0>
		DO(IO1) — SPI_ATCRTMR1_R_DIO<1>
		GND, EPAD

PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_ATCRTMR01_VDDIO

VCC CRITICAL
UF190 64MBIT-1.2V GD25UF64E WLCSP-COMBO
OMIT_TABLE 335S00638

SPI_ATCRTMR1_CLK_R	D2	SCLK	
SPI_ATCRTMR1_CS_L	B3	CS*	
SPI_ATCRTMR1_R_DIO<2>	D3	IO2	
SPI_ATCRTMR1_R_DIO<3>	C2	IO3	
	B2	VCC	
	E3	VSS	
SPI_ATCRTMR1_R_DIO<0>	E2	SI(IO0)	
SPI_ATCRTMR1_R_DIO<1>	C3	SO(IO1)	
	A2,A3,F2,F3	NC	

PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC1

Apple Inc.

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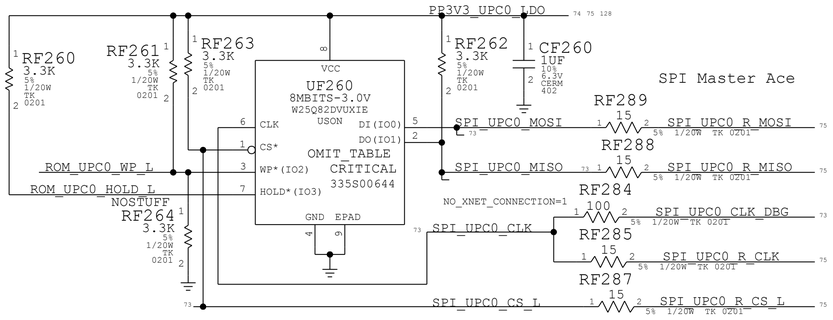
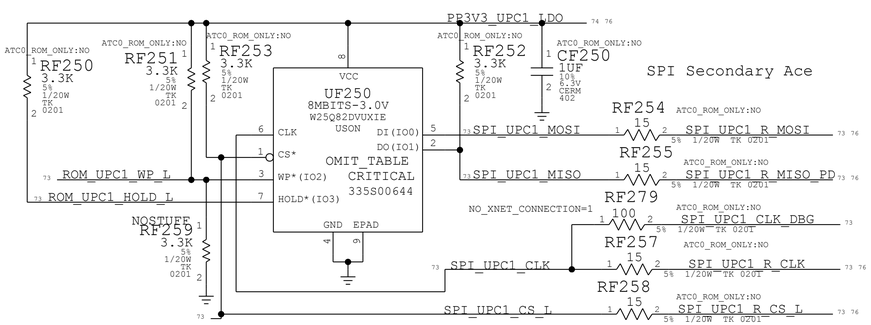


PACK_OPTION=UPC1_ROM:YES



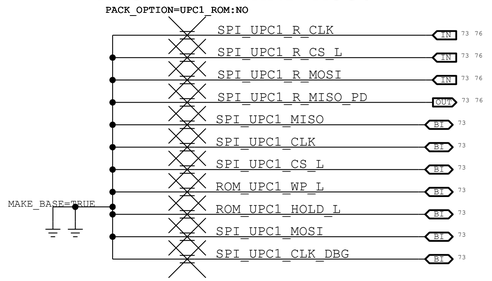
UPC1 Dedicated ROM and UART Debug chain possible pack_options:

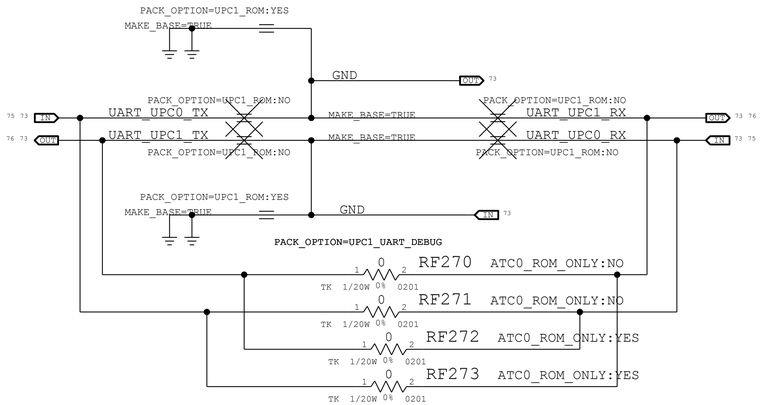
1. UPC1 may need its own ROM and need a fall-back method to no ROM for UPC1
 pick: "UPC1_ROM:YES" , "UPC1_UART_DEBUG" and "UPC1_UART_PD:NO"

2. UPC1 needs its own ROM and do not need a fall-back method to no ROM for UPC1
 pick: "UPC1_ROM:YES" and "UPC1_UART_PD:YES"

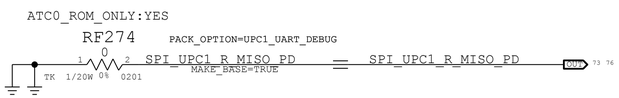
3. UPC1 does not need its own ROM
 pick: "UPC1_ROM:NO" and "UPC1_UART_PD:NO"

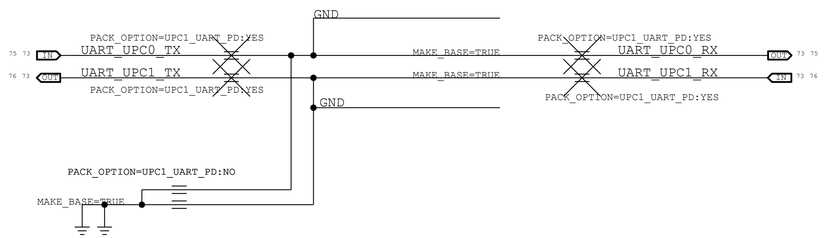
Ace 1 is UART Ace?



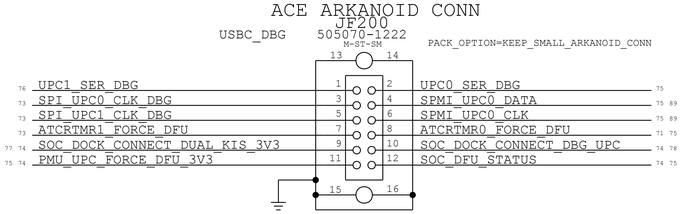


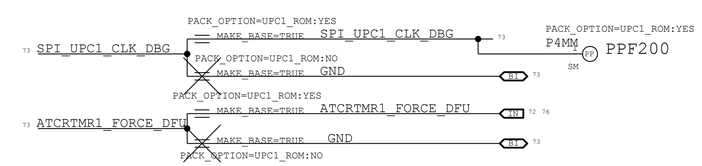
ATC0_ROM_ONLY:YES



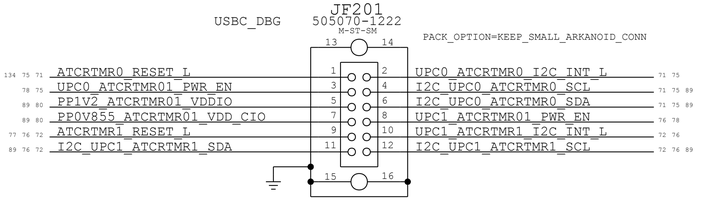


ACE ARKANOID CONN

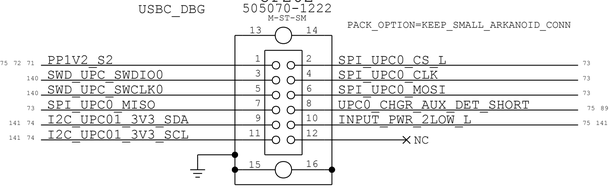


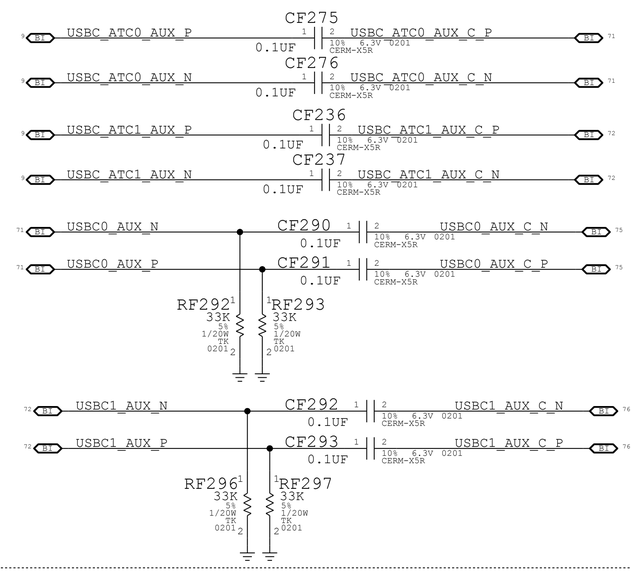


BRIDGE ARKANOID CONN



AARDVARKANOID CONN UPC0





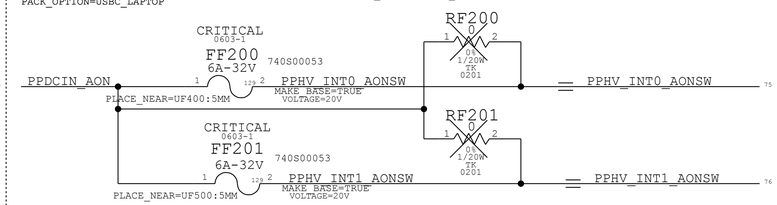
HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Support 1 ATC01

Apple Inc.

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UPC 0 is the Debug Port

ATC0 / UPC0 / RTMR0

SWD_SOC_SWCLK — MAKE_BASE=TRUE
SWD_SOC_SWDIO — MAKE_BASE=TRUE
UART_DEBUGPRT_R2D — MAKE_BASE=TRUE
UART_DEBUGPRT_D2R — MAKE_BASE=TRUE
PD_UPC0_DBG_R — MAKE_BASE=TRUE

RF321 100K 1/20W 5% 1 2 TK 0201 — PD_UPC0_DBG_R

PMU_ACTIVE_READY
SOC_DFU_STATUS — MAKE_BASE=TRUE
UPC0_SOC_FORCE_DFU — MAKE_BASE=TRUE — PACK_OPTION=SOC_FORCE_DFU:YES

SOC_DOCK_CONNECT_DBG_UPC — MAKE_BASE=TRUE
INT_I2C_EUSBLS0_L — MAKE_BASE=TRUE
UPC0_SOC_FORCE_DFU — MAKE_BASE=TRUE — PD_UPC0_GPIO11 — PACK_OPTION=SOC_FORCE_DFU:NO
I2C_UPC01_3V3_SCL — CKPLUS_WAIVE=I2C_PULLUP
I2C_UPC01_3V3_SDA — CKPLUS_WAIVE=I2C_PULLUP

RF311 100K 1/20W 5% 1 2 TK 0201 — PD_UPC0_GPIO5 — MAKE_BASE=TRUE
RF312 100K 1/20W 5% 1 2 TK 0201 — PD_UPC0_GPIO6 — MAKE_BASE=TRUE
RF313 100K 1/20W 5% 1 2 TK 0201 — PD_UPC0_GPIO11 — MAKE_BASE=TRUE
PACK_OPTION=SOC_FORCE_DFU:YES

UPC 1 GPIOs

ATC1 / UPC1 / RTMR1

RF300 100K 1/20W 5% 1 2 TK 0201 — PD_UPC1_DBG_R — MAKE_BASE=TRUE — CKPLUS_WAIVE=SINGLE_NODENET

PD_UPC1_DBG_R
PMU_ACTIVE_READY
SOC_DFU_STATUS — MAKE_BASE=TRUE
UPC1_SOC_FORCE_DFU — MAKE_BASE=TRUE — PACK_OPTION=SOC_FORCE_DFU:YES

SOC_DOCK_CONNECT_DUAL_KIS_3V3 — MAKE_BASE=TRUE
INT_I2C_EUSBLS1_L — MAKE_BASE=TRUE
I2C_UPC01_3V3_SCL
I2C_UPC01_3V3_SDA

RF301 100K 1/20W 5% 1 2 TK 0201 — PD_UPC1_GPIO5 — MAKE_BASE=TRUE
RF302 100K 1/20W 5% 1 2 TK 0201 — PD_UPC1_GPIO6 — MAKE_BASE=TRUE
RF304 100K 1/20W 5% 1 2 TK 0201 — PD_UPC1_GPIO11 — MAKE_BASE=TRUE
RF305 100K 1/20W 5% 1 2 TK 0201 — PD_UPC1_GPIO16 — MAKE_BASE=TRUE

ATCRTMR Boot Config

[2:0] = [011] 10K 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

RF380 10K 5% 1/20W TK 0201 — ATCRTMR0_BOOT_CONFIG2
RF381 10K 5% 1/20W TK 0201 — ATCRTMR0_BOOT_CONFIG1 — NOSTUFF
RF382 10K 5% 1/20W TK 0201 — ATCRTMR0_BOOT_CONFIG0 — LFKA_TEST_MODE:NO

RF383 10K 5% 1/20W TK 0201 — ATCRTMR1_BOOT_CONFIG2
RF384 10K 5% 1/20W TK 0201 — ATCRTMR1_BOOT_CONFIG1 — NOSTUFF
RF385 10K 5% 1/20W TK 0201 — ATCRTMR1_BOOT_CONFIG0 — LFKA_TEST_MODE:NO

LFKA_TEST_MODE:YES
RF386 10K 1/20W 2% TK 0201 — RF387 10K 1/20W 5% TK 0201 — RF388 10K NOSTUFF 5% 1/20W TK 0201 — PP1V2_ATCRTMR01_VDDIO
ATCRTMR0_BOOT_CONFIG2
ATCRTMR0_BOOT_CONFIG1
ATCRTMR0_BOOT_CONFIG0

LFKA_TEST_MODE:YES
RF389 10K 1/20W 2% TK 0201 — RF390 10K 1/20W 5% TK 0201 — RF391 10K NOSTUFF 5% 1/20W TK 0201 — PP1V2_ATCRTMR01_VDDIO
ATCRTMR1_BOOT_CONFIG2
ATCRTMR1_BOOT_CONFIG1
ATCRTMR1_BOOT_CONFIG0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00073	2	RES,TK,0 OHM, 1A MAX,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:DEFAULT_500mA
117S00073	2	RES,TK,0 OHM, 1A MAX,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:DISABLED
117S00131	2	RES,TK,51K OHM,5%,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:1000mA
117S00090	2	RES,TK,10K OHM,5%,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:1000mA
117S00098	2	RES,TK,20K OHM,5%,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	2	RES,TK,10K OHM,5%,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	2	RES,TK,10K OHM,5%,1/20W,0201	RF332,RF334	CRITICAL	SYS_BOOT_PWR:3000mA
117S00131	2	RES,TK,51K OHM,5%,1/20W,0201	RF333,RF335	CRITICAL	SYS_BOOT_PWR:3000mA

STRAP0/BUSPOWER

PP3V3_UPC0_LDO
PP3V3_UPC1_LDO

OMIT_TABLE RF332 10K 5% 1/20W TK 0201 1 2 — PACK_OPTION=USBC_LAPTOP
OMIT_TABLE RF334 10K 5% 1/20W TK 0201 1 2 — PACK_OPTION=USBC_LAPTOP
OMIT_TABLE RF333 20K 5% 1/20W TK 0201 1 2 — PACK_OPTION=USBC_LAPTOP
OMIT_TABLE RF335 20K 5% 1/20W TK 0201 1 2 — PACK_OPTION=USBC_LAPTOP

PACK_OPTION=USBC_DESKTOP — MAKE_BASE=TRUE
UPC0_STRAP0_BUSPOWER
UPC1_STRAP0_BUSPOWER
PACK_OPTION=USBC_DESKTOP

Unused ports

RF32A 100K 1/20W 5% 1 2 TK 0201 — PD_UPC1_USBP3_RP — MAKE_BASE=TRUE — PD_UPC1_USBP3_RP
RF31A 100K 1/20W 5% 1 2 TK 0201 — PD_UPC0_USBP3_RP — MAKE_BASE=TRUE — PD_UPC0_USBP3_RP

ATCRTMR0 CHIP 0X00

GND — MAKE_BASE=TRUE — GND

ATCRTMR1 CHIP 0X01

PP1V2_ATCRTMR01_VDDIO
XWF3000 SHORT-16L-0.1MM-SM 2 1
ATCRTMR1_CHIPID_0
GND — MAKE_BASE=TRUE

Connections for Laptops (USBC power in) — PACK_OPTION=USBC_LAPTOP

USBC0_CC1 — MAKE_BASE=TRUE — USBC0_CC1
USBC0_CC2 — MAKE_BASE=TRUE — USBC0_CC2
USBC1_CC1 — MAKE_BASE=TRUE — USBC1_CC1
USBC1_CC2 — MAKE_BASE=TRUE — USBC1_CC2

Connections for Desktops (No USBC power in) — PACK_OPTION=USBC_DESKTOP — MAKE_BASE=TRUE

LDCM

PACK_OPTION=LDCM:ENABLED — PACK_OPTION=LDCM:DISABLED

GND — USBC0_LDCM_CAC_RDC
GND — USBC0_LDCM_LB
GND — USBC1_LDCM_CAC_RDC
GND — USBC1_LDCM_LB

MAKE_BASE=TRUE

For production tie SPMI STRAP to GND directly
Enables SPMI Interface to SoC
SPMI: STRAP1=GND
I2C: STRAP1=LDO_3V3

STRAPS Configurations

PACK_OPTION=UPC_STRAP1_PD:NO — MAKE_BASE=TRUE

GND — GND — MAKE_BASE=TRUE
GND — GND — MAKE_BASE=TRUE

RF330 0 1/20W 0% TK 0201 1 2
RF331 0 1/20W 0% TK 0201 1 2
PACK_IGNORE=TRUE
PACK_OPTION=UPC_STRAP1_PD:YES

PACK_OPTION=UPC_STRAP1_PD:NO

Connect PMU FORCE_DFU output here

STRAP2
PMU_UPC_FORCE_DFU_3V3 — MAKE_BASE=TRUE — PMU_UPC_FORCE_DFU_3V3
UPC0_SOC_FORCE_DFU_3V3 — MAKE_BASE=TRUE — UPC0_SOC_FORCE_DFU_3V3

STRAP5
GND — MAKE_BASE=TRUE — GND

UPC0: STRAP3=GND STRAP4=GND
UPC1: STRAP3=NC STRAP4=GND
UPC2: STRAP3=GND STRAP4=NC
UPC5: STRAP3=NC STRAP4=140K

NC_UPC1_I2C_ADDR — MAKE_BASE=TRUE — NC_UPC1_I2C_ADDR — NO_TEST=1
GND — MAKE_BASE=TRUE — GND
GND — MAKE_BASE=TRUE — GND

Is UPCx_5V_EN being used?

UPC01_5V_EN — RF350 100K 5% 1/20W TK 0201 1 2
UPC01_5V_EN — RF351 100K 5% 1/20W TK 0201 1 2
PACK_IGNORE=TRUE
PACK_OPTION=USBC01_VR5V_LOCAL_NO

PP TO AVOID UPC01_REQUEST_DFU NOT CONNECTED WARNING

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 2 ATC01

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 153 OF 700
SHEET: 74 OF 156

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*** IN PROGRESS ***

73 PPHV_INT0_AONSW

MAX 100uF TOTAL ON RAIL

136 76 PP5V_S2SW_USBC01

136 76 PP5V_S2SW_USBC01

138S00123
CF406 10UF 20% 10V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

OMIT_TABLE

UF400
SN2012024
BGA

POWER

DIGITAL CORE I/O & CONTROL

TYPE-C

PORT MUX

		M22	HRESET		
75	PD_UPC0_MRESET	H18	GPIO14_MRESET		
134 73 71	OUT ATCRTMR0_RESET_L	B4	GPIO15_RESETZ		
73	OUT UPC0_SER_DBG	F26	GPIO0		
74	IN PMU_ACTIVE_READY	D18	GPIO1		
74 73	IN SOC_DFU_STATUS	K24	GPIO2		
74	OUT UPC0_SOC_FORCE_DFU	L21	GPIO3	PU	
74	OUT SOC_DOCK_CONNECT_DBG_UPC	J25	GPIO4		
74	OUT PD_UPC0_GPIO5	J9	GPIO5		
74	IN PD_UPC0_GPIO6	C1	GPIO6		
89 74	OUT UPC01_5V_EN	C5	GPIO7		
73 71	OUT ATCRTMR0_FORCE_DFU	F10	GPIO8		
73 71	IN UPC0_ATCRTMR0_I2C_INT_L	H10	GPIO9	PU	
74	IN INT_I2C_EUSBLS0_L	A3	GPIO10	PU	
74	BI PD_UPC0_GPIO11	L25	GPIO11		
141 73	OUT INPUT_PWR_2LOW_L	E11	GPIO12	PU	
89	OUT UPC_DFU_BOOTED_L	M26	GPIO16_DFU_BOOTED_L		
141	OUT UPC_PMU_RESET_1V2	G19	GPIO17_FORCE_RST_REQ		
71	BI USBC0_CIO_LSTX	L13	GPIO18_LSTXRX		
71	OUT USBC0_CIO_LSRX	C3	GPIO19_LSRX		
89 73	OUT UPC0_CHGR_AUX_DET_SHORT	N23	GPIO20_SS_HOLD		
71	IN ATCRTMR0_LSTX_DIR	G25	GPIO21_LSX_DIR		
74	IN UPC0_STRAP0_BUSPOWER	J17	STRAP0_BUSPOWER		
74	IN GND	L27	STRAP1_I2C_SPMI_SEL		
74 73	IN PMU_UPC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN		
74	IN GND	M20	STRAP3_I2C_ADDR0		
74	IN GND	N21	STRAP4_I2C_ADDR1		
74	IN GND	J21	STRAP5_VDDIO_CFG		
	UPC0_R_OSC	B10	R_OSC		
141 78	NC_UPC0_AID0	F14	AID0		
	NC_UPC0_AID1 NO_TEST=1	G15	AID1		
	NC_UPC0_AID2 NO_TEST=1	H14	AID2		
	NC_UPC0_AID3 NO_TEST=1	E15	AID3		
89 73 71	BI I2C_UPC0_ATCRTMR0_SDA	A25	I2CC_SDA		
89 73 71	BI I2C_UPC0_ATCRTMR0_SCL	B26	I2CC_SCL		
74	BI I2C_UPC01_3V3_SDA	K28	I2C1_SDA_GPIO23		
74	IN I2C_UPC01_3V3_SCL	J27	I2C1_SCL_GPIO22		
	NC_INT_I2C_UPC0_L NO_TEST=1	H26	I2C_IRQ1Z		
89 73	BI SPMI_UPC0_DATA	N25	SPMI_I2C2_DATA	1V25	
89 73	IN SPMI_UPC0_CLK	M24	SPMI_I2C2_CLK	1V25	
	NC_INT_I2C_SMC_UPC0_L NO_TEST=1	K26	I2C_IRQ2Z		
73	OUT SPI_UPC0_R_CLK	G27	SPI_CLK		
73	OUT SPI_UPC0_R_MOSI	H28	SPI_COPI		
73	IN SPI_UPC0_R_MISO	F28	SPI_CIPO		
73	OUT SPI_UPC0_R_CS_L	E27	SPI_CSZ		
140 12	BI SWD_UPC_SWDIO0	E25	SWD_DATA	IPU	
140 12	BI SWD_UPC_SWCLK0	E23	SWD_CLK	IPU	
75 73	IN UART_UPC0_RX	D28	UART_RX		
73	OUT UART_UPC0_TX	C27	UART_TX		
89	BI USB2_UPC0_P1_P	A15	USB_RP1_P		
89	BI USB2_UPC0_P1_N	B16	USB_RP1_N		
143	BI USB_DBG_LS_P	A17	USB_RP2_P		
143	BI USB_DBG_LS_N	B18	USB_RP2_N		
74	BI PD_UPC0_USBP3_RP	A19	USB_RP3_P		
74	BI PD_UPC0_USBP3_RP	B20	USB_RP3_N		
73	BI USBC0_AUX_C_P	D14	AUX_P		
73	BI USBC0_AUX_C_N	C15	AUX_N		
75	PD_UPC0_HPD	G11	GPIO13_HPDTXRX		
134 74	IN SWD_SOC_SWCLK	E19	DEBUG0_GPIO24		
134 74	OUT SWD_SOC_SWDIO	F18	DEBUG1_GPIO25		
134 74	OUT UART_DEBUGPRT_R2D	H22	DEBUG2_GPIO26		
134 74	BI UART_DEBUGPRT_D2R	D22	DEBUG3_GPIO27		
74	BI PD_UPC0_DBG_R	G23	DEBUG4_GPIO28		
74	BI PD_UPC0_DBG_R	F22	DEBUG5_GPIO29		
74	BI PD_UPC0_DBG_R	C23	DEBUG6_GPIO30		
74	BI PD_UPC0_DBG_R	D26	DEBUG7_GPIO31		

1M 5% 1/20W TK 0201 RF405 UART_UPC0_RX 73 75

100K 5% 1/20W TK 0201 RF406 PD_UPC0_MRESET 75

100K 5% 1/20W TK 0201 RF407 PD_UPC0_HPD 75

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL RF403 15K 0.1% 1/20W TK 0201 103S00582

Configurable as SPMI or I2C Port 2
SMC SPMI: 0XD
AP SPMI: 0XC
I2C: 0X38

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

GROUND

GND A1 B2 K16 K20 M28 N19 N27

PPVBUS_USBC0 69 128

CF401 1UF 10% 35V X5R 0402

DF400 DSN2 NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2 76 78 79 135

CF400 10UF 20% 6.3V CERM 0402

PP1V2_S2 71 72 73 76 78 79 135

CF402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750 VOLTAGE=3.3V

PP3V3_UPC0_LDO 73 74 128

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.0750 VOLTAGE=1.8V

CF408 10UF 20% 6.3V CERM 0402

PP1V8_UPC0_LDO

CF417 10UF 20% 6.3V CERM 0402

PP1V8_S2 76 79 135

CF403 0.1UF 10% 6.3V CERM-X5R 0201

VIN_3V3	C19		
VDDIO	C25		
LDO_3V3	B22		
LDO_1V8	A23		
VIN_LV	A27 / B28		
VOUT_LV	B24		UPC0_ATCRTMR01_PWR_EN 73 78 (cap needed when used as power source)
SS	A5	UPC0_SS	
LDO_CORE	A21	PP1V5_UPC0_LDO_CORE	VOLTAGE=1.5V MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750
C_CC1	M16 / N15	USBC0_CC1	
C_CC2	M18 / N17	USBC0_CC2	
RPD_G1	L17	USBC0_CC1	BI 74
RPD_G2	L19	USBC0_CC2	BI 74
C_USB_TP	A11	USBC0_USB_TOP_P	BI 69 128
C_USB_TN	A13	USBC0_USB_TOP_N	BI 69 128
C_USB_BP	B12	USBC0_USB_BOT_P	BI 69
C_USB_BN	B14	USBC0_USB_BOT_N	BI 69
C_SBU1	C11	USBC0_SBU1	BI 69 128
C_SBU2	D10	USBC0_SBU2	BI 69 128
LDCM	B8	USBC0_LDCM_CAC_RDC	74
LDCM_LB	C7	USBC0_LDCM_LB	IN 69 74 128
LDCM_SENSE	A7	USBC0_LDCM_SW	
LDCM_COMP	B6	USBC0_LDCM_COMP	
LDCM_SW	A9	USBC0_LDCM_SW	MAKE_BASE=TRUE

CF405 10UF 20% 6.3V CERM 0402

CF409 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_CAP

PACK_OPTION=ACE2_SS_GND GND MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 BI 69 74 128

MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 BI 69 74 128

CF414 220PF 5% 50V C0G 0201-1

CF413 220PF 5% 50V C0G 0201-1

LDCM circuit subject to change

PACK_OPTION=LDCM:ENABLED CRITICAL CF420 2.2UF 10% 35V X5R 0402 138S00488

CAC

RDC

PACK_OPTION=LDCM:ENABLED CRITICAL RF411 402K 1% 1/20W TK 0201 118S00666

PACK_IGNORE=TRUE PACK_OPTION=LDCM:DISABLED RF414 100K 5% 1/20W TK 0201

PACK_IGNORE=TRUE PACK_OPTION=LDCM:DISABLED 10K RF415 1/20W 5% 0201 TK

PACK_OPTION=LDCM:ENABLED R2 CRITICAL RF410 4.99K 1/20W 0.1% 0201 TK 103S00656

PACK_OPTION=LDCM:ENABLED

PACK_OPTION=LDCM:ENABLED CRITICAL RF413 R1 10K 1/20W 0.1% 0201 TK 103S00593

128 69 IN USBC0_LDCM USBC0_LDCM_R

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Port Controller ATC0

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

PAGE: 154 OF 700

SHEET: 75 OF 156

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73 PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

136 75 PP5V_S2SW_USBC01

136 75 PP5V_S2SW_USBC01

CF506 138S00123 1 2 10UF 20% 10V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

OMIT_TABLE

UF500 SN2012024 BGA

	M22	HRESET	
76 PD_UPC1_MRESET	H18	GPIO14_MRESET	
77 73 72 OUT ATCRTMR1_RESET_L	B4	GPIO15_RESETZ	
73 OUT UPC1_SER_DBG	F26	GPIO0	
74 IN PMU_ACTIVE_READY	D18	GPIO1	
74 IN SOC_DFU_STATUS	K24	GPIO2	
74 OUT UPC1_SOC_FORCE_DFU	L21	GPIO3	PU
74 OUT SOC_DOCK_CONNECT_DUAL_KIS_3V3	J25	GPIO4	
74 OUT PD_UPC1_GPIO5	J9	GPIO5	
74 IN PD_UPC1_GPIO6	C1	GPIO6	
89 74 OUT UPC01_5V_EN	C5	GPIO7	
73 72 OUT ATCRTMR1_FORCE_DFU	F10	GPIO8	
73 72 IN UPC1_ATCRTMR1_I2C_INT_L	H10	GPIO9	PU
74 IN INT_I2C_EUSBLS1_L	A3	GPIO10	PU
74 B1 PD_UPC1_GPIO11	L25	GPIO11	
141 OUT INPUT_PWR_2LOW_L	E11	GPIO12	PU
74 OUT PD_UPC1_GPIO16	M26	GPIO16_DFU_BOOTED_L	
141 OUT UPC_PMU_RESET_1V2	G19	GPIO17_FORCE_RST_REQ	
73 B1 USBC1_CIO_LSTX	L13	GPIO18_LSTXRX	
73 OUT USBC1_CIO_LSRX	C3	GPIO19_LSRX	
89 OUT UPC1_CHGR_AUX_DET_SHORT	N23	GPIO20_SS_HOLD	
73 IN ATCRTMR1_LSTX_DIR	G25	GPIO21_LSX_DIR	
74 IN UPC1_STRAP0_BUSPOWER	J17	STRAP0_BUSPOWER	
74 IN GND	L27	STRAP1_I2C_SPMI_SEL	
74 IN UPC0_SOC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN	
74 IN NC_UPC1_I2C_ADDR	M20	STRAP3_I2C_ADDR0	
74 IN GND	N21	STRAP4_I2C_ADDR1	
74 IN GND	J21	STRAP5_VDDIO_CFG	
UPC1_R_OSC	B10	R_OSC	
NC_UPC1_AID0 NO_TEST=1	F14	AID0	
NC_UPC1_AID1 NO_TEST=1	G15	AID1	
NC_UPC1_AID2 NO_TEST=1	H14	AID2	
NC_UPC1_AID3 NO_TEST=1	E15	AID3	
89 73 72 B1 I2C_UPC1_ATCRTMR1_SDA	A25	I2CC_SDA	
89 73 72 B1 I2C_UPC1_ATCRTMR1_SCL	B26	I2CC_SCL	
74 B1 I2C_UPC01_3V3_SDA	K28	I2C1_SDA_GPIO23	
74 IN I2C_UPC01_3V3_SCL	J27	I2C1_SCL_GPIO22	
NC_INT_I2C_UPC1_L NO_TEST=1	H26	I2C_IRQ1Z	
89 B1 SPMI_UPC1_DATA	N25	SPMI_I2C2_DATA	
89 IN SPMI_UPC1_CLK	M24	SPMI_I2C2_CLK	
NC_INT_I2C_SMC_UPC1_L NO_TEST=1	K26	I2C_IRQ2Z	
73 OUT SPI_UPC1_R_CLK	G27	SPI_CLK	
73 OUT SPI_UPC1_R_MOSI	H28	SPI_COPI	
73 IN SPI_UPC1_R_MISO_PD	F28	SPI_CIPO	
73 OUT SPI_UPC1_R_CS_L	E27	SPI_CSZ	
72 B1 SWD_UPC_SWDIO1	E25	SWD_DATA	IPU
72 B1 SWD_UPC_SWCLK1	E23	SWD_CLK	IPU
76 73 IN UART_UPC1_RX	D28	UART_RX	
73 OUT UART_UPC1_TX	C27	UART_TX	
89 B1 USB2_UPC1_P1_P	A15	USB_RP1_P	
89 B1 USB2_UPC1_P1_N	B16	USB_RP1_N	
143 73 B1 USB2_ATC1_DBG_LS_P	A17	USB_RP2_P	
143 73 B1 USB2_ATC1_DBG_LS_N	B18	USB_RP2_N	
74 B1 PD_UPC1_USBP3_RP	A19	USB_RP3_P	
74 B1 PD_UPC1_USBP3_RP	B20	USB_RP3_N	
73 B1 USBC1_AUX_C_P	D14	AUX_P	
73 B1 USBC1_AUX_C_N	C15	AUX_N	
76 PD_UPC1_HPD	G11	GPIO13_HPDTXRX	
74 B1 PD_UPC1_DBG_R	E19	DEBUG0_GPIO24	
74 B1 PD_UPC1_DBG_R	F18	DEBUG1_GPIO25	
74 B1 PD_UPC1_DBG_R	H22	DEBUG2_GPIO26	
74 B1 PD_UPC1_DBG_R	D22	DEBUG3_GPIO27	
74 B1 PD_UPC1_DBG_R	G23	DEBUG4_GPIO28	
74 B1 PD_UPC1_DBG_R	F22	DEBUG5_GPIO29	
74 B1 PD_UPC1_DBG_R	C23	DEBUG6_GPIO30	
74 B1 PD_UPC1_DBG_R	D26	DEBUG7_GPIO31	

DIGITAL CORE I/O & CONTROL

POWER

TYPE-C

PORT MUX

1M 5% 1/20W TK 0201 RF505 UART_UPC1_RX 73 76

100K 5% 1/20W TK 0201 RF506 PD_UPC1_MRESET 76

100K 5% 1/20W TK 0201 RF507 PD_UPC1_HPD 76

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL RF503 15K 0.1% 1/20W TK 0201 103S00582

Configurable as SPMI or I2C Port 2
SMC SPMI: 0XB
AP SPMI: 0XA
I2C: 0X3F

PPVBUS_USBC1 69 128

CF501 1UF 10% 35V X5R 0402

DF500 DSN2 NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2 75 78 79 135

CF500 10UF 20% 6.3V CERM 0402

PP1V2_S2 71 72 73 75 78 79 135

CF502 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC1_LDO 73 74

CF508 10UF 20% 6.3V CERM 0402

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V

PP1V8_UPC1_LDO

CF517 10UF 20% 6.3V CERM 0402

PP1V8_S2 75 79 135

CF503 0.1UF 10% 6.3V CERM-X5R 0201

VIN_3V3	C19		
VDDIO	C25		
LDO_3V3	B22		
LDO_1V8	A23		
VIN_LV	A27, B28		
VOUT_LV	B24	UPC1_ATCRTMR01_PWR_EN 73 78 (cap needed when used as power source)	
SS	A5	UPC1_SS	
LDO_CORE	A21	PP1V5_UPC1_LDO_CORE	VOLTAGE=1.5V MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750
C_CC1	M16, N15	USBC1_CC1	
C_CC2	M18, N17	USBC1_CC2	
RPD_G1	L17	USBC1_CC1	
RPD_G2	L19	USBC1_CC2	
C_USB_TP	A11	USBC1_USB_TOP_P	
C_USB_TN	A13	USBC1_USB_TOP_N	
C_USB_BP	B12	USBC1_USB_BOT_P	
C_USB_BN	B14	USBC1_USB_BOT_N	
C_SBU1	C11	USBC1_SBU1	
C_SBU2	D10	USBC1_SBU2	
LDCM	B8	USBC1_LDCM_CAC_RDC	
LDCM_LB	C7	USBC1_LDCM_LB	
LDCM_SENSE	A7	USBC1_LDCM_SW	
LDCM_COMP	B6	USBC1_LDCM_COMP	
LDCM_SW	A9	USBC1_LDCM_SW	

CF505 10UF 20% 6.3V CERM 0402

CF509 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_CAP

PACK_OPTION=ACE2_SS_GND GND MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500

MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500

CF514 220PF 5% 50V COG 0201-1

CF513 220PF 5% 50V COG 0201-1

LDCM circuit subject to change

PACK_OPTION=LDCM:ENABLED
CRITICAL
CF520 2.2UF 10% 35V X5R 0402 138S00488

CAC

RDC

PACK_OPTION=LDCM:ENABLED
CRITICAL
RF511 402K 1% 1/20W TK 0201 118S00666

PACK_IGNORE=TRUE
PACK_OPTION=LDCM:DISABLED
RF515 10K 5% 1/20W 0201 TK

PACK_OPTION=LDCM:DISABLED
RF514 100K 5% 1/20W TK 0201

PACK_IGNORE=TRUE
PACK_OPTION=LDCM:ENABLED
R2 CRITICAL RF510 4.99K 1% 1/20W 0.1% 0201 TK 103S00656

PACK_OPTION=LDCM:ENABLED

PACK_OPTION=LDCM:ENABLED
CRITICAL
RF513 10K 1% 1/20W 0.1% 0201 TK 103S00593
R1

128 69 IN USBC1_LDCM — USBC1_LDCM_R

GROUND

GND

A1 B2 K16 K20 M28 N19 N27

BOM COST GROUP=USB-C

PAGE TITLE: USB-C: Port Controller ATC1

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

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*** OK2INTEGRATE ***

MACAW 0

PP1V2_S2
CF612 1.0UF 20% 6.3V X5R 0201-1
CF613 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.A4:5MM
PLACE_NEAR=UF600.A4:5MM

PP1V8_S2
CF604 0.1UF 10% 10V X5R-CERM 0201
CF602 0.1UF 10% 10V X5R-CERM 0201
CF603 4.7UF 20% 4V CER-X5R 0201
CF600 1.0UF 20% 6.3V X5R 0201-1
CF615 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.B2:5MM
PLACE_NEAR=UF600.B2:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM

PP1V1_MACAW0_VCCD
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
CF606 4.7UF 20% 6.3V X6S 0402

PP3V3_S2
CF607 0.1UF 10% 10V X5R-CERM 0201
CF608 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.C6:5MM
PLACE_NEAR=UF600.C6:5MM

UF600
CYUSB2405A2
CSP
338S00851

VCCD D4
VDDD B5
VDDIO A4
VDD3V3 C6
VSS C5
VSSQ C2

BOMOPTION=USBC_DUAL_KIS:NO
PLACE_NEAR=UF690.1:2MM
EUSB_DBG_P — RF690 0 1/20W 0% TK 0201 — EUSB_ATC0_DBG_P
NO_XNET_CONNECTION=1
EUSB_DBG_N — RF691 0 1/20W 0% TK 0201 — EUSB_ATC0_DBG_N
NO_XNET_CONNECTION=1
PLACE_NEAR=UF690.2:2MM
BOMOPTION=USBC_DUAL_KIS:NO

ATCRTMR0_RESET_1V2_1V8_MCW_L — RF603 4.7K 5% 1/20W TK 0201 — RESET*
TPF600 A TP-P50 ATCRTMR0_RESET_L_R

OMIT_TABLE
CRITICAL

INT_I2C_EUSBLS0_L — INT
I2C_UPC0_ATCRTMR0_SDA — SDA
I2C_UPC0_ATCRTMR0_SCL — SCL
EUSB_ATC0_P — EDP0
EUSB_ATC0_N — EDN0
EUSB_ATC0_DBG_P — EDP1
EUSB_ATC0_DBG_N — EDN1
CROSS
TPT_MACAW0_DEBUG_SWDCLK — GPIO_0/SWDCLK
TPT_MACAW0_DEBUG_SWDDAT — GPIO_1/SWDDAT

DP0 D6 USB2_ATC0_LS_MUX_P
DN0 D5 USB2_ATC0_LS_MUX_N
DP1 D2 USB_DBG_LS_MUX_P
DN1 D3 USB_DBG_LS_MUX_N

BOMOPTION=USBC_DUAL_KIS:YES
PP3V3_S2
CF690 1.0UF 20% 6.3V X5R 0201-1
BOMOPTION=USBC_DUAL_KIS:YES
NO_XNET_CONNECTION=1
EUSB_DBG_P — 1 Y+ 353S4037 M+ 5 — EUSB_ATC0_DBG_P
EUSB_DBG_N — 2 Y- UF690 M- 4 — EUSB_ATC0_DBG_N
PI3USB102EZLE TQFN CRITICAL
D+ 7 — EUSB_ATC1_DBG_P
D- 6 — EUSB_ATC1_DBG_N
SOC_DOCK_CONNECT_DUAL_KIS_3V3 — SEL 10 OE* 8
GND 9
RF692 47K 5% 1/20W TK 0201
LOW --> UPC0 Default KIS
HIGH --> UPC1 KIS
BOMOPTION=USBC_DUAL_KIS:YES

XIP C1 MACAW0_CLK24M_IN
XOP D1 MACAW0_CLK24M_OUT_R
RF600 0 1/20W 0% TK 0201
YF600 1.60X1.20MM 197S0591
CRITICAL CF611 9.5PF +/-0.1PF 50V C0G 0201 CER-C0G 131S00077
CRITICAL 131S00077 CF610 9.5PF +/-0.1PF 50V CER-C0G 0201
RESREF B6 MACAW0_RESREF
RF601 6.04K 1% 1/20W TK 0201

MACAW 1

PP1V2_S2
CF662 1.0UF 20% 6.3V X5R 0201-1
CF663 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.A4:5MM
PLACE_NEAR=UF650.A4:5MM

PP1V8_S2
CF654 0.1UF 10% 10V X5R-CERM 0201
CF651 0.1UF 10% 10V X5R-CERM 0201
CF652 4.7UF 20% 4V CER-X5R 0201
CF653 1.0UF 20% 6.3V X5R 0201-1
CF665 1.0UF 20% 6.3V X5R 0201-1
138S00138
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM

PP1V1_MACAW1_VCCD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.1V
CF656 4.7UF 20% 6.3V X6S 0402

PP3V3_S2
CF657 0.1UF 10% 10V X5R-CERM 0201
CF658 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.C6:5MM
PLACE_NEAR=UF650.C6:5MM

UF650
CYUSB2405A2
CSP
338S00851

VCCD D4
VDDD B5
VDDIO A4
VDD3V3 C6
VSS C5
VSSQ C2

ATCRTMR1_RESET_L — RESET*

OMIT_TABLE
CRITICAL

INT_I2C_EUSBLS1_L — INT
I2C_UPC1_ATCRTMR1_SDA — SDA
I2C_UPC1_ATCRTMR1_SCL — SCL
EUSB_ATC1_P — EDP0
EUSB_ATC1_N — EDN0
EUSB_ATC1_DBG_P — EDP1
EUSB_ATC1_DBG_N — EDN1
CROSS
TPT_MACAW1_DEBUG_SWDCLK — GPIO_0/SWDCLK
TPT_MACAW1_DEBUG_SWDDAT — GPIO_1/SWDDAT

DP0 D6 USB2_ATC1_LS_P
DN0 D5 USB2_ATC1_LS_N
DP1 D2 USB2_ATC1_DBG_LS_P
DN1 D3 USB2_ATC1_DBG_LS_N

XIP C1 MACAW1_CLK24M_IN
XOP D1 MACAW1_CLK24M_OUT_R
RF650 0 1/20W 0% TK 0201
YF660 1.60X1.20MM 197S0591
CRITICAL CF661 9.5PF +/-0.1PF 50V C0G 0201 CER-C0G 131S00077
CRITICAL 131S00077 CF660 9.5PF +/-0.1PF 50V CER-C0G 0201
RESREF B6 MACAW1_RESREF
RF651 6.04K 1% 1/20W TK 0201

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: USB2 RPT

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
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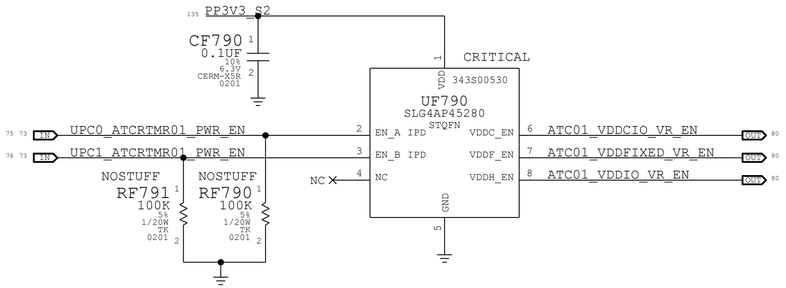
*** REFERENCE ONLY ***

Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF400 VDDIO) same time or before System 1.8V (UF400 VIN_LV pin)

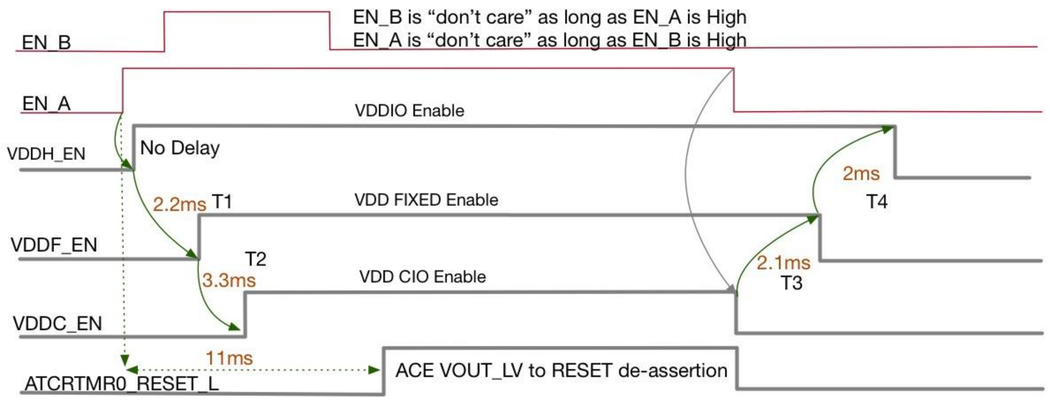
Power-up Sequence Requirements: 3.3_S2 to UF790 --> system 1.2V (UF400 VDDIO) same time or before system 1.8V (UF400) VIN_LV pin)

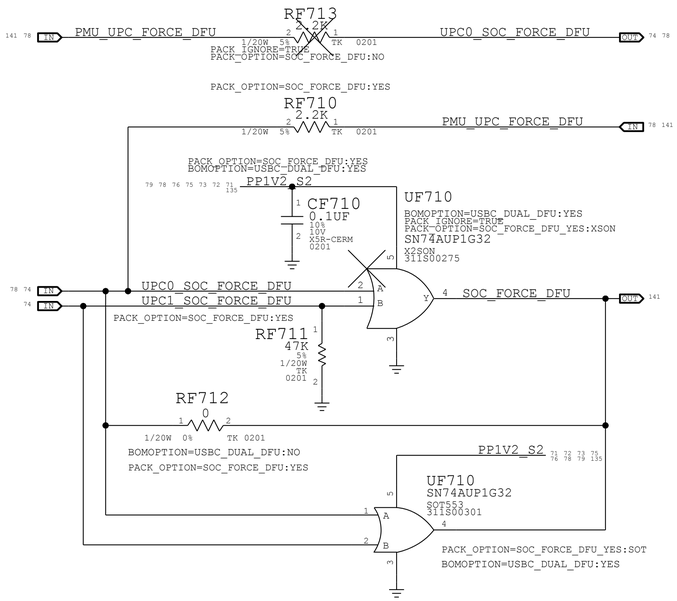
Power-down Sequence Requirements: The 1.8V first or at the same time as 1V2 --> 3V3_S2 needs to get disabled at minimum of 6ms from when 1V8 is discharged to below 300mV

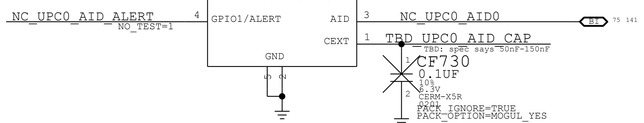
The 3.3V needs to be HIGH before VIN_LV of Aces



Note1: As long as EN_A or EN_B are High, the outputs stay High
Note2: Outputs are an ORed and delayed version of EN_A or EN_B

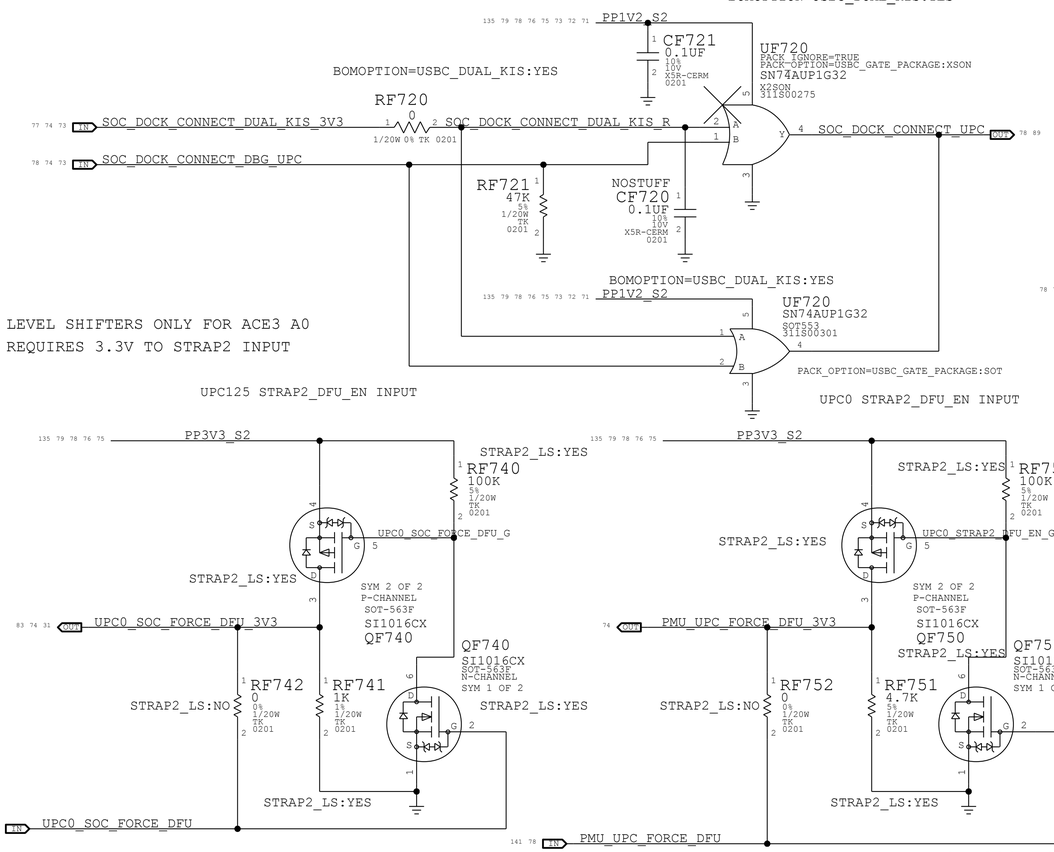






DUAL KIS Connection

BOMOPTION=USBC_DUAL_KIS:YES



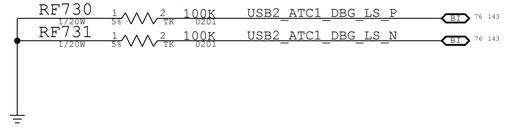
LEVEL SHIFTERS ONLY FOR ACE3 A0
REQUIRES 3.3V TO STRAP2 INPUT

UPC125 STRAP2_DFU_EN INPUT

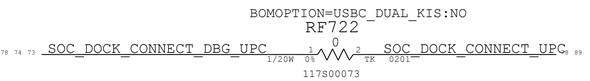
UPC0 STRAP2_DFU_EN INPUT

BOM_COST_GROUP=USB-C

BOMOPTION=USBC_DUAL_KIS:NO



BOMOPTION=USBC_DUAL_KIS:NO



PAGE TITLE

USB-C: Support 3 ATC01

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D

REVISION 4.0.0

BRANCH dvt-2

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*** OK2INTEGRATE ***

SET ONE OPTION FOR THE PBUS CAPS

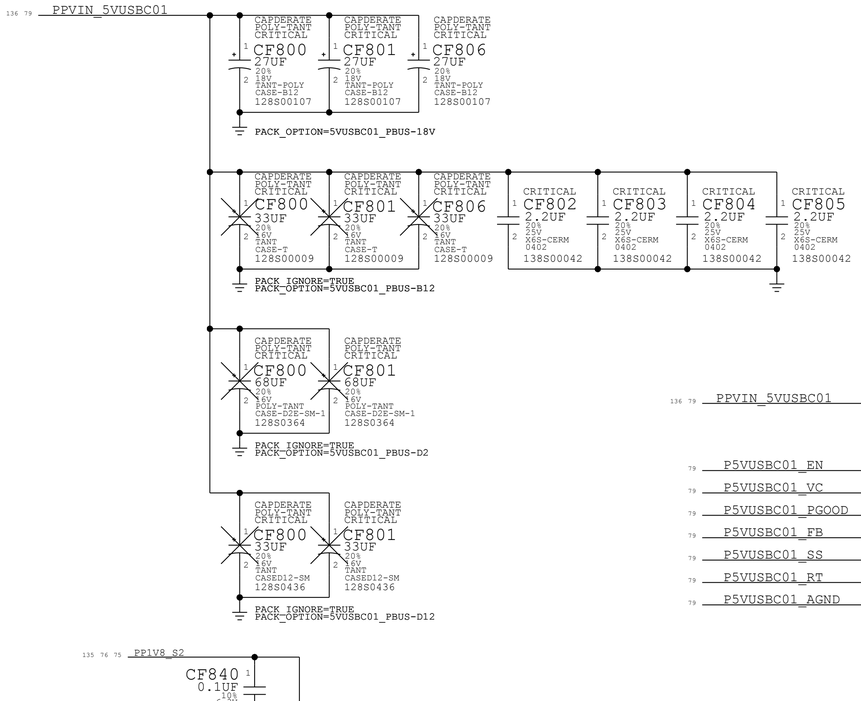
PACK_OPTION=5VUSBC01_PBUS-B12
PACK_OPTION=5VUSBC01_PBUS-D2
PACK_OPTION=5VUSBC01_PBUS-D12
PACK_OPTION=5VUSBC01_PBUS-18V

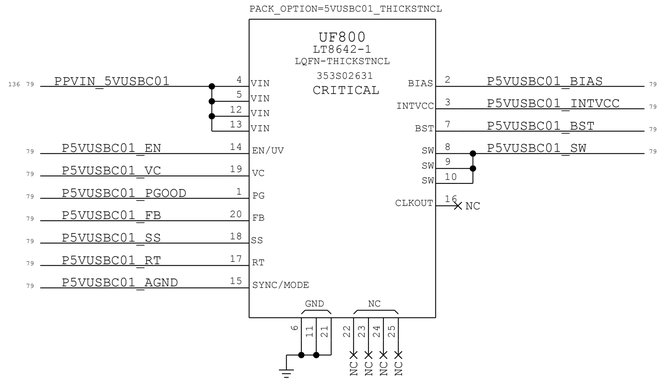
SET ONE OPTION FOR UF800

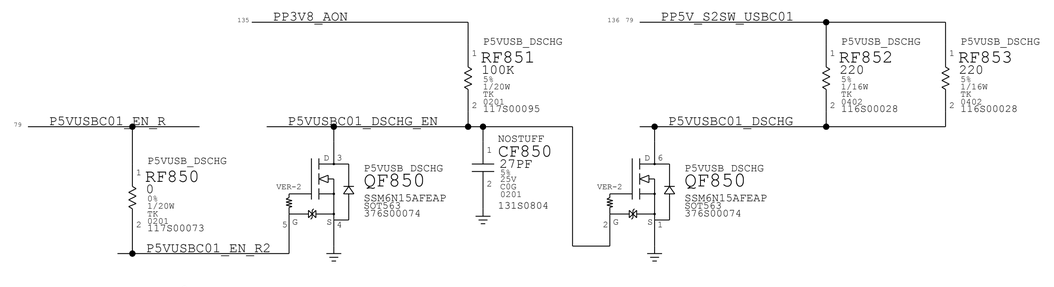
PACK_OPTION=5VUSBC01_THINSTNCL
PACK_OPTION=5VUSBC01_THICKSTNCL

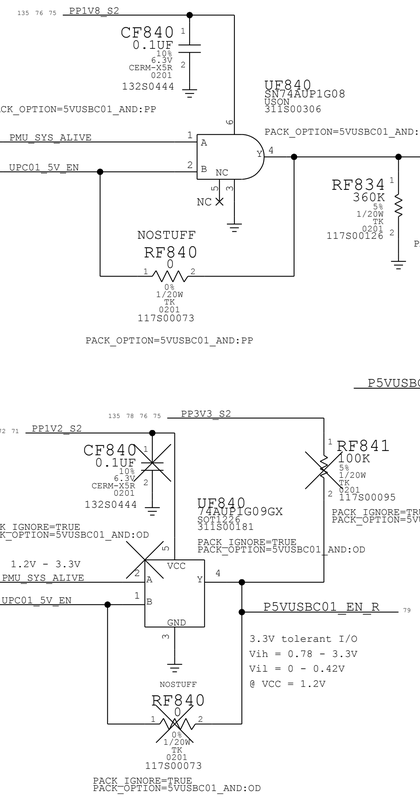
SET ONE OPTION FOR UF840 BUFFER

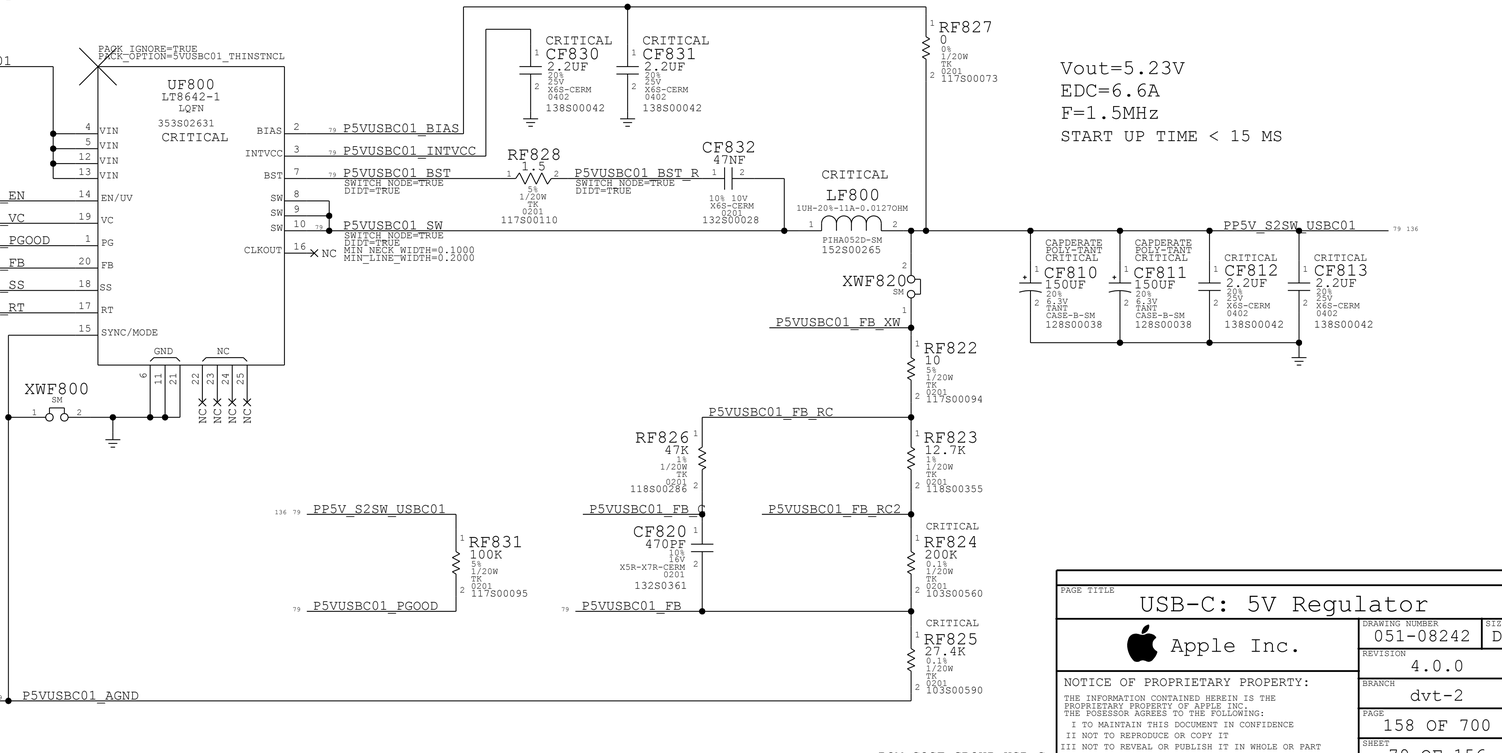
PACK_OPTION=5VUSBC01_AND:PP
PACK_OPTION=5VUSBC01_AND:OD











PAGE TITLE: USB-C: 5V Regulator

Apple Inc.

DRAWING NUMBER: 051-08242 | SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
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*** OK2INTEGRATE ***

PP1V2_ATCRTMR01_VDDIO

RF904 4.7K 5% 1/20W TK 0201 — NOSTUFF
PACK_OPTION=ATC_VR_PG-RES
P1V2_ATC01_PGOOD

XWF901 SM — PACK_IGNORE=TRUE, PACK_OPTION=ATC01_VR_MLCC-COMBO
XWF902 SM — PLACE_NEAR=UF900.8:2MM
PP3V8_ATC01_LDO → NO_XNET_CONNECTION=1

PP3V8_ATC01_VDDIO_REG — VOLTAGE=3.8V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
CF902–CF905 10UF 20% 6.3V CER-X6S 0402-COMBO
CF902–CF905 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

P1V2_ATC01_SVR_PGND — VOLTAGE=0V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000

UF900 TPS628502 SOT583 353S02660 — CRITICAL
VIN, EN, MODE_SYNC, PG, COMP_FSET, GND, SW, FB

ATC01_VDDIO_VR_EN → RF909 0Ω 1/20W TK 0201 → ATC01_VDDIO_VR_EN_R
RF901 100K 1% 1/20W TK 0201
P1V2_ATC01_AGND
P1V2_ATC01_PGOOD
RF900 100K 1% 1/20W TK 0201

LF900 CRITICAL 0.47UH-3.7A-0.034OHM PIJD16140H-SM 152S00984
DIDT=TRUE, SWITCH_NODE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
P1V2_ATC01_SW → PP1V2_ATC01_REG_XW — VOLTAGE=1.23V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
XWF904 SM — NO_XNET_CONNECTION=1
XWF903 SM — NO_XNET_CONNECTION=1
P1V2_ATC01_FB_TOP_R

P1V2_ATC01_FB_RC → RF910 3.16K 1% 1/20W TK 0201 → CF906 100PF 5% 50V C0G 0201 (131S00090) → P1V2_ATC01_AGND
P1V2_ATC01_FB_R → RF907 15K 0.1% 1/20W TK 0201 → RF908 15K 0.1% 1/20W TK 0201 → P1V2_ATC01_FB
RF906 316 1% 1/20W TK 0201
CF901 3300PF 10% 10V X7R-CERM 0201
P1V2_ATC01_FB_TOP → RF905 10 5% 1/20W TK 0201

XWF900 SM — NO_XNET_CONNECTION=1, PLACE_NEAR=UF900.8:2MM, VOLTAGE=0V

PACK_IGNORE=TRUE, PACK_OPTION=ATC01_VR_MLCC-COMBO
PP1V2_ATCRTMR01_VDDIO
CF908–CF921 10UF 20% 6.3V CER-X6S 0402-COMBO
CF908–CF921 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

Vout = 1.213V
Iout Max = 0.96A
F = 1.8 MHZ

PP3V8_AON
QF910 SSM6N37FEAP SOT563 376S00078 — CRITICAL
RF914 100K 1% 1/20W TK 0201 117S00095 — NOSTUFF
RF911 10 5% 1/5W TK 0402
RF912 10 5% 1/5W TK 0402
RF913 10 5% 1/5W TK 0402
P1V2_ATC01_DSCHG
CF929 47PF 5% 25V C0G 0201 — NOSTUFF
ATC01_P1V2_DSCHG_EN_RC
PACK_OPTION=ATC_VR_DSCHG-EN-R:NO
RF915 0Ω 1/20W TK 0201
ATC01_VDDIO_VR_EN
PACK_IGNORE=TRUE, PACK_OPTION=ATC_VR_DSCHG-EN-R:YES
PACK_IGNORE=TRUE, PACK_OPTION=ATC_VR_MLCC-DSCHG

PP1V2_ATCRTMR01_VDDIO

RF934 4.7K 5% 1/20W TK 0201 — NOSTUFF
PACK_OPTION=ATC_VR_PG-RES
P0V855_ATC01_PGOOD

XWF931 SM — PACK_IGNORE=TRUE, PACK_OPTION=ATC01_VR_MLCC-COMBO
XWF932 SM — PLACE_NEAR=UF930.8:2MM
PP3V8_ATC01_LDO → NO_XNET_CONNECTION=1

PP3V8_ATC01_VDDCIO_REG — VOLTAGE=3.8V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
CF932–CF935 10UF 20% 6.3V CER-X6S 0402-C40MBO
CF932–CF935 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

P0V855_ATC01_SVR_PGND — VOLTAGE=0V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000

UF930 TPS628502 SOT583 353S02660 — CRITICAL
VIN, EN, MODE_SYNC, PG, COMP_FSET, GND, SW, FB

ATC01_VDDCIO_VR_EN → RF939 0Ω 1/20W TK 0201 → ATC01_VDDCIO_VR_EN_R
RF931 100K 1% 1/20W TK 0201
P0V855_ATC01_AGND
P0V855_ATC01_PGOOD
RF930 100K 1% 1/20W TK 0201

LF930 CRITICAL 0.47UH-3.7A-0.034OHM PIJD16140H-SM 152S00984
DIDT=TRUE, SWITCH_NODE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
P0V855_ATC01_SW → PP0V855_ATC01_REG_XW — VOLTAGE=0.86V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
XWF934 SM — NO_XNET_CONNECTION=1
XWF933 SM — NO_XNET_CONNECTION=1
P0V855_ATC01_FB_TOP_R

P0V855_ATC01_FB_RC → RF940 3.16K 1% 1/20W TK 0201 → CF936 100PF 5% 50V C0G 0201 (131S00090) → P0V855_ATC01_AGND
P0V855_ATC01_FB_R → RF937 10K 0.1% 1/20W TK 0201 → RF938 27.4K 0.1% 1/20W TK 0201 → P0V855_ATC01_FB
RF936 1.96K 1% 1/20W TK 0201
CF931 3300PF 10% 10V X7R-CERM 0201
P0V855_ATC01_FB_TOP → RF935 10 5% 1/20W TK 0201

XWF930 SM — NO_XNET_CONNECTION=1, PLACE_NEAR=UF930.8:2MM, VOLTAGE=0V

PACK_IGNORE=TRUE, PACK_OPTION=ATC01_VR_MLCC-COMBO
PP0V855_ATCRTMR01_VDD_CIO
CF938–CF951 10UF 20% 6.3V CER-X6S 0402-COMBO
CF938–CF951 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

VOUT = 0.8621V
IOUT MAX = 0.5A
F = 1.8 MHZ

PP3V8_AON
QF940 SSM6N37FEAP SOT563 376S00078 — CRITICAL
RF944 100K 1% 1/20W TK 0201 117S00095 — NOSTUFF
RF941 10 5% 1/5W TK 0402
RF942 10 5% 1/5W TK 0402
RF943 10 5% 1/5W TK 0402
P0V855_ATC01_DSCHG
CF959 4700PF 10% 25V X5R 0201-1 — NOSTUFF
ATC01_P0V855_DSCHG_EN_RC
PACK_OPTION=ATC_VR_DSCHG-EN-R:NO
RF945 0Ω 1/20W TK 0201
ATC01_VDDCIO_VR_EN
PACK_IGNORE=TRUE, PACK_OPTION=ATC_VR_DSCHG-EN-R:YES
PACK_IGNORE=TRUE, PACK_OPTION=ATC_VR_MLCC-DSCHG

PP1V2_ATCRTMR01_VDDIO

RF964 4.7K 5% 1/20W TK 0201 — NOSTUFF
PACK_OPTION=ATC_VR_PG-RES
P0V805_ATC01_PGOOD

XWF961 SM — PACK_IGNORE=TRUE, PACK_OPTION=ATC01_VR_MLCC-COMBO
XWF962 SM — PLACE_NEAR=UF960.8:2MM
PP3V8_ATC01_LDO → NO_XNET_CONNECTION=1

PP3V8_ATC01_VDDFIXED_REG — VOLTAGE=3.8V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
CF962–CF965 10UF 20% 6.3V CER-X6S 0402-COMBO
CF962–CF965 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

P0V805_ATC01_SVR_PGND — VOLTAGE=0V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000

UF960 TPS628502 SOT583 353S02660 — CRITICAL
VIN, EN, MODE_SYNC, PG, COMP_FSET, GND, SW, FB

ATC01_VDDFIXED_VR_EN → RF969 0Ω 1/20W TK 0201 → ATC01_VDDFIXED_VR_EN_R
RF961 100K 1% 1/20W TK 0201
P0V805_ATC01_AGND
P0V805_ATC01_PGOOD
RF960 100K 1% 1/20W TK 0201

LF960 CRITICAL 0.47UH-3.7A-0.034OHM PIJD16140H-SM 152S00984
DIDT=TRUE, SWITCH_NODE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
P0V805_ATC01_SW → PP0V805_ATC01_REG_XW — VOLTAGE=0.805V, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
XWF964 SM — NO_XNET_CONNECTION=1
XWF963 SM — NO_XNET_CONNECTION=1
P0V805_ATC01_FB_TOP_R

P0V805_ATC01_FB_RC → RF970 3.16K 1% 1/20W TK 0201 → CF966 100PF 5% 50V C0G 0201 (131S00090) → P0V805_ATC01_AGND
P0V805_ATC01_FB_R → RF967 10K 0.1% 1/20W TK 0201 → RF968 30.9K 0.1% 1/20W TK 0201 → P0V805_ATC01_FB
RF966 665 1% 1/20W TK 0201
CF961 3300PF 10% 10V X7R-CERM 0201
P0V805_ATC01_FB_TOP → RF965 10 5% 1/20W TK 0201

XWF960 SM — NO_XNET_CONNECTION=1, PLACE_NEAR=UF960.8:2MM, VOLTAGE=0V

PACK_IGNORE=TRUE, PACK_OPTION=ATC01_VR_MLCC-COMBO
PP0V805_ATCRTMR01_VDD_FIXED
CF968–CF981 10UF 20% 6.3V CER-X6S 0402-COMBO
CF968–CF981 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=ATC01_VR_MLCC-REGULAR

VOUT = 8073V
IOUT MAX = 0.7A
F = 1.8 MHZ

PP3V8_AON
QF960 SSM6N37FEAP SOT563 376S00078 — CRITICAL
RF974 100K 1% 1/20W TK 0201 117S00095 — NOSTUFF
RF971 10 5% 1/5W TK 0402
RF972 10 5% 1/5W TK 0402
RF973 10 5% 1/5W TK 0402
P0V805_ATC01_DSCHG
CF989 47PF 5% 25V C0G 0201 — NOSTUFF
ATC01_P0V805_DSCHG_EN_RC
PACK_OPTION=ATC_VR_DSCHG-EN-R:NO
RF975 0Ω 1/20W TK 0201
ATC01_VDDFIXED_VR_EN
PACK_IGNORE=TRUE, PACK_OPTION=ATC_VR_DSCHG-EN-R:YES
PACK_IGNORE=TRUE, PACK_OPTION=ATC_VR_MLCC-DSCHG

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: ATC01 REGULATORS

Apple Inc.

DRAWING NUMBER: 051-08242 — SIZE: D
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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

USB HIGH-SPEED AC COUPLING

PP1V2_S2

RG062 1.5K 1% 1/20W 0201 TK — I2C_UPC2_ATCRTMR2_SCL
RG063 1.5K 1% 1/20W 0201 TK — I2C_UPC2_ATCRTMR2_SDA
RG043 47K 5% 1/20W TK 0201 — CIO_ATC2_LSTX
RG044 47K 5% 1/20W TK 0201 — CIO_ATC2_LSRX

ATCRTMR2_CFP_RCAL_NEG
CG011 10PF 5% 25V C0G 0201
RG011 200 1% 1/20W TK 0201-1
ATCRTMR2_CFP_RCAL_POS

ATCRTMR2_SFP_RCAL_NEG
CG010 10PF 5% 25V C0G 0201
RG010 200 1% 1/20W TK 0201-1
ATCRTMR2_SFP_RCAL_POS

USBC_ATC2_R2D_C_P<1>	CG020 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_R2D_P<1>	GND_VOID=TRUE
USBC_ATC2_R2D_C_N<1>	CG021 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_R2D_N<1>	GND_VOID=TRUE
USBC_ATC2_R2D_C_P<2>	CG024 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_R2D_P<2>	GND_VOID=TRUE
USBC_ATC2_R2D_C_N<2>	CG025 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_R2D_N<2>	GND_VOID=TRUE
USBC_ATC2_D2R_P<1>	CG022 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_D2R_C_P<1>	GND_VOID=TRUE
USBC_ATC2_D2R_N<1>	CG023 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_D2R_C_N<1>	GND_VOID=TRUE
USBC_ATC2_D2R_P<2>	CG026 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_D2R_C_P<2>	GND_VOID=TRUE
USBC_ATC2_D2R_N<2>	CG027 0.22UF 20% 6.3V X5R 0201	USBC_ATC2_D2R_C_N<2>	GND_VOID=TRUE

UG000
TMNB25B1-K1S1
FCCSP
OMIT_TABLE CRITICAL
338S00888 SYM 2 OF 2

USBC_ATC2_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	SFP PHY
USBC_ATC2_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N	
USBC_ATC2_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P	
USBC_ATC2_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N	
USBC_ATC2_R2D_P<1>	P7	SFP_PHY_RXTX_1_P	
USBC_ATC2_R2D_N<1>	N7	SFP_PHY_RXTX_1_N	
USBC_ATC2_R2D_P<2>	P3	SFP_PHY_RXTX_3_P	
USBC_ATC2_R2D_N<2>	N3	SFP_PHY_RXTX_3_N	
USBC_ATC2_AUX_C_P	L4	SFP_LPDP_AUX_P	
USBC_ATC2_AUX_C_N	M4	SFP_LPDP_AUX_N	
CIO_ATC2_LSTX	G1	USB4_SFP_SB_RX	
CIO_ATC2_LSRX	G2	USB4_SFP_SB_TX	
ATCRTMR2_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P	
ATCRTMR2_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N	
GND	M1	CHIP_ID_0	GPIO PERIPHERAL
ATCRTMR2_CHIPID_1	N1	CHIP_ID_1	
ATCRTMR2_BOOT_CONFIG0	H2	BOOT_CONFIG0	
ATCRTMR2_BOOT_CONFIG1	J1	BOOT_CONFIG1	
ATCRTMR2_BOOT_CONFIG2	K1	BOOT_CONFIG2	
ATCRTMR2_FORCE_DFU	C1	FORCE_DFU	
NC_ATCRTMR2_GPIO0	K2	GPIO0	
NC_ATCRTMR2_GPIO1 (NO_TEST=1)	L3	GPIO1	
NC_ATCRTMR2_GPIO2	K3	GPIO2	
NC_ATCRTMR2_GPIO3	L10	GPIO3	
ATCRTMR2_RESET_L	L2	COLD_RESET*	CLOCKS AND RESET
	M2	CFSB	
ATCRTMR2_XTAL24M_IN	F11	XI0	
ATCRTMR2_XTAL24M_OUT	E11	XO0	

CFP_PHY_RXTX_0_P	A9	USBC2_R2D_CR_P<1> (GND_VOID=TRUE)	OMIT
CFP_PHY_RXTX_0_N	B9	USBC2_R2D_CR_N<1> (GND_VOID=TRUE)	OMIT
CFP_PHY_RXTX_2_P	A5	USBC2_R2D_CR_P<2> (GND_VOID=TRUE)	OMIT
CFP_PHY_RXTX_2_N	B5	USBC2_R2D_CR_N<2> (GND_VOID=TRUE)	OMIT
CFP_PHY_RXTX_1_P	A7	USBC2_D2R_P<1>	IN
CFP_PHY_RXTX_1_N	B7	USBC2_D2R_N<1>	IN
CFP_PHY_RXTX_3_P	A3	USBC2_D2R_P<2> (GND_VOID=TRUE)	IN
CFP_PHY_RXTX_3_N	B3	USBC2_D2R_N<2> (GND_VOID=TRUE)	IN
CFP_LPDP_AUX_P	D4	USBC2_AUX_P	IN
CFP_LPDP_AUX_N	C4	USBC2_AUX_N	IN
USB4_CFP_SB_RX	F1	USBC2_CIO_LSRX	IN
USB4_CFP_SB_TX	E1	USBC2_CIO_LSTX	IN
USB4_CFP_SB_TX_DIR	H1	ATCRTMR2_LSTX_DIR	OUT
CFP_PHY_RCAL_P	C8	ATCRTMR2_CFP_RCAL_POS	
CFP_PHY_RCAL_N	D8	ATCRTMR2_CFP_RCAL_NEG	
QSPI_CS*	N11	SPI_ATCRTMR2_CS_L	
QSPI_SCLK	M11	SPI_ATCRTMR2_CLK	
QSPI_DQ0	K10	SPI_ATCRTMR2_DIO<0>	
QSPI_DQ1	K11	SPI_ATCRTMR2_DIO<1>	
QSPI_DQ2	J9	SPI_ATCRTMR2_DIO<2>	
QSPI_DQ3	J11	SPI_ATCRTMR2_DIO<3>	
I2C0_SCL	C2	I2C_ATCRTMR_SCL	IN
I2C0_SDA	D3	I2C_ATCRTMR_SDA	IN
I2C1_SCL	E2	I2C_UPC2_ATCRTMR2_SCL	IN
I2C1_SDA	D2	I2C_UPC2_ATCRTMR2_SDA	IN
I2C1_INT	B1	UPC2_ATCRTMR2_I2C_INT_L	OUT
TESTMODE	L9	ATCRTMR2_TESTMODE	TEST AND DEBUG
JTAG_SEL	C11	ATCRTMR2_JTAG_SEL	
JTAG_TCK	B11	SWD_NUB_ATCRTMR2_SWCLK	IN
JTAG_TMS	D10	SWD_NUB_ATCRTMR2_SWDIO	IN
JTAG_TDI	D9	TP_ATCRTMR2_JTAG_TDI	
JTAG_TDO	C10	ATCRTMR2_JTAG_TDO	
JTAG_TRST*	E10	TP_ATCRTMR2_JTAG_TRESET	
ANALOGMUX_OUT	F9	NC_ATCRTMR2_ANALOGMUX_OUT	
TST_CLKOUT	M10	NC_ATCRTMR2_TST_CLKOUT	
TST_CLK_LVDS_0_P	H10	NC_ATCRTMR2_CLK_LVDSP<0>	NO_TEST=1
TST_CLK_LVDS_0_N	H11	NC_ATCRTMR2_CLK_LVDSN<0>	NO_TEST=1
TST_CLK_LVDS_1_P	G11	NC_ATCRTMR2_CLK_LVDSP<1>	NO_TEST=1
TST_CLK_LVDS_1_N	G10	NC_ATCRTMR2_CLK_LVDSN<1>	NO_TEST=1

ATCRTMR2_XTAL24M_OUT
RG060 499 1% 1/20W TK 0201
197S0591 CRITICAL YG000 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-600HM
ATCRTMR2_XTAL24M_IN
ATC2_24M_O_R
CRITICAL CG060 15PF 5% 50V C0G 0201
CRITICAL 131S0831 CG061 15PF 5% 50V C0G 0201

PP0V855_ATCRTMR2_VDD_CIO
CG030 14UF 20% 4V X5R 0402-D2X-1
CG031 14UF 20% 4V X5R 0402-D2X-1
138S00149
CG032 0.1UF 10% 6.3V X6S 0201
CG033 0.1UF 10% 6.3V X6S 0201

PP1V2_ATCRTMR2_VDDIO
132S0395 CG034 0.1UF 10% 6.3V X6S 0201
138S00039 CG035 2.2UF 20% 4V X6S-CERM 0201
CG036 14UF 20% 4V X5R 0402-D2X-1
CG037 14UF 20% 4V X5R 0402-D2X-1

VDD_CIO_0	J4	VDDIO12_CIO_0	K5
VDD_CIO_0	J6	VDDIO12_CIO_0	K7
VDD_CIO_0	J8	VDDIO12_CIO_0	L6
VDD_CIO_1	F4	VDDIO12_CIO_1	D6
VDD_CIO_1	F6	VDDIO12_CIO_1	E5
VDD_CIO_1	F8	VDDIO12_CIO_1	E7
		VDDIO12_PLL_SOC0	K8
		VDDIO12_PLL_SOC1	H8
		VDDIO12_XTAL	H9
VDD_FIXED	G4	VDDIO12	E9
VDD_FIXED	G5	VDDIO12	H3
VDD_FIXED	H5	VDDIO12	K9
VDD_FIXED	H6	VDDIO12_EFUSE1	F3
VDD_FIXED_PLL	G7	VDDIO12_AMUX	F7
VDD_FIXED_XTAL	G9		
VSS	A1	VSS	H4
VSS	A2	VSS	H7
VSS	A4	VSS	J2
VSS	A6	VSS	J3
VSS	A8	VSS	J5
VSS	A10	VSS	J7
VSS	A11	VSS	J10
VSS	B2	VSS	K4
VSS	B4	VSS	K6
VSS	B6	VSS	L1
VSS	B8	VSS	L5
VSS	B10	VSS	L7
VSS	C3	VSS	L11
VSS	C5	VSS	M3
VSS	C6	VSS	M5
VSS	C7	VSS	M6
VSS	C9	VSS	M7
VSS	D1	VSS	M9
VSS	D5	VSS	N2
VSS	D7	VSS	N4
VSS	D11	VSS	N6
VSS	E3	VSS	N8
VSS	E4	VSS	N10
VSS	E6	VSS	P1
VSS	E8	VSS	P2
VSS	F2	VSS	P4
VSS	F5	VSS	P6
VSS	F10	VSS	P8
VSS	G3	VSS	P10
VSS	G6	VSS	P11
VSS	G8		

PP0V805_ATCRTMR2_VDD_FIXED
CG040 0.1UF 10% 6.3V X6S 0201
CG041 0.1UF 10% 6.3V X6S 0201
CG042 2.2UF 20% 4V X6S-CERM 0201
CG043 2.2UF 20% 4V X6S-CERM 0201
CG044 2.2UF 20% 4V X6S-CERM 0201
CG045 14UF 20% 4V X5R 0402-D2X-1
CG046 14UF 20% 4V X5R 0402-D2X-1

PP0V805_ATCRTMR2_VDD_FIXED
CG050 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UG000.G7:5MM

PPVDD_FIXED_ATCRTMR2_XTAL_R
PP0V805_ATCRTMR2_VDD_FIXED
RG051 10 1% 1/20W TK 0201 VOLTAGE=0.805V
CG051 4UF 20% 2.5V X6S 0201
117S00094
138S00329

PP1V2_ATCRTMR2_VDDIO
138S00039 CG052 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=UG000.K8:5MM

PP1V2_ATCRTMR2_VDDIO_XTAL_F
155S0644 FLG000 240-OHM-0.2A-0.9-OHM 0201
VOLTAGE=1.2V
PP1V2_ATCRTMR2_VDDIO
CG063 2.2UF 20% 4V X6S-CERM 0201
138S00039
CG062 0.1UF 10% 6.3V X6S 0201
132S0395

Connect to GND directly or via a resistor
GND
PP1V2_ATCRTMR2_VDDIO
132S0395 CG064 0.1UF 10% 6.3V X6S 0201

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RG045 47K 5% 1/20W TK 0201
ATCRTMR2_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RG047 47K 5% 1/20W TK 0201
ATCRTMR2_JTAG_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RG040 10K 5% 1/20W TK 0201
ATCRTMR2_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

SPI_ATCRTMR2_DIO<0> — RG097 33 1/20W 5% TK 0201 — SPI_ATCRTMR2_R_DIO<0>
SPI_ATCRTMR2_DIO<1> — RG098 33 1/20W 5% TK 0201 — SPI_ATCRTMR2_R_DIO<1>

PP1V2_ATCRTMR2_VDDIO
RG090 3.3K 5% 1/20W TK 0201
NOSTUFF RG091 3.3K 5% 1/20W TK 0201
NOSTUFF RG092 3.3K 5% 1/20W TK 0201
NOSTUFF RG093 3.3K 5% 1/20W TK 0201
CG090 1.0UF 20% 6.3V X5R 0201-1

UG090
64MBIT-1.2V
W25Q64NE
XSON-1
OMIT_TABLE CRITICAL 335S00574

SPI_ATCRTMR2_CLK	RG094 33	SPI_ATCRTMR2_CLK_R	CLK
SPI_ATCRTMR2_CS_L			CS*
SPI_ATCRTMR2_DIO<2>	RG095 33	SPI_ATCRTMR2_R_DIO<2>	WP*(IO2)
SPI_ATCRTMR2_DIO<3>	RG096 33	SPI_ATCRTMR2_R_DIO<3>	HOLD*(IO3)
		SPI_ATCRTMR2_R_DIO<0>	DI(IO0)
		SPI_ATCRTMR2_R_DIO<1>	DO(IO1)

PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_ATCRTMR2_VDDIO
UG090
64MBIT-1.2V
GD25UF64E
WLCSP-COMBO
VCC CRITICAL
OMIT_TABLE 335S00638

SPI_ATCRTMR2_CLK_R	D2	SCLK	
SPI_ATCRTMR2_CS_L	B3	CS*	
SPI_ATCRTMR2_R_DIO<2>	D3	IO2	
SPI_ATCRTMR2_R_DIO<3>	C2	IO3	
	E2	SI(IO0)	SPI_ATCRTMR2_R_DIO<0>
	C3	SO(IO1)	SPI_ATCRTMR2_R_DIO<1>
	A2	NC	NC
	A3	NC	NC
	F2	NC	NC
	F3	NC	NC
	E3	VSS	

PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

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Apple Inc.

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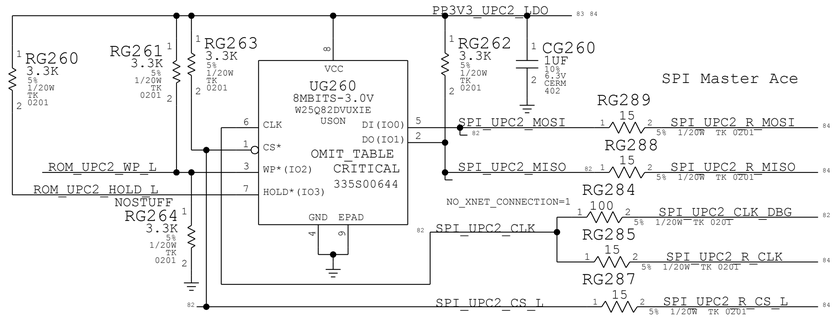
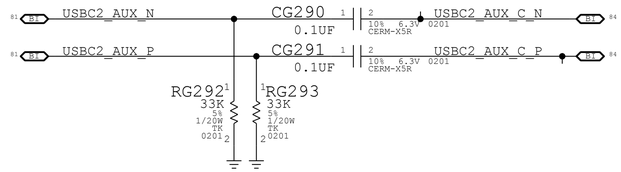
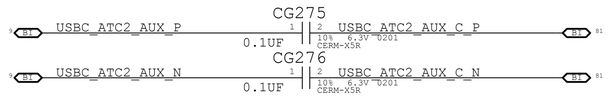
*** OK2INTEGRATE ***





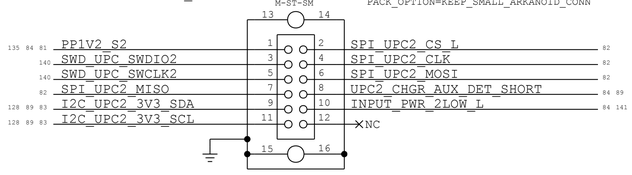


ACE ARKANOID CONN

JG200
USBC_DBG 505070-1222 M-ST-SM
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

AARDVARKANOID CONN

JG202
USBC_DBG 505070-1222 M-ST-SM
PACK_OPTION=KEEP_SMALL_ARKANOID_CONN



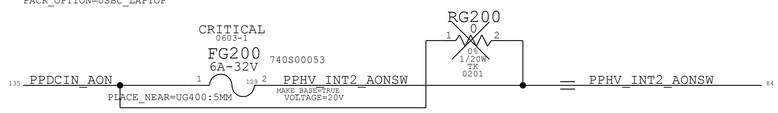
HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 1 ATC2

Apple Inc.

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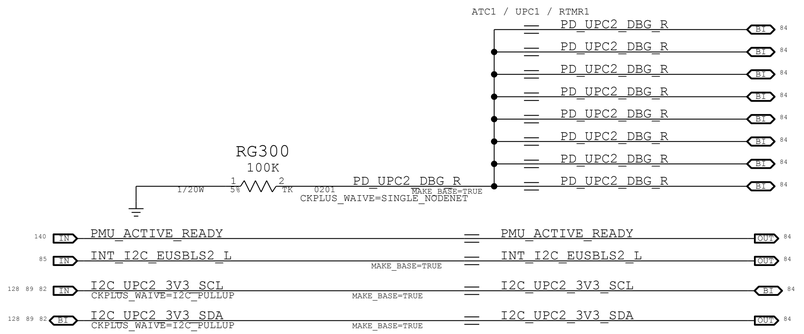
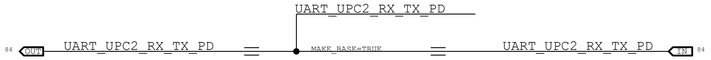
*** OK2INTEGRATE ***

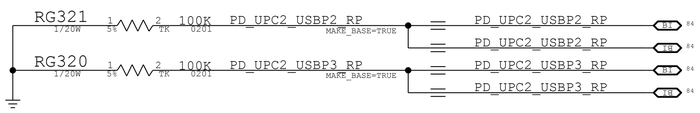
UPC 2 GPIOs

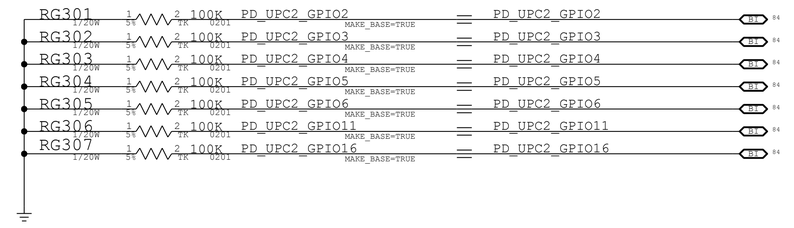


UART_UPC2_RX_TX_PD



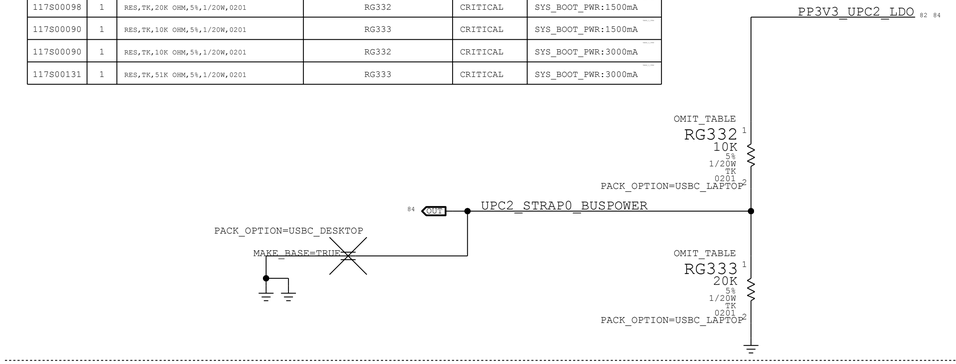
Unused ports

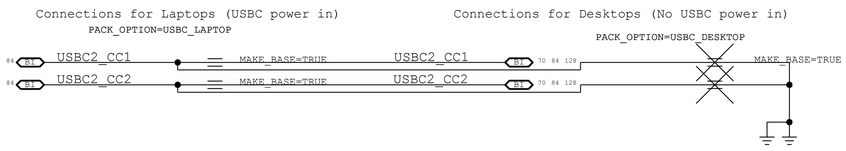




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00073	1	RES,TK,0 OHM, 1A MAX,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:DEFAULT_500mA
117S00073	1	RES,TK,0 OHM, 1A MAX,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:DISABLED
117S00131	1	RES,TK,51K OHM,5%,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:1000mA
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:1000mA
117S00098	1	RES,TK,20K OHM,5%,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:1500mA
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RG332	CRITICAL	SYS_BOOT_PWR:3000mA
117S00131	1	RES,TK,51K OHM,5%,1/20W,0201	RG333	CRITICAL	SYS_BOOT_PWR:3000mA

STAP0/BUSPOWER

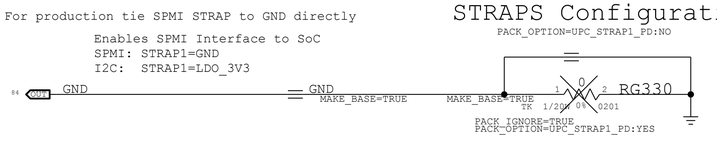




STRAPS Configurations

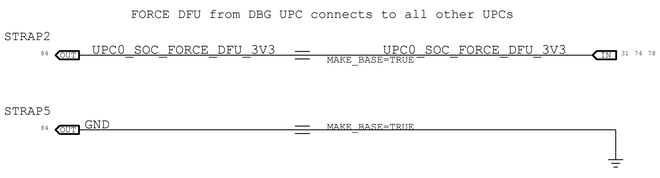
For production tie SPMI STRAP to GND directly

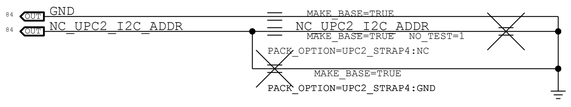
Enables SPMI Interface to SoC
SPMI: STRAP1=GND
I2C: STRAP1=LDO_3V3



UPC0: STRAP3=GND STRAP4=GND
UPC1: STRAP3=NC STRAP4=GND
UPC2: STRAP3=GND STRAP4=NC (LEGACY) GND (CURRENT)
UPC5: STRAP3=NC STRAP4=140K

FORCE DFU from DBG UPC connects to all other UPCs

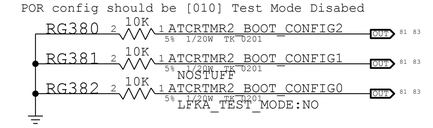


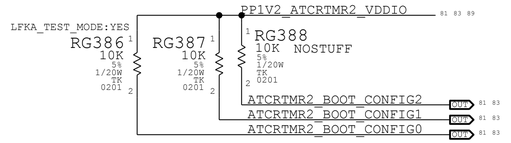


Is UPCx_5V_EN being used?

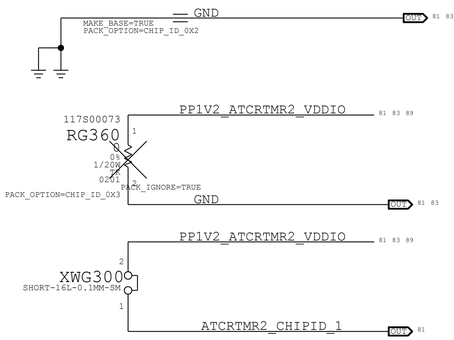
ATCRTMR Boot Config

[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

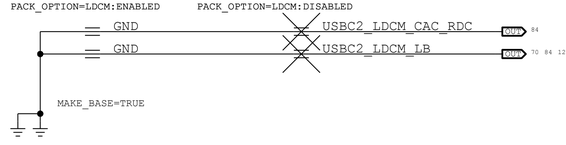




ATCRTMR2 CHIP 0X02/0X03



LDCM



BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Support 2 ATC2

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
PAGE: 163 OF 700
SHEET: 83 OF 156

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*** OK2INTEGRATE ***

MAX 100uF TOTAL ON RAIL

82 PPHV_INT2_AONSW

136 PP5V_S2SW_USBC23

136 PP5V_S2SW_USBC23

1 CG406 2 138S00123 10UF 20% 10V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

OMIT_TABLE

UG400 SN2012024 BGA

POWER

DIGITAL CORE I/O & CONTROL

TYPE-C

PORT MUX

	M22	HRESET		
84 PD_UPC2_MRESET	H18	GPIO14_MRESET		
85 82 83 OUT ATCRTMR2_RESET_L	B4	GPIO15_RESETZ		
82 OUT UPC2_SER_DBG	F26	GPIO0		
83 IN PMU_ACTIVE_READY	D18	GPIO1		
83 IN PD_UPC2_GPIO2	K24	GPIO2		
83 OUT PD_UPC2_GPIO3	L21	GPIO3	PU	
83 OUT PD_UPC2_GPIO4	J25	GPIO4		
83 OUT PD_UPC2_GPIO5	J9	GPIO5		
83 IN PD_UPC2_GPIO6	C1	GPIO6		
87 83 OUT UPC23_5V_EN	C5	GPIO7		
82 83 OUT ATCRTMR2_FORCE_DFU	F10	GPIO8		
82 81 IN UPC2_ATCRTMR2_I2C_INT_L	H10	GPIO9	PU	
83 IN INT_T2C_EUSBLS2_L	A3	GPIO10	PU	
83 BI PD_UPC2_GPIO11	L25	GPIO11		
141 83 OUT INPUT_PWR_2LOW_L	E11	GPIO12	PU	
83 OUT PD_UPC2_GPIO16	M26	GPIO16_DFU_BOOTED_L		
141 OUT UPC_PMU_RESET_1V2	G19	GPIO17_FORCE_RST_REQ		
83 BI USBC2_CIO_LSTX	L13	GPIO18_LSTXRX		
83 OUT USBC2_CIO_LSRX	C3	GPIO19_LSRX		
89 82 OUT UPC2_CHGR_AUX_DET_SHORT	N23	GPIO20_SS_HOLD		
84 IN ATCRTMR2_LSTX_DIR	G25	GPIO21_LSX_DIR		
83 UPC2_STRAP0_BUSPOWER	J17	STRAP0_BUSPOWER		
83 GND	L27	STRAP1_I2C_SPMI_SEL		
83 IN UPC0_SOC_FORCE_DFU_3V3	J13	STRAP2_DFU_EN		
83 GND	M20	STRAP3_I2C_ADDR0		
83 NC_UPC2_I2C_ADDR	N21	STRAP4_I2C_ADDR1		
83 GND	J21	STRAP5_VDDIO_CFG		
UPC2_R_OSC	B10	R_OSC		
NC_UPC2_AID0 NO_TEST=1	F14	AID0		
NC_UPC2_AID1 NO_TEST=1	G15	AID1		
NC_UPC2_AID2 NO_TEST=1	H14	AID2		
NC_UPC2_AID3 NO_TEST=1	E15	AID3		
89 82 81 BI I2C_UPC2_ATCRTMR2_SDA	A25	I2CC_SDA		
89 82 81 BI I2C_UPC2_ATCRTMR2_SCL	B26	I2CC_SCL		
83 BI I2C_UPC2_3V3_SDA	K28	I2C1_SDA_GPIO23		
83 IN I2C_UPC2_3V3_SCL	J27	I2C1_SCL_GPIO22		
NC_INT_T2C_UPC2_L NO_TEST=1	H26	I2C_IRQ1Z		
89 BI SPMI_UPC2_DATA	N25	SPMI_I2C2_DATA		
89 IN SPMI_UPC2_CLK	M24	SPMI_I2C2_CLK		
NC_INT_I2C_SMC_UPC2_L NO_TEST=1	K26	I2C_IRQ2Z		
82 OUT SPI_UPC2_R_CLK	G27	SPI_CLK		
82 OUT SPI_UPC2_R_MOSI	H28	SPI_COPI		
82 IN SPI_UPC2_R_MISO	F28	SPI_CIPO		
82 OUT SPI_UPC2_R_CS_L	E27	SPI_CSZ		
140 12 BI SWD_UPC_SWDIO2	E25	SWD_DATA	IPU	
140 12 BI SWD_UPC_SWCLK2	E23	SWD_CLK	IPU	
84 83 IN UART_UPC2_RX_TX_PD	D28	UART_RX		
83 OUT UART_UPC2_RX_TX_PD	C27	UART_TX		
83 BI USB2_UPC2_P1_P	A15	USB_RP1_P		
83 BI USB2_UPC2_P1_N	B16	USB_RP1_N		
83 BI PD_UPC2_USBP2_RP	A17	USB_RP2_P		
83 BI PD_UPC2_USBP2_RP	B18	USB_RP2_N		
83 BI PD_UPC2_USBP3_RP	A19	USB_RP3_P		
83 BI PD_UPC2_USBP3_RP	B20	USB_RP3_N		
82 BI USBC2_AUX_C_P	D14	AUX_P		
82 BI USBC2_AUX_C_N	C15	AUX_N		
84 PD_UPC2_HPD	G11	GPIO13_HPDTXRX		
83 BI PD_UPC2_DBG_R	E19	DEBUG0_GPIO24		
83 BI PD_UPC2_DBG_R	F18	DEBUG1_GPIO25		
83 BI PD_UPC2_DBG_R	H22	DEBUG2_GPIO26		
83 BI PD_UPC2_DBG_R	D22	DEBUG3_GPIO27		
83 BI PD_UPC2_DBG_R	G23	DEBUG4_GPIO28		
83 BI PD_UPC2_DBG_R	F22	DEBUG5_GPIO29		
83 BI PD_UPC2_DBG_R	C23	DEBUG6_GPIO30		
83 BI PD_UPC2_DBG_R	D26	DEBUG7_GPIO31		

1 RG405 2 1M 5% 1/20W TK 0201 — UART_UPC2_RX_TX_PD 83 84

1 RG406 2 100K 5% 1/20W TK 0201 — PD_UPC2_MRESET 84

1 RG407 2 100K 5% 1/20W TK 0201 — PD_UPC2_HPD 84

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

CRITICAL RG403 1 15K 0.1% 1/20W TK 0201 2 103S00582

Configurable as SPMI or I2C Port 2
SMC SPMI: 0X9
AP SPMI: 0X8
I2C: 0X3B

PPVBUS_USBC2 70 128

CG401 1 1UF 10% 25V X5R 0402 2

DG400 DSNG NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2 135

CG400 1 10UF 20% 6.3V CERM 0402 2

PP1V2_S2 81 82 135

CG402 1 1.0UF 20% 6.3V X5R 0201-1 2

MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750 VOLTAGE=3.3V

PP3V3_UPC2_LDO 82 83

CG408 1 10UF 20% 6.3V CERM 0402 2

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.0750 VOLTAGE=1.8V

PP1V8_UPC2_LDO

CG417 1 10UF 20% 6.3V CERM 0402 2

PP1V8_S2 135

CG403 1 0.1UF 10% 6.3V CERM-X5R 0201 2

VIN_3V3	C19	
VDDIO	C25	
LDO_3V3	B22	
LDO_1V8	A23	
VIN_LV	A27, B28	
VOUT_LV	B24	UPC2_ATCRTMR2_PWR_EN 82 86 (cap needed when used as power source)
SS	A5	UPC2_SS
LDO_CORE	A21	PP1V5_UPC2_LDO_CORE — VOLTAGE=1.5V MIN_LINE_WIDTH=0.2800 MIN_NECK_WIDTH=0.0750
C_CC1	M16, N15	USBC2_CC1
C_CC2	M18, N17	USBC2_CC2
RPD_G1	L17	USBC2_CC1 BI 83
RPD_G2	L19	USBC2_CC2 BI 83
C_USB_TP	A11	USBC2_USB_TOP_P BI 70
C_USB_TN	A13	USBC2_USB_TOP_N BI 70
C_USB_BP	B12	USBC2_USB_BOT_P BI 70
C_USB_BN	B14	USBC2_USB_BOT_N BI 70
C_SBU1	C11	USBC2_SBU1 BI 70 128
C_SBU2	D10	USBC2_SBU2 BI 70 128
3V3 LDCM	B8	USBC2_LDCM_CAC_RDC
3V3 LDCM_LB	C7	USBC2_LDCM_LB IN 70 83 128
3V3 LDCM_SENSE	A7	USBC2_LDCM_SW
3V3 LDCM_COMP	B6	USBC2_LDCM_COMP
3V3 LDCM_SW	A9	USBC2_LDCM_SW

CG405 1 10UF 20% 6.3V CERM 0402 2

CG409 1 0.68UF 5% 6.3V X6S 0402 2

PACK_OPTION=ACE2_SS_CAP

PACK_OPTION=ACE2_SS_GND GND MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500

BI 70 83 128

MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500

BI 70 83 128

CG414 1 220PF 5% 50V C0G 0201-1 2

CG413 1 220PF 5% 50V C0G 0201-1 2

LDCM circuit subject to change

PACK_OPTION=LDCM:ENABLED

CRITICAL CG420 2.2UF 10% 35V X5R 0402 1 2 138S00488

CAC

RDC

PACK_OPTION=LDCM:ENABLED

CRITICAL RG411 402K 1% 1/20W TK 0201 1 2 118S00666

PACK_IGNORE=TRUE

PACK_OPTION=LDCM:DISABLED RG414 100K 5% 1/20W TK 0201 1 2

PACK_OPTION=LDCM:DISABLED 10K RG415 1 2 5% 1/20W 0201 TK

PACK_OPTION=LDCM:ENABLED R2 CRITICAL 4.99K RG410 1 2 1/20W 0.1% 0201 TK 103S00656

PACK_OPTION=LDCM:ENABLED

PACK_OPTION=LDCM:ENABLED

CRITICAL RG413 R1 10K 1/20W 0.1% 0201 TK

128 70 IN USBC2_LDCM 1 2 USBC2_LDCM_R 103S00593

GROUND

GND A1 B2 K16 K20 M28 N19 N27

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Port Controller ATC2

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D

REVISION: 4.0.0

BRANCH: dvt-2

PAGE: 164 OF 700

SHEET: 84 OF 156

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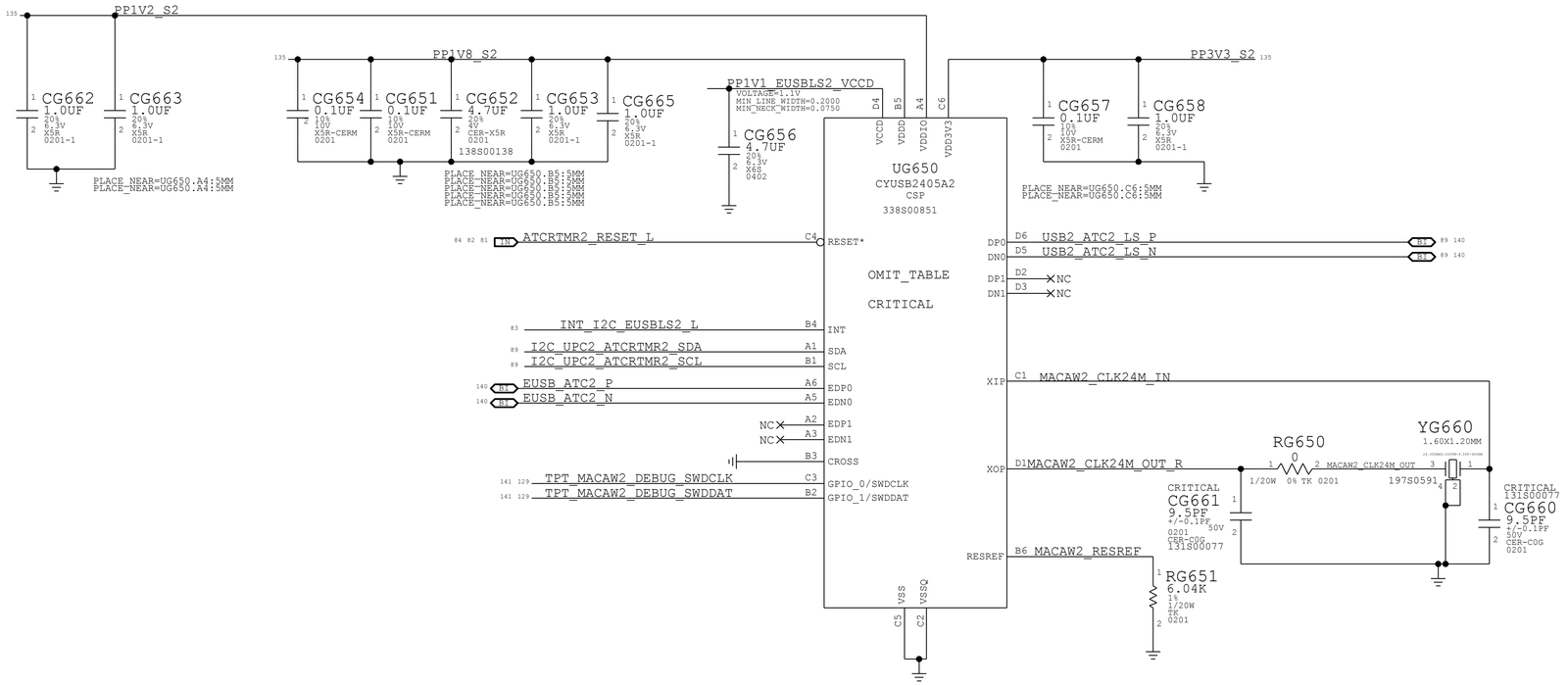
*** OK2INTEGRATE ***

MACAW 2



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: USB2 RPT2

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 166 OF 700
SHEET 85 OF 156

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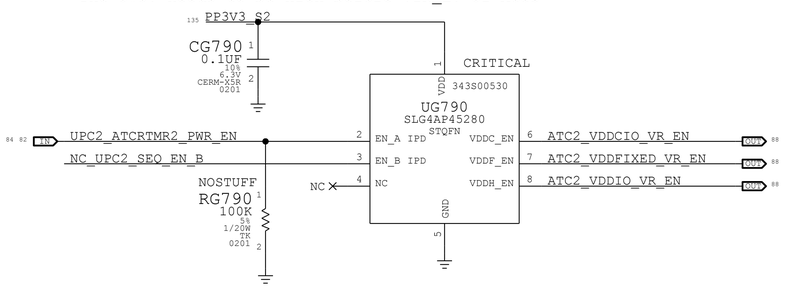
*** OK2INTEGRATE ***

Sequencing Requirements: 3.3V to UG790 --> system 1.2V (UG400 VDDIO) same time or before System 1.8V (UG400 VIN_LV pin)

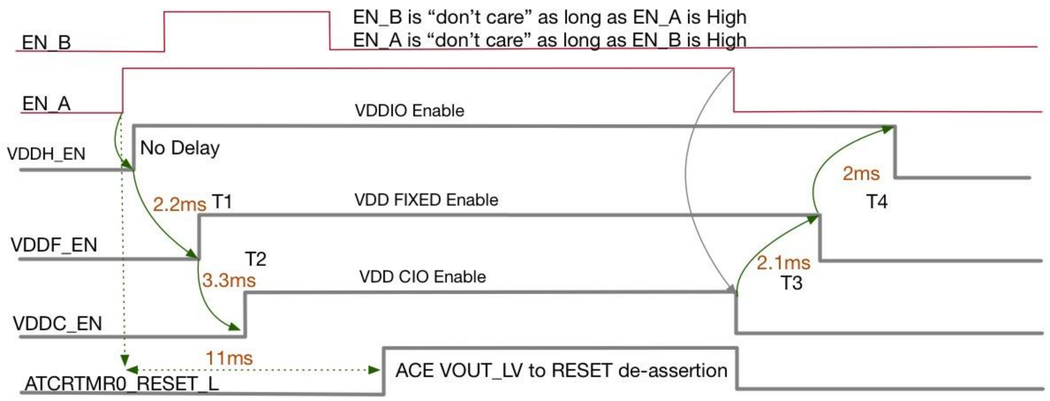
Power-up Sequence Requirements: 3.3_S2 to UG790 --> system 1.2V (UG400 VDDIO) same time or before system 1.8V (UG400) VIN_LV pin)

Power-down Sequence Requirements: The 1.8V first or at the same time as 1V2 --> 3V3_S2 needs to get disabled at minimum of 6ms from when 1V8 is discharged to below 300mV

The 3.3V needs to be HIGH before VIN_LV of Aces



Note1: As long as EN_A or EN_B are High, the outputs stay High
Note2: Outputs are an ORed and delayed version of EN_A or EN_B



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: HS Level Shifters ATC2

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 167 OF 700
SHEET 86 OF 156

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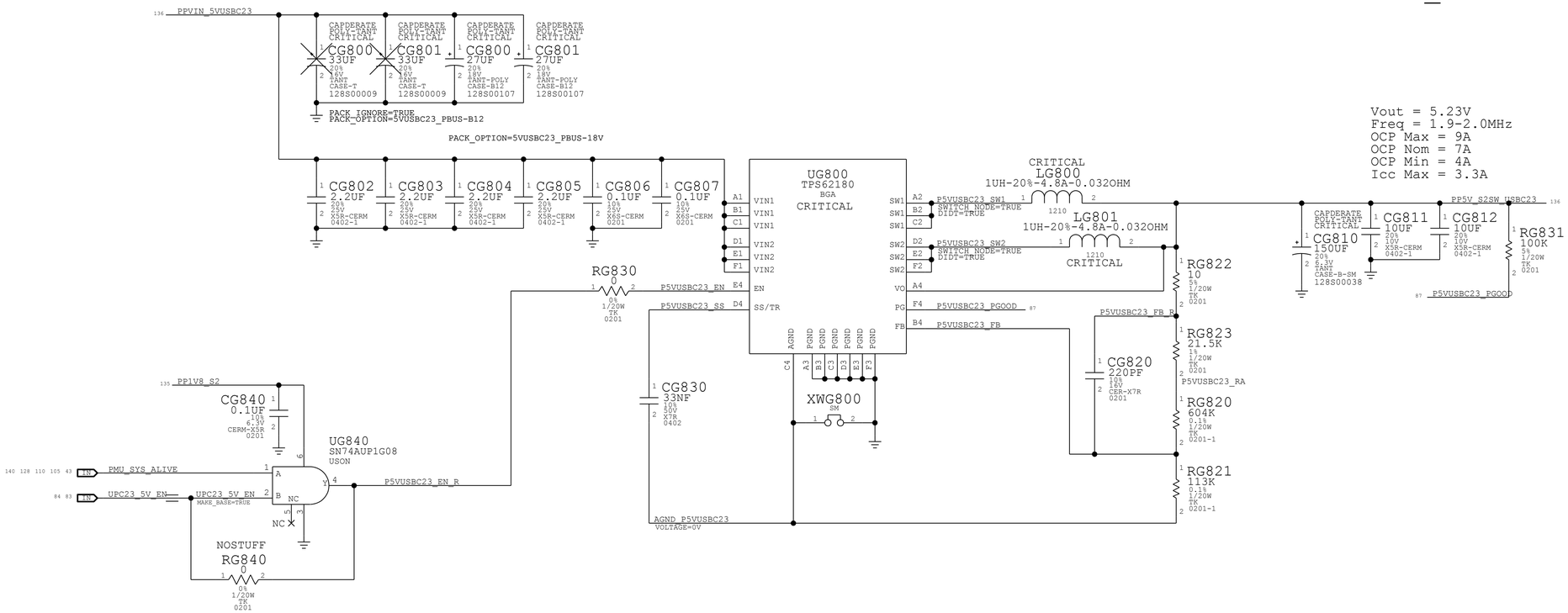
*** OK2INTEGRATE ***

Set one option for the PBUS caps
PACK_OPTION=5VUSBC23_PBUS-B12
PACK_OPTION=5VUSBC23_PBUS-18V



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: 5V Regulator

Apple Inc.

DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
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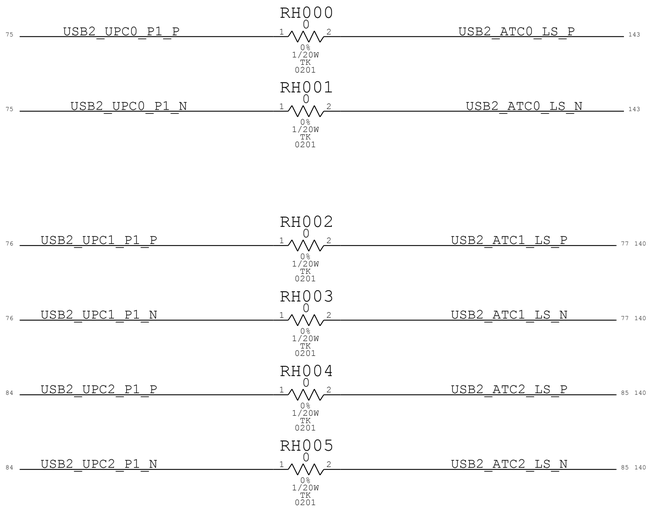
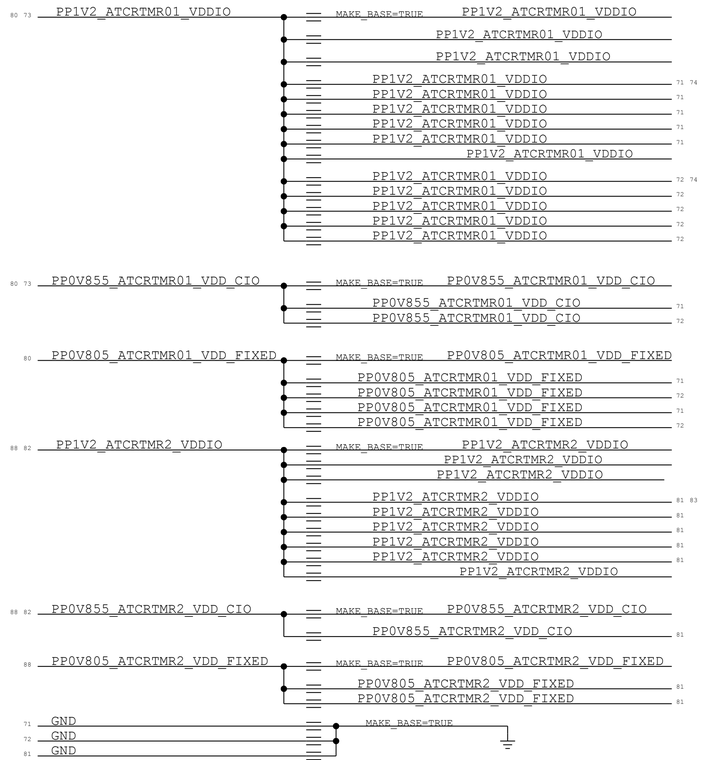
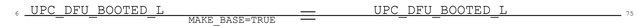
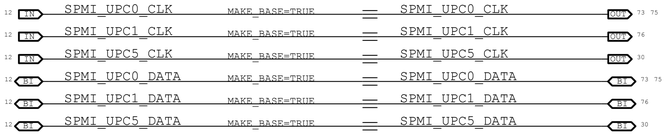


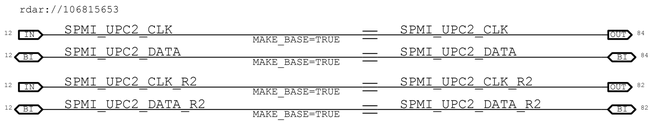




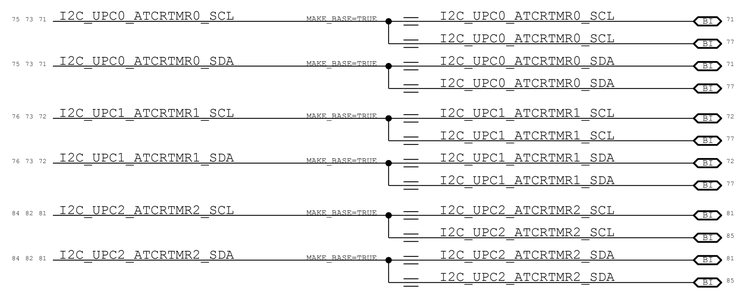
ALIASES FOR SPMI

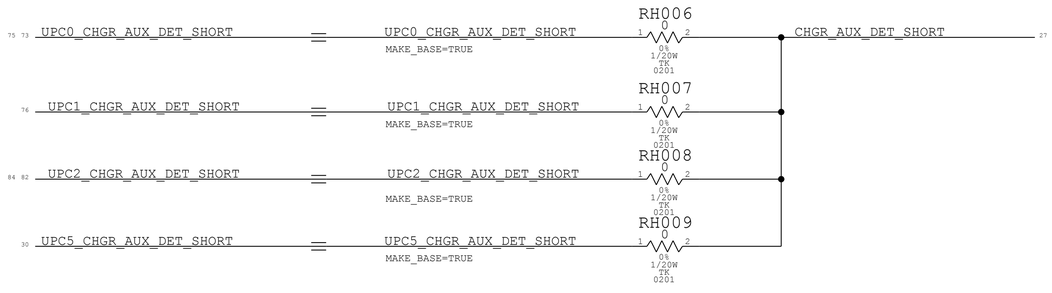


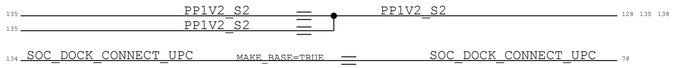
rdar://106815653

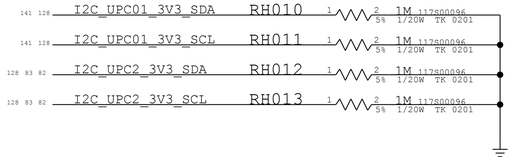


ALIASES FOR I2C









BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: SUPPORT

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HDMI CONNECTOR THRU-HOLE

JH500
RCPT-HDMI-ACC-BLK-X2094
F-RT-TH

HDMI_DATA_CONN_P<2> (91 90) GND_VOID=TRUE
HDMI_DATA_CONN_N<2> (91 90) GND_VOID=TRUE
HDMI_DATA_CONN_P<0> (91 90) GND_VOID=TRUE
HDMI_DATA_CONN_N<0> (91 90) GND_VOID=TRUE
HDMI_CEC_CONN (128 90)
HDMI_DDC_5V_CONN_SCL (128 90)
HDMI_HPD_IN_CONN (128 90)

TMDS_DATA2+ 1
TMDS_DATA2- 3
TMDS_DATA1_SHLD 5
TMDS_DATA0+ 7
TMDS_DATA0- 9
TMDS_CLK_SHLD 11
CEC 13
SCL 15
DDC/CEC/HEC GND 17
HOT_PLUG_DETECT 19

TMDS_DATA2_SHLD 2
TMDS_DATA1+ 4
TMDS_DATA1- 6
TMDS_DATA0_SHLD 8
TMDS_CLK+ 10
TMDS_CLK- 12
RSVD 14
SDA 16
+5V_PWR 18

IO20 20
IO22 22
IO24 24
IO26 26
IO28 28
IO30 30
IO32 32
IO21 21
IO23 23
IO25 25
IO27 27
IO29 29
IO31 31
IO33 33

OMIT_TABLE
SHLD PINS
514S00359

PACK_IGNORE=TRUE
PACK_OPTION=HDMICONN:PORTABLES_16

HDMI_DATA_CONN_P<1> (91 90)
HDMI_DATA_CONN_N<1> (91 90)
HDMI_CLK_CONN_P (91 90)
HDMI_CLK_CONN_N (91 90)
HDMI_RSVD (90 128)
HDMI_DDC_5V_CONN_SDA (90 128)
PP5V0_HDMI_DDC_CONN (90 94 128)

117S00073
RH525
0
0% 1/20W TK 0201
PACK_IGNORE=TRUE
PACK_OPTION=HDMICONN:PORTABLES_16

HDMI CONNECTOR THRU-HOLE

JH500
RCPT-HDMI-ACC-BLK-X1982
F-RT-TH

(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)

(0.5A OVER-CURRENT LIMIT IMPLEMENTED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S00359	1	CONN,RCPT,HDMI,ACC BLK,X2094	JH500	CRITICAL	HDMICONN:PORTABLES_16_BTN1
514S00509	1	CONN,RCPT,HDMI,BTN2,TALL,X2757	JH500	CRITICAL	HDMICONN:PORTABLES_16_BTN2
514S00360	1	CONN,RCPT,HDMI,ACC BLK,X1982	JH500	CRITICAL	HDMICONN:PORTABLES_14_BTN1
514S00510	1	CONN,RCPT,HDMI,BTN2,X2757	JH500	CRITICAL	HDMICONN:PORTABLES_14_BTN2

OMIT_TABLE
SHLD PINS
514S00360

PACK_OPTION=HDMICONN:PORTABLES_14

RH525
0
0% 1/20W TK 0201
PACK_OPTION=HDMICONN:PORTABLES_14

HDMI CONNECTOR THRU-HOLE

JH500
HDMI-RCPT-X2655
F-RT-TH

SHLD PINS
514-00230

PACK_IGNORE=TRUE
PACK_OPTION=HDMICONN:DESKTOP

RH525
0
0% 1/20W TK 0201
PACK_IGNORE=TRUE
PACK_OPTION=HDMICONN:DESKTOP

155S0831
FLH500
600-OHM-25%-1.3A-0.15OHM
0603

PP5V0_HDMI_DDC_CONN VOLTAGE=5V
PP5V0_HDMI_DDC_LDSW VOLTAGE=5V

DZH505
5.5V-6.2PF
0201-THICKSTNCL
377S0183

CH512 1UF 10% 25V X5R 402 138S0683
CH511 0.1UF 10% 16V X5R-CERM 0201 132S0288
CH515 0.1UF 10% 16V X5R-CERM 0201 132S0288

PP5V_S2_HDMI (135 94 90)

117S00087
RH527 4.7K 5% 1/20W TK 0201

TPH501 TP-P4 HDMI_5V_FAULT

UH502
FFF2495C
CSP
CRITICAL
VIN
VOUT
353S01211ISET
OCFLAGB
GND
ON
OVERCURRENT PROTECTION

HDMI_5V_ON
HDMI_5V_ISET

RH528 0 (NI) 1/20W TK 0201 117S00073
RH526 2.32K 1% 1/20W TK 0201 118S00784

CH514 0.1UF 10% 16V X5R-CERM 0201 132S0288
CH516 12PF 5% 25V NP0-C0G 0201 131S0445
CH517 3.0PF +/-0.1PF 25V NP0-C0G 0201 131S0439
CH518 1.8PF +/-0.1PF 25V C0G 201 131S0198

PP5V_S2_HDMI (90 94 135)
PP5V0_HDMI_DDC_CONN (90 94 128)

DH507
NSR0620P2XXG
SOD-923-HF
371S0695
VTH(MAX) = 1.15V

PP5V0_S2SW_HDMI_D VOLTAGE=5V

RH506 2.2K 5% 1/20W TK 0201 117S00099
RH505 2.2K 5% 1/20W TK 0201 117S00099

TPH502 TP-P4

CRITICAL
LH504
FERR-470-OHM-215MA-1.5OHM
0201
155S0694

HDMI_CEC_CONN (128 90)
HDMI_CEC (BI 92 93)

NOSTUFF
CH504 22PF 5% 25V C0G 0201

LH501
FERR-470-OHM-215MA-1.5OHM
0201 CRITICAL 155S0694

HDMI_DDC_5V_CONN_SCL (128 90)
131S0866

NOSTUFF
CH505 18PF 5% 25V C0G 0201

HDMI_DDC_5V_FLT_SCL
RH509 33 5% 1/20W TK 0201 117S00122
HDMI_DDC_5V_SCL (BI 92 94 141)

LH502
FERR-470-OHM-215MA-1.5OHM
0201 CRITICAL 155S0694

HDMI_DDC_5V_CONN_SDA (128 90)
131S0807

NOSTUFF
CH506 18PF 5% 25V C0G 0201

HDMI_DDC_5V_FLT_SDA
RH510 33 5% 1/20W TK 0201 117S00122
HDMI_DDC_5V_SDA (BI 92 94 141)

LH503
FERR-470-OHM-215MA-1.5OHM
0201 CRITICAL 155S0694

HDMI_HPD_IN_CONN (128 90)

HDMI_HPD_IN_FLT
RH511 0 0% 1/20W TK 0201 117S00073
HDMI_HPD_IN (OUT 92 93 94 141)

DZH503 ESD8011 X3DFN2-THICKSTNCL CRITICAL 377S00031
DZH502 ESD8011 X3DFN2-THICKSTNCL CRITICAL 377S00031
DZH501 ESD8011 X3DFN2-THICKSTNCL CRITICAL 377S00031
DZH500 ESD8011 X3DFN2-THICKSTNCL CRITICAL 377S00031

CH507 220PF 10% 25V X7R-CERM 201 132S0212

SERIES R VALUES TO BE CONFIRMED

PP3V3_AWAKESW_DP2HDMI (94 93 92)

DATA_FILT CH508 0.1UF 10% 6.3V CERM-X5R 0201 132S0444
DATA_FILT RH512 100K 5% 1/20W TK 0201 117S00095

QH501 NTZD3155C SOT-563-HF 376S0636 P-CHN

HDMI_PIND_VBIAS (OUT 91)

DATA_FILT RH513 10K 5% 1/20W TK 0201 117S00090
DATA_FILT CH509 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

PIND_PFET_EN

DP2HDMI_1.5G_FILT_EN	PIN DIODE	FILTER
LOW	UNBIASED	OFF
HI	BIASED	ON

DP2HDMI_1.5G_FILT_EN (92 IN)

QH501 NTZD3155C SOT-563-HF 376S0636 N-CHN
VTH = 0.5V - 1V MAX

DATA_FILT RH514 100K 5% 1/20W TK 0201 117S00095

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: CONNECTOR

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*** OK2INTEGRATE***

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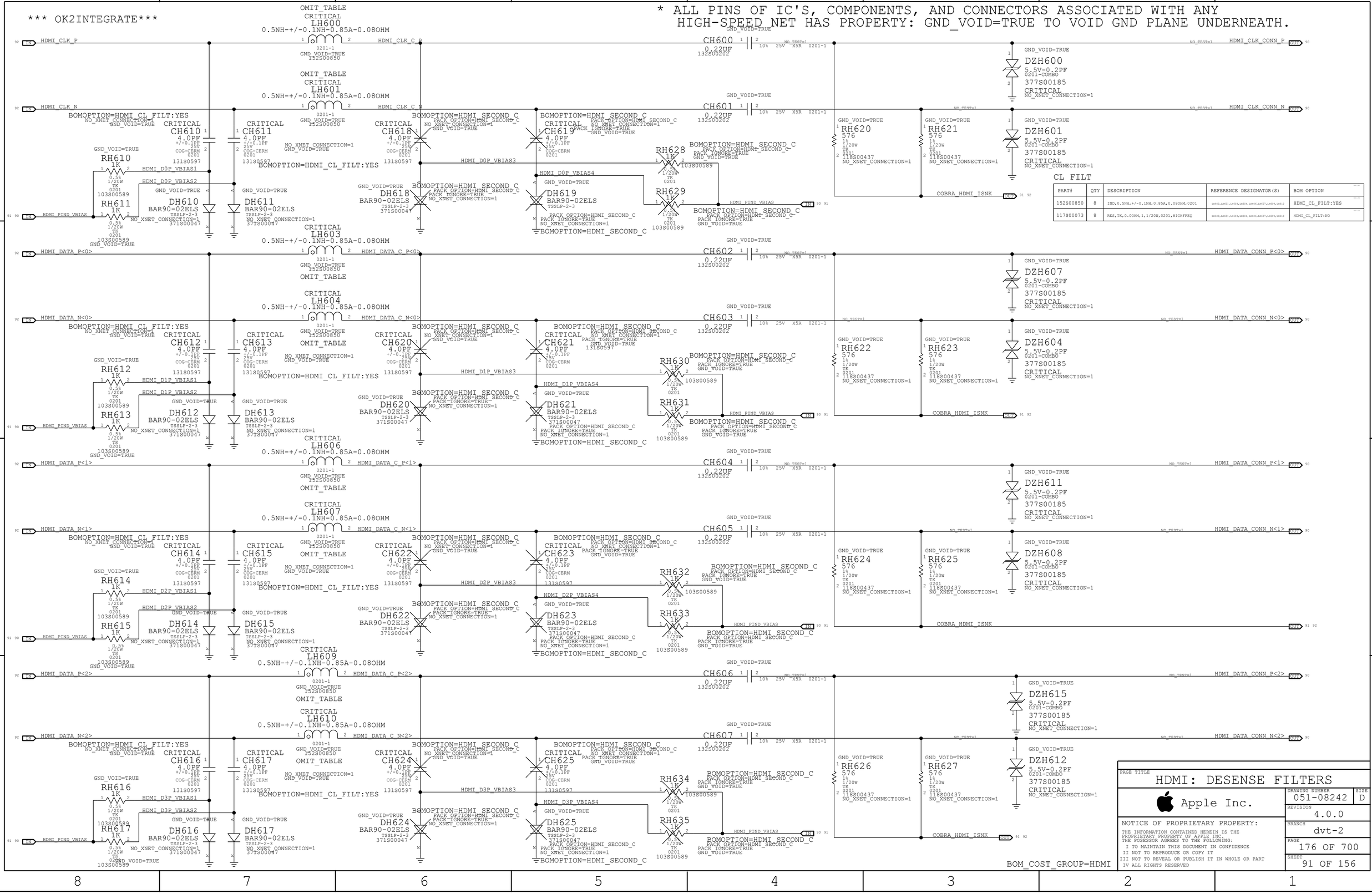

CL FILT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00850	8	IND,0.5NH,+/-0.1NH,0.85A,0.08OHM,0201	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CL_FILT:YES
117S00073	8	RES,TK,0.0OHM,1,1/20W,0201,HIGHFREQ	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CL_FILT:NO

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: DESENSE FILTERS

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*** IN PROGRESS ***

OMIT_TABLE

OMIT_TABLE

OMIT_TABLE

SW GPIO TPS PER <RDAR://74536924>,<RDAR://79172907>,<RDAR://77622534>

NOTE: PMU AND SAK MUST BE OD (VDD 1V8) FOR RESET TO HAVE 1V2 PU

VIEW YOUR SOC ARCHITECTURE FOR I2C HOOKUP

DESKTOPS WITH >1 COBRA:USE COBRAPART:1
PORTABLES: COBRAPART:0
TO DIFFERENTIATE WITH I2C ADDRESS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00772	1	IC,COBRA,PS190,DP2 TO HDMI,A0,BGA120	UH700	CRITICAL	COBRA-A0
338S00957	1	IC,COBRA,PS190,DP2 TO HDMI,A1,BGA120	UH700	CRITICAL	COBRA-A1_CGF2
998-29948	1	IC,COBRA,A1,DP TO HDMI CNVTR,DEV,BGA120	UH700	CRITICAL	COBRA-A1_CGF1

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: COBRA

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*** IN PROGRESS ***

LPDP AC Caps

From SOC → To HDMI

DP_DP2HDMI_DATA_N<0>	CH820 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<0>
DP_DP2HDMI_DATA_P<0>	CH821 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<0>
DP_DP2HDMI_DATA_N<1>	CH822 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<1>
DP_DP2HDMI_DATA_P<1>	CH823 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<1>
DP_DP2HDMI_DATA_N<2>	CH824 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<2>
DP_DP2HDMI_DATA_P<2>	CH825 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<2>
DP_DP2HDMI_DATA_N<3>	CH826 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<3>
DP_DP2HDMI_DATA_P<3>	CH827 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<3>
DP_DP2HDMI_AUX_N	CH828 0.1UF	10% 6.3V CERM-X5R 0201	DPRX_AUX_N
DP_DP2HDMI_AUX_P	CH829 0.1UF	10% 6.3V CERM-X5R 0201	DPRX_AUX_P

132S0444

DP2HDMI_RESET_L → RH801 0 0% 1/20W TF 0201 117S00073 → DP2HDMI_RESET_R_L

THIS SHORTS PMU TO SAK CONTROL

HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	UH701	CRITICAL	HDMI_ROM:512
341S02274	1	ROM,HDMI (V03.00.00) DVT,X2267	UH701	CRITICAL	HDMI_ROM:3_00

USE APN:341 ROM OPTIONS
APN:335 ARE BASE BLANK PARTS

THIS IS USED FOR CONTROLLING HDMI PORT POWER VIA THE PMU SYS ALIVE NET
THIS SAK IS USED FOR COBRA POWER SEQUENCING

***PLEASE REFER TO NOTE1 ON CSA2 FOR PROPER SIGNAL NAMING OF "PP1V8_HDMI_PWR_SEQ"

PP1V8_AON → CH806 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UH806 SLG4AP45256 STQFN 343S00528

PMU_SYS_ALIVE	2	SYS_ACTIVE	DISCHARGE_EN	4 P0V95_DSCHG_EN_RC
DP2HDMI_PWR_EN	3	HDMI_ENABLE	PP0V95V_EN	12 P0V95_HDMI_EN
NC_UH805_5	5	NC	PP1V2_EN	9 P1V2_HDMI_PWR_EN
NC_UH805_11	11	NC	PP3V3_EN	8 P3V3_HDMI_PWR_EN
			RESETB	10 DP2HDMI_RESET_R_L
			RESETB_2	6 NC_TP_HDMI_SAK_RESETB_2

VDD pin 1, GND pin 7

TPH704 TP-P40

LEVEL SHIFTERS

PP1V2_S2 → CH842 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

NO_XNET_CONNECTION=1 → RH822 30K 1% 1/20W TF 0201 118S00521

PP3V3_AWAKEFSW_DP2HDMI → CH841 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

311S00337 UH840 SN74AXC1T45-S SOT-5X3 (VCCA VCCB DIR GND)

SPI_DP2HDMI_HOLD_L → A → B → SPI_DP2HDMI_HOLD_L_3V3

PP3V3_S2 → CH802 0.1UF 10% 16V X5R-CERM 0201 132S0288

UH802 SN74LVC1G07 SON (VCC GND) 311S0536

HDMI_HPD_IN → HDMI_AOP_HPD_R → RH804 100 1% 1/20W TF 0201-1 118S00250 → HDMI_HPD_AOP

PP1V2_S2 → RH803 30K 1% 1/20W TF 0201 118S00521 NOSTUFF

PP1V2_S2 → CH801 0.1UF 10% 16V X5R-CERM 0201 132S0288

NO_XNET_CONNECTION=1 → RH815 30K 1% 1/20W TF 0201 118S00521

UH801 SN74AUP2G07 SON 311S00285 (VCC GND)

HDMI_CEC_AOP_TX → RH806 0 0% 1/20W TF 0201 117S00073 → AOP_HDMI_CEC_R

CEC_R → RH810 187 1% 1/20W TF 0201 118S00361 → HDMI_CEC

NO_XNET_CONNECTION=1 → RH816 27K 5% 1/20W TF 0201 117S00121

HDMI_AOP_CEC_R → RH805 100 1% 1/20W TF 0201-1 118S00250 → HDMI_CEC_AOP_RX

CONNECT THIS NET TO 5V_S2_MAIN

PLACE THIS NEAR 5V_S2_MAIN_VR_OUTPUT
PLACE_NEAR=CM917:10mm

XWH801 SM

PP5V_S2_HOLD → PP5V_S2_HDMI_LDO VOLTAGE=5

BOM_COST_GROUP=HDMI

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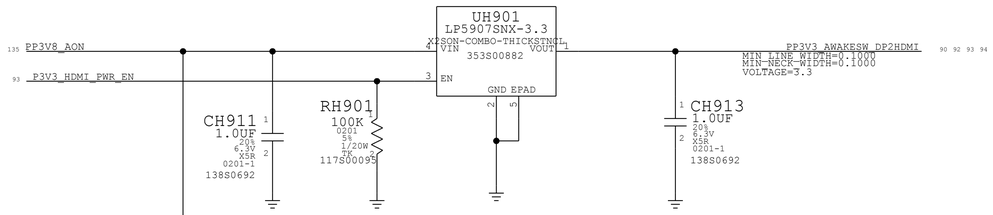
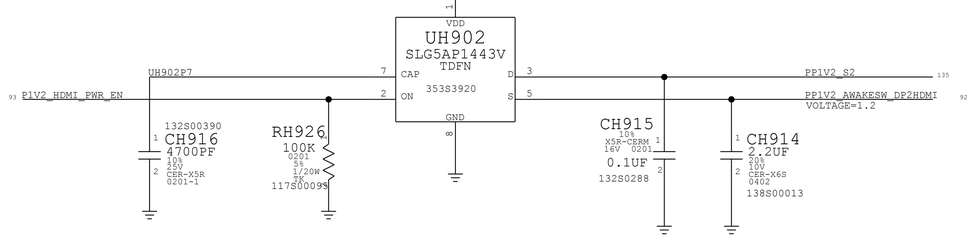
3.3V LDO



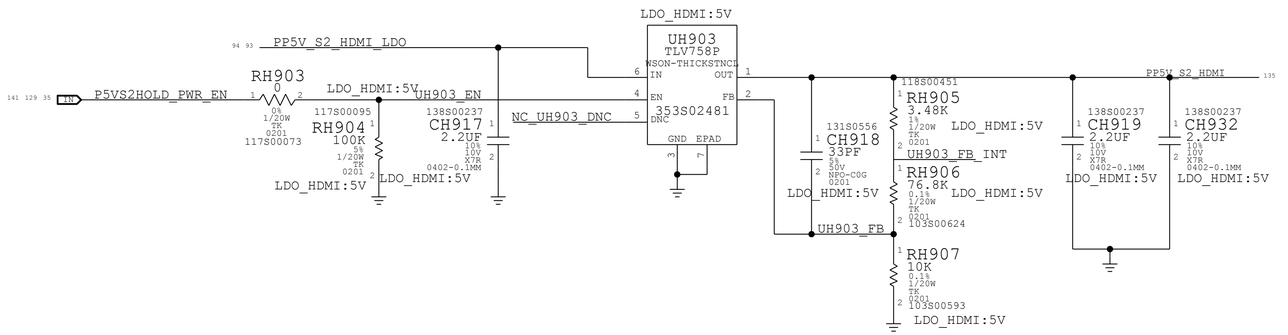
1.2V LOAD SW



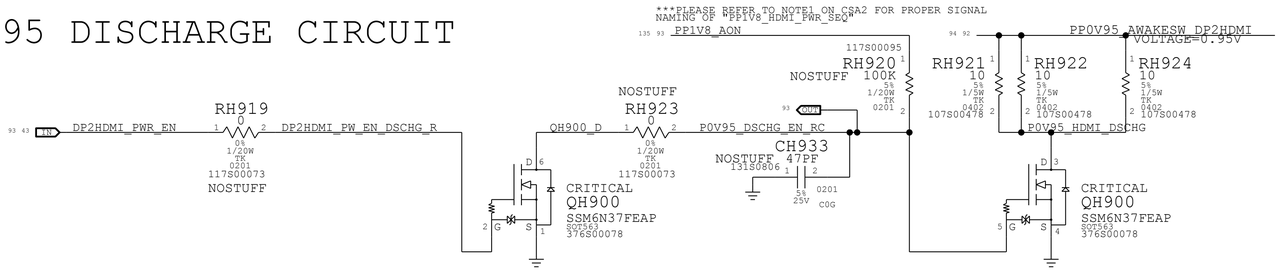
THIS IS USED FOR LONGER 5V POWER PATHS TO ENSURE GOOD 5V REGULATION

Enable BOMOPTION LDO_HDMI:NONE to disable the LDO use

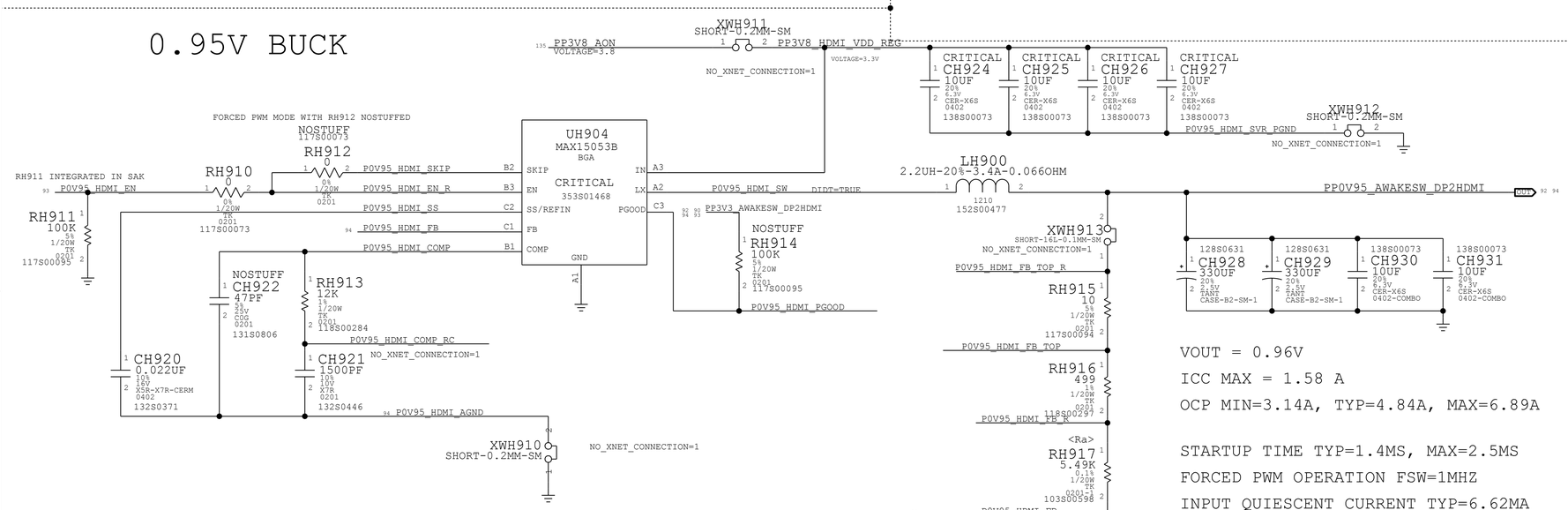
Enable BOMOPTION LDO_HDMI:5V to test HDMI 5V limit to 5.3V



0.95 DISCHARGE CIRCUIT



0.95V BUCK



VOUT = 0.96V

ICC MAX = 1.58 A

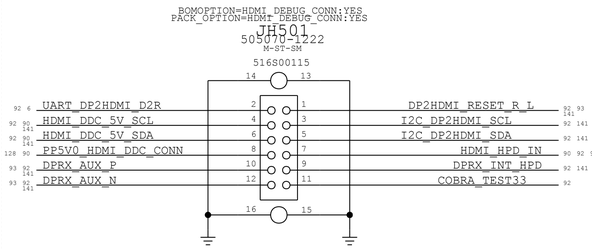
OCP MIN=3.14A, TYP=4.84A, MAX=6.89A

STARTUP TIME TYP=1.4MS, MAX=2.5MS

FORCED PWM OPERATION FSW=1MHZ

INPUT QUIESCENT CURRENT TYP=6.62MA

HDMI DEBUG CONNECTOR



PAGE TITLE

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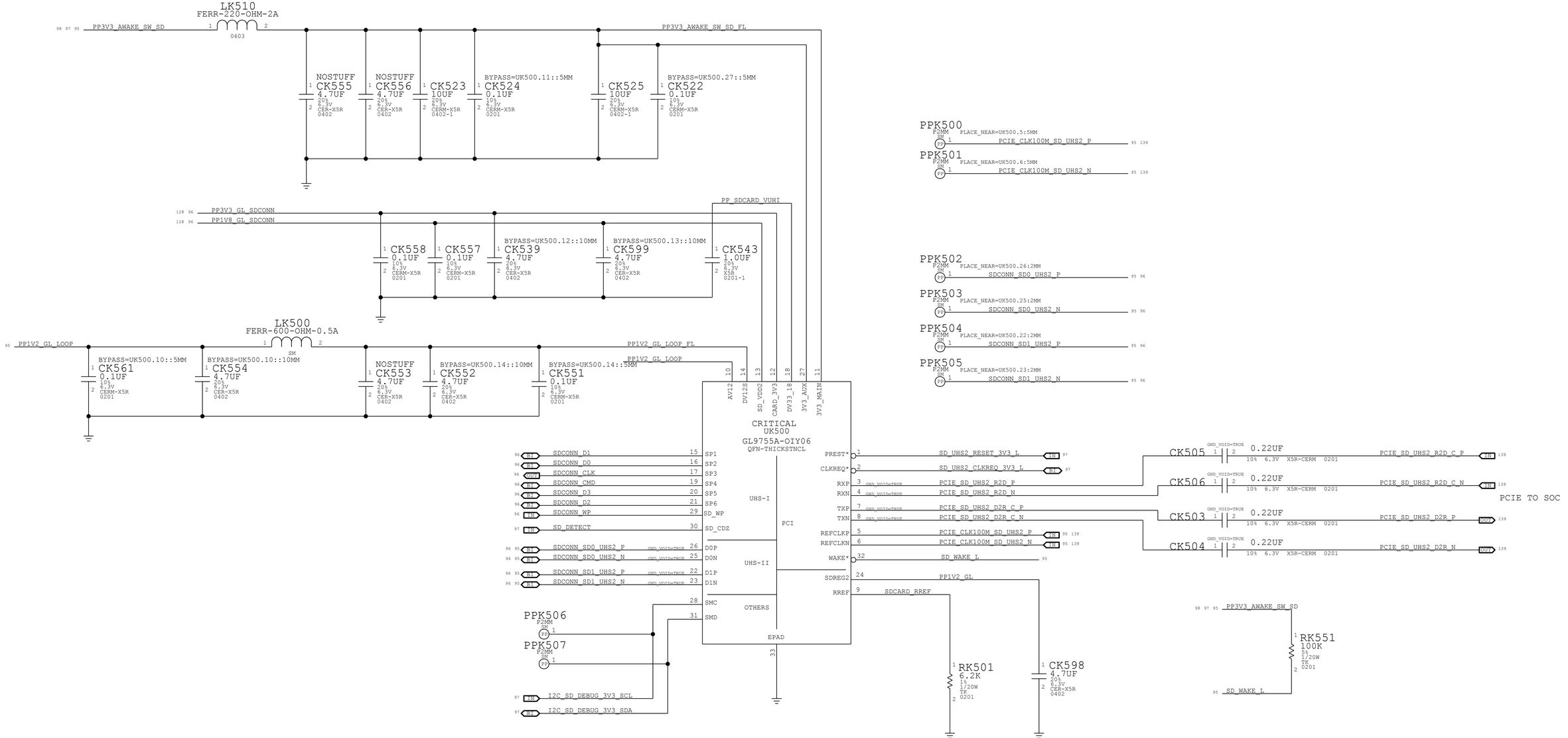

PAGE TITLE
SDCARD CONTROLLER

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
BRANCH dvt-2
PAGE 195 OF 700
SHEET 95 OF 156

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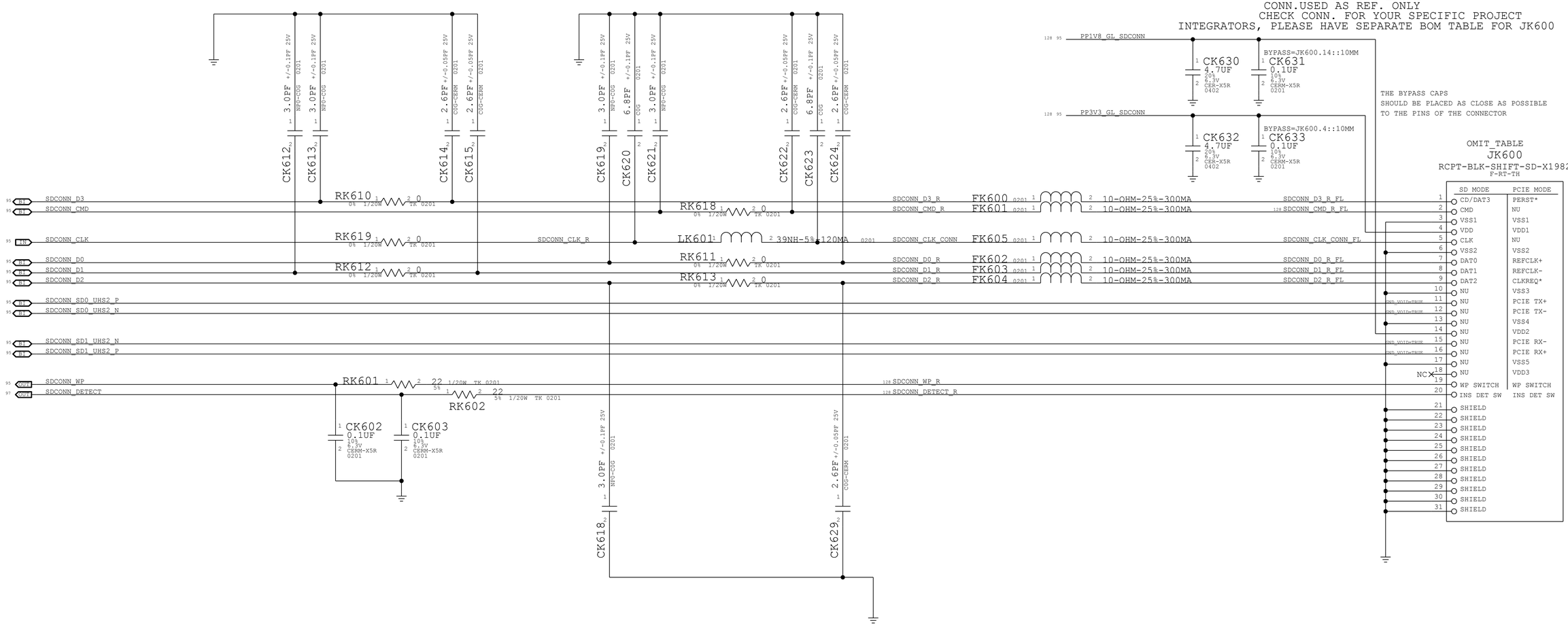
SD CARD CONNECTOR
514-00196

CONN.USED AS REF. ONLY
CHECK CONN. FOR YOUR SPECIFIC PROJECT
INTEGRATORS, PLEASE HAVE SEPARATE BOM TABLE FOR JK600



BOM_COST_GROUP=SDCARD

PAGE TITLE: SDCARD CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
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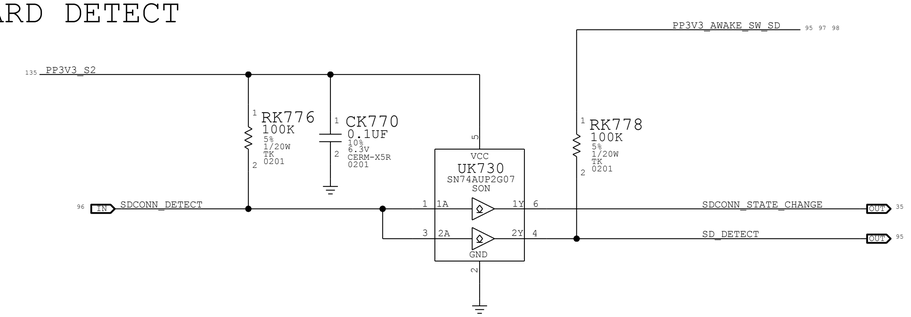
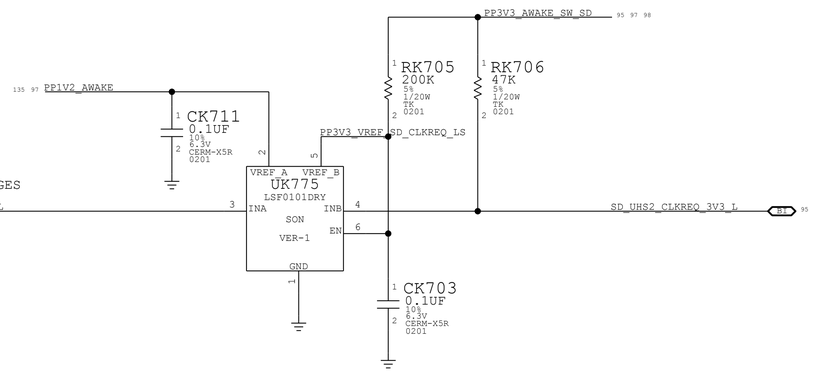
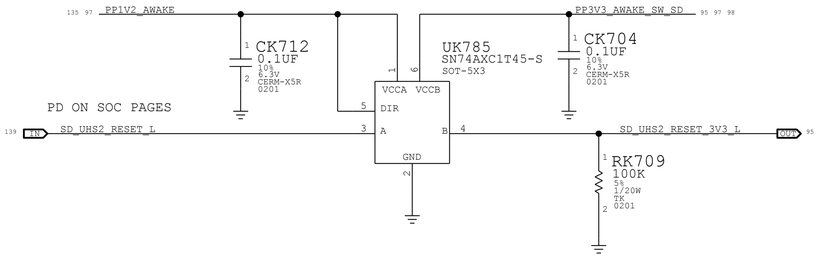
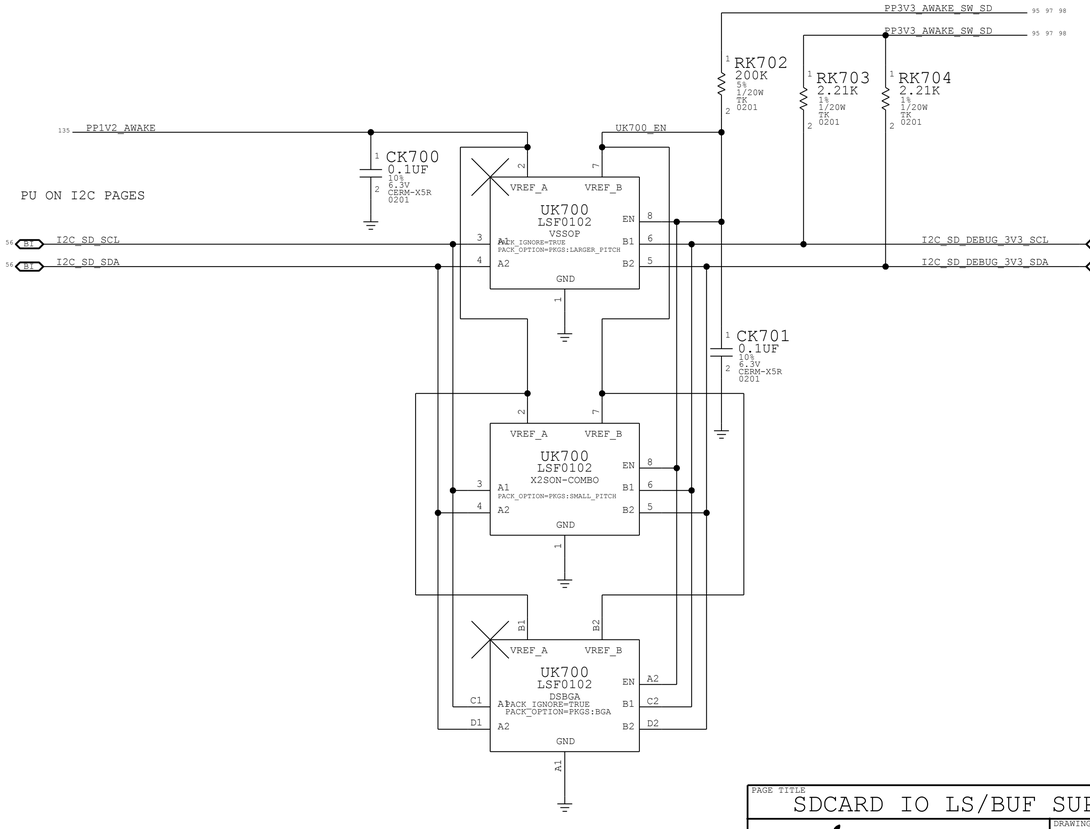
CARD DETECT



CONTROLLER IO







BOM_COST_GROUP=SDCARD

PAGE TITLE
SDCARD IO LS/BUF SUPPORT

Apple Inc.

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REVISION 4.0.0
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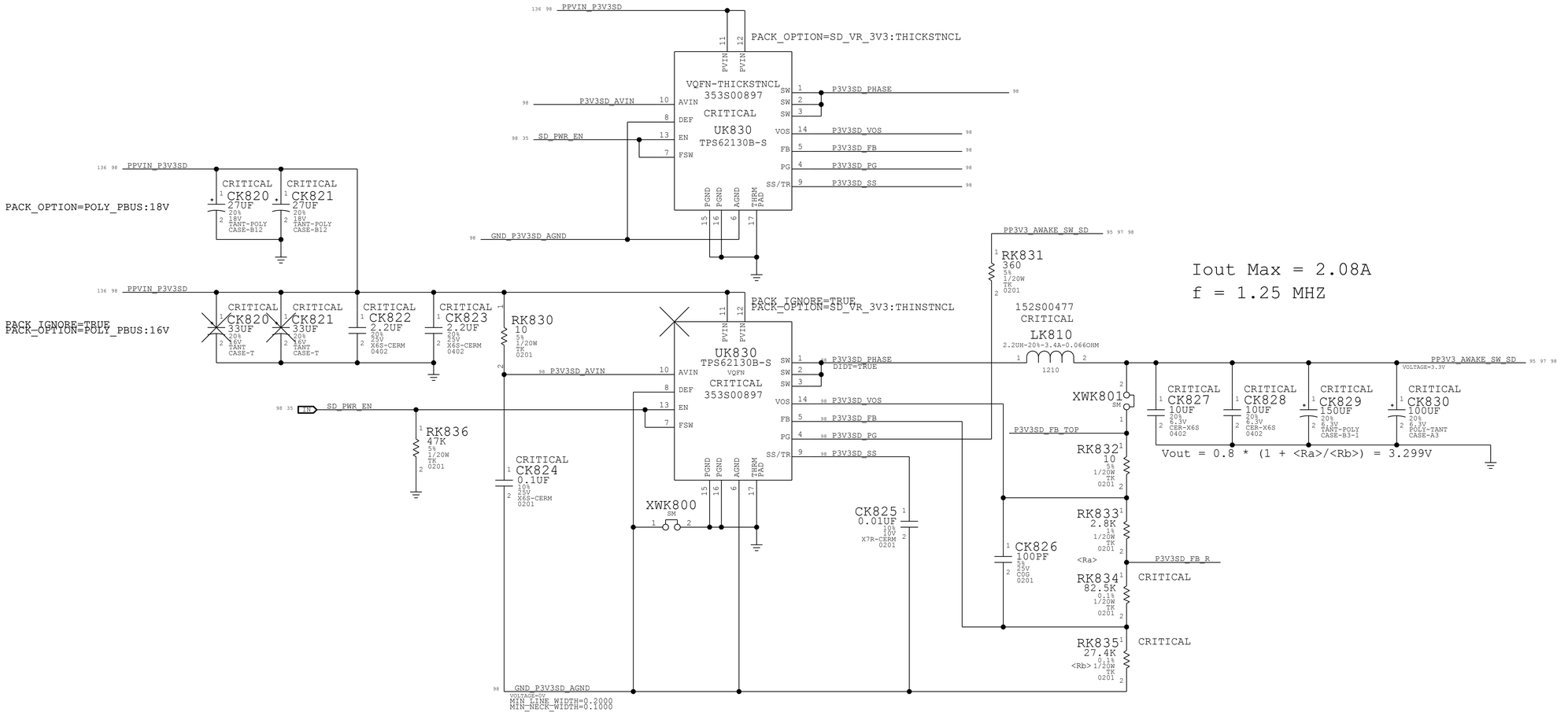

PAGE TITLE: SDCARD POWER SUPPORT

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*** OK2INTEGRATE ***

FOR SYSTEM INTEGRATION INFORMATION OF WILLAMETTE REFER TO
RDAR://PROBLEM/72432057

WILLAMETTE WIFI/BT MODULE

PLACE_NEAR=UL000.48:5MM
PLACE_NEAR=UL000.48:5MM
PLACE_NEAR=UL000.48:5MM
PP3V8_AON_WLBT 99 133 136
CL005 10UF 20% 10V X5R-CERM 0402-8
CL030 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL020 12PF 5% 25V NP0-C0G 0201
VBAT

PLACE_NEAR=UL000.37:5MM
PLACE_NEAR=UL000.37:5MM
PLACE_NEAR=UL000.37:5MM
PP3V8_AON_WLBT 99 133 136
CL006 10UF 20% 10V X5R-CERM 0402-8
CL031 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL021 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.79:5MM
PLACE_NEAR=UL000.79:5MM
PLACE_NEAR=UL000.79:5MM
PP3V8_AON_WLBT 99 133 136
CL007 10UF 20% 10V X5R-CERM 0402-8
CL032 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL022 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.12:5MM
PLACE_NEAR=UL000.12:5MM
PLACE_NEAR=UL000.12:5MM
PP3V8_AON_WLBT 99 133 136
CL008 10UF 20% 10V X5R-CERM 0402-8
CL033 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL023 12PF 5% 25V NP0-C0G 0201
5GFEM

PLACE_NEAR=UL000.31:5MM
PLACE_NEAR=UL000.31:5MM
PLACE_NEAR=UL000.31:5MM
PP1V8_S2 99 133 135
CL010 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL
CL024 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.86:5MM
PLACE_NEAR=UL000.86:5MM
PLACE_NEAR=UL000.86:5MM
PP1V8_S2 99 133 135
CL011 10UF 20% 10V X5R-CERM 0402-8
CRITICAL
CL025 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.22:5MM
PLACE_NEAR=UL000.22:5MM
PLACE_NEAR=UL000.22:5MM
PP1V8_S2 99 133 135
CL012 0.1UF 10% 6.3V CERM-X5R 0201
CL034 3PF +/-0.1PF 25V C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.4:5MM
PLACE_NEAR=UL000.4:5MM
PLACE_NEAR=UL000.4:5MM
PP1V8_S2 99 133 135
CL013 0.1UF 10% 6.3V CERM-X5R 0201
CL035 3PF +/-0.1PF 25V C0G 0201
5GFEM_C1

PP1V8_S2 135 133 99
PP3V8_AON_WLBT 136 133 99
PP1V2_S2 102
PLACE_NEAR=UL000.52:4MM
CL014 0.1UF 10% 6.3V CERM-X5R 0201

UL000
2103-602102-10
LGA
SYM 1 OF 4

11	VDD_5G_CGC1			
12	VDD_5G_CGC1			
13	VDD_5G_CGC1			
14	VDD_5G_CGC1			
37	VDD_2G_C0			
38	VDD_2G_C0			
79	VDD_2G_C1			
80	VDD_2G_C1			
69	VDD_BT			
48	VBAT			
49	VBAT			
50	VBAT			
133	VBAT			
134	VBAT			
135	VBAT			
31	VDD1V8_2G_C0			
86	VDD1V8_2G_C1			
22	VDD1V8_5G_C0			
4	VDD1V8_5G_C1			
66	VDD1V8_BB			
67	VDDIO_RF			
52	VDDIO1P8			
	VDDIO1P2			

100 99 6	OUT	RF_ANT_0	NO_TEST=1	28 ANT_0
100 99 6	OUT	RF_ANT_1	NO_TEST=1	89 ANT_1
100 99 6	OUT	RF_BT_DED	NO_TEST=1	73 BT_DEDICATED
		NC_BT_GPIO_2	NO_TEST=1	413 BT_GPIO_2
100 99 6	OUT	BT_TIME_SYNC		435 BT_GPIO_3
99	OUT	BT_I2C_DATA		129 BT_GPIO_4
99	OUT	BT_I2C_CLK		41 BT_GPIO_5
99 12	IN	SPMI_WLBT_CLK		126 SPMI_HEB_CLK
99 12	BI	SPMI_WLBT_DATA		391 SPMI_HEB_DAT
99		BT_LHL_GPIO2		523 LHL_GPIO2
		NC_SPMI_IDC_CLK		40 SPMI_IDC_CLK
		NC_SPMI_IDC_DATA		127 SPMI_IDC_DAT
100 99 43 35	IN	WLBT_PWR_EN		130 WLBT_REG_ON
100 99 35	IN	PMU_CLK32K_WLBT		479 WLBT_CLK_32K
99		WLAN_JTAG_SEL		540 JTAG_SEL
				131 PACKAGEOPTION_2

RL002 10K 5% 1/20W TK 0201

OMIT_TABLE

WL_GPIO_0		WLBT_WAKE		542 OUT 43 99 100
WL_GPIO_1		WLAN_TIME_SYNC		528 OUT 6 99 100
WL_GPIO_2		TP_WLAN_JTAG_TCK		526 99 100
WL_GPIO_3		TP_WLAN_JTAG_TMS		525 99 100
WL_GPIO_4		TP_WLAN_JTAG_TDI		75 99
WL_GPIO_5		TP_WLAN_JTAG_TDO		76 99
WL_GPIO_6		TP_WLAN_JTAG_TRSTN		158 99
WL_GPIO_7		WL_GPIO_7		538 99
WL_GPIO_8		NC_WL_GPIO_8	NO_TEST=1	153
WL_GPIO_9		NC_WL_GPIO_9	NO_TEST=1	527
WL_GPIO_10		NC_WL_GPIO_10	NO_TEST=1	159
WL_GPIO_11		NC_WL_GPIO_11	NO_TEST=1	140
WL_GPIO_12		NC_WL_GPIO_12	NO_TEST=1	138
WL_GPIO_13		NC_WL_GPIO_13	NO_TEST=1	42
WL_GPIO_14		NC_WL_GPIO_14	NO_TEST=1	539
WL_GPIO_15		NC_WL_GPIO_15	NO_TEST=1	139
WL_GPIO_16		NC_WL_GPIO_16	NO_TEST=1	541
WL_GPIO_18		NC_WL_GPIO_18	NO_TEST=1	44
WL_GPIO_19		NC_WL_GPIO_19	NO_TEST=1	43
WLBT_PCIE_PERST_L		WLBT_RESET_L		534 IN 8 99 100
WLBT_PCIE_CLKREQ_L		WLBT_CLKREQ_R_L		531 99
WLBT_PCIE_RXD_P		PCIE_WLBT_R2D_P		143 99 129
WLBT_PCIE_RXD_N		PCIE_WLBT_R2D_N		142 99 129
WLBT_PCIE_TXD_P		PCIE_WLBT_D2R_C_P		146 99 129
WLBT_PCIE_TXD_N		PCIE_WLBT_D2R_C_N		145 99 129
WLBT_PCIE_REFCLK_P		PCIE_CLK100M_WLBT_P		148 IN 8 99
WLBT_PCIE_REFCLK_N		PCIE_CLK100M_WLBT_N		149 IN 8 99

GND_VOID=TRUE
PLACE_NEAR=UL000.143:4MM
CL001 0.1UF 6.3V 10% 2 CERM-X5R 0201
8 IN PCIE_WLBT_R2D_C_P — PCIE_WLBT_R2D_P 99 129
8 IN PCIE_WLBT_R2D_C_N — PCIE_WLBT_R2D_N 99 129
CL002 0.1UF 6.3V 10% 2 CERM-X5R 0201
GND_VOID=TRUE
PLACE_NEAR=UL000.142:4MM

GND_VOID=TRUE
PLACE_NEAR=UL000.146:4MM
CL003 0.1UF 6.3V 10% 2 CERM-X5R 0201
99 129 PCIE_WLBT_D2R_C_P — PCIE_WLBT_D2R_P OUT 8 99
99 129 PCIE_WLBT_D2R_C_N — PCIE_WLBT_D2R_N OUT 8 99
CL004 0.1UF 6.3V 10% 2 CERM-X5R 0201
GND_VOID=TRUE
PLACE_NEAR=UL000.145:4MM

99 12 SPMI_WLBT_CLK — RL003 200K 1/20W 5% 0201 TK
99 12 SPMI_WLBT_DATA — RL004 200K 1/20W 5% 0201 TK

99 WLBT_CLKREQ_R_L — RL001 1K 1/20W 5% 0201-1 TK — WLBT_CLKREQ_L BI 8 99 100

BOM_COST_GROUP=WIRELESS

TPL001 A — PMU_CLK32K_WLBT 35 99 100
TPL002 A — WLBT_PWR_EN 35 43 99 100
TPL003 A — WLBT_WAKE 43 99 100
TPL004 A — TP_WLAN_JTAG_TCK 99 100
TPL005 A — TP_WLAN_JTAG_TMS 99 100
TPL006 A — TP_WLAN_JTAG_TDI 99
TPL007 A — TP_WLAN_JTAG_TDO 99
TPL008 A — TP_WLAN_JTAG_TRSTN 99
TPL009 A — WLAN_JTAG_SEL 99
TPL010 A — BT_TIME_SYNC 6 99 100
TPL011 A — WLAN_TIME_SYNC 6 99 100
TPL012 A — BT_I2C_DATA 99
TPL013 A — BT_I2C_CLK 99
TPL018 A — SPMI_WLBT_CLK 12 99
TPL019 A — SPMI_WLBT_DATA 12 99
TPL020 A — BT_LHL_GPIO2 99
TPL023 A — WLBT_RESET_L 8 99 100
TPL024 A — WLBT_CLKREQ_L 8 99 100
TPL025 A — WL_GPIO_7 99

All TPL: TP-P40 PACK_IGNORE=TRUE PACK_OPTION=WLBT_TP_0P5 PACK_OPTION=WLBT_TP_0P4

PPL021 P2MM SM PB 1 — PCIE_CLK100M_WLBT_P 8 99
PPL022 P2MM SM PB 1 — PCIE_CLK100M_WLBT_N 8 99
PPL026 P2MM SM PB 1 — PCIE_WLBT_D2R_P 8 99
PPL027 P2MM SM PB 1 — PCIE_WLBT_D2R_N 8 99
PACK_IGNORE=TRUE PACK_OPTION=WLBT_PP_D2R

WILLAMETTE BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S01093	1	MODULE,WLAN/BT,WILLAMETTE, ES4.7	UL000	CRITICAL	

WLMT ALT BOM TABLE:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S01206	339S01093	ANY	UL000	AMKOR

PAGE TITLE: WIFI/BT: MODULE

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DRAWING NUMBER 051-08242 SIZE D
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WILLAMETTE WIFI/BT MODULE GND

UL000
2103-602102-10
LGA
SYM 2 OF 4

1	GND	GND	110		
2	GND	GND	111		
3	GND	GND	112		
5	GND	GND	113		
6	GND	GND	114		
7	GND	GND	115		
8	GND	GND	116		
9	GND	GND	117		
10	GND	GND	118		
15	GND	GND	119		
16	GND	GND	120		
17	GND	GND	121		
18	GND	GND	122		
19	GND	GND	123		
20	GND	GND	124		
21	GND	GND	125		
23	GND	GND	128		
24	GND	GND	132		
25	GND	GND	136		
26	GND	GND	137		
27	GND	GND	141		
29	GND	GND	144		
30	GND	GND	147		
32	GND	GND	150		
33	GND	GND	151		
34	GND	GND	152		
35	GND	GND	154		
36	GND	GND	155		
39	GND	GND	156		
45	GND	GND	157		
46	GND	GND	160		
47	GND	GND	161		
51	GND	GND	162		
53	GND	GND	163		
54	GND	GND	164		
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106	GND	GND	206		
107	GND	GND	207		
108	GND	GND	208		
109	GND	GND	209		

UL000
2103-602102-10
LGA
SYM 3 OF 4

210	GND	GND	290
211	GND	GND	291
212	GND	GND	292
213	GND	GND	293
214	GND	GND	294
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216	GND	GND	296
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283	GND	GND	363
284	GND	GND	364
285	GND	GND	365
286	GND	GND	366
287	GND	GND	367
288	GND	GND	368
289	GND	GND	369

UL000
2103-602102-10
LGA
SYM 4 OF 4

370	GND	GND	453
371	GND	GND	454
372	GND	GND	455
373	GND	GND	456
374	GND	GND	457
375	GND	GND	458
376	GND	GND	459
377	GND	GND	460
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380	GND	GND	463
381	GND	GND	464
382	GND	GND	465
383	GND	GND	466
384	GND	GND	467
385	GND	GND	468
386	GND	GND	469
387	GND	GND	470
388	GND	GND	471
389	GND	GND	472
390	GND	GND	473
392	GND	GND	474
393	GND	GND	475
394	GND	GND	476
395	GND	GND	477
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412	GND	GND	495
414	GND	GND	496
415	GND	GND	497
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417	GND	GND	499
418	GND	GND	500
419	GND	GND	501
420	GND	GND	502
421	GND	GND	503
422	GND	GND	504
423	GND	GND	505
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438	GND	GND	519
439	GND	GND	520
440	GND	GND	521
441	GND	GND	522
442	GND	GND	524
443	GND	GND	529
444	GND	GND	530
445	GND	GND	532
446	GND	GND	533
447	GND	GND	535
448	GND	GND	536
449	GND	GND	537
450	GND	GND	543
451	GND	GND	544
452	GND	GND	545

ANTENNA CONNECTORS

2G_C0
5G_C0
BT_C0

JL120
IR050D15010C
F-ST-SM
1 RF_ANT_0 NO_TEST=1 BT 99 100
SUNWAY_1P5MM
PACK_OPTION=SUNWAY
BOMOPTION=RF_CONN

JL140
20449-001E-03
F-ST-SM
1 RF_ANT_0 99 100
SUNWAY_1P5MM
PACK_IGNORE=TRUE
PACK_OPTION=IPEX_1P5
BOMOPTION=RF_CONN

JL130
20431-001E-01
F-ST-SM
2 SIGNAL RF_ANT_0 99 100
GND
IPEX 2MM
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN

RF CONNECTOR ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0867	518S00033	RFCONN_ALT	ALL	IPEX

2G_C1
5G_C1
BT_C1

JL121
IR050D15010C
F-ST-SM
1 RF_ANT_1 NO_TEST=1 BT 99 100
SUNWAY_1P5MM
PACK_OPTION=SUNWAY
BOMOPTION=RF_CONN

JL141
20449-001E-03
F-ST-SM
1 RF_ANT_1 99 100
SUNWAY_1P5MM
PACK_IGNORE=TRUE
PACK_OPTION=IPEX_1P5
BOMOPTION=RF_CONN

JL131
20431-001E-01
F-ST-SM
2 SIGNAL RF_ANT_1 99 100
GND
IPEX 2MM
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN

BT_C1_DED

JL122
IR050D15010C
F-ST-SM
1 100 RF_BT_DED_ANT NO_TEST=1
SUNWAY_1P5MM
PACK_OPTION=3X_ANTENNA
BOMOPTION=RF_CONN

JL142
20449-001E-03
F-ST-SM
1
SUNWAY_1P5MM
PACK_IGNORE=TRUE
PACK_OPTION=IPEX_1P5_3X
BOMOPTION=RF_CONN

UL101
2GHZ
LFL182G44UA1F627
1 IN OUT 3 RF_BT_DED NO_TEST=1 BT 99 100
2 GND
PACK_OPTION=3X_ANTENNA
BOMOPTION=RF_CONN
ALLOW_APPLE_PREFIX=U

JL132
20431-001E-01
F-ST-SM
2 SIGNAL 100 RF_BT_DED_ANT
GND
IPEX 2MM
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN

UL111
2GHZ
LFL182G44UA1F627
1 IN OUT 3 RF_BT_DED 99 100
2 GND
PACK_IGNORE=TRUE
PACK_IGNORE=TRUE
PACK_OPTION=3X_ANTENNA_IPEX
BOMOPTION=RF_CONN
ALLOW_APPLE_PREFIX=U

WLBT DEBUG CONNECTOR

JL103
505070-1222
M-ST-SM

99 6	WLAN_TIME_SYNC	2	1	TP_WLAN_JTAG_TCK	99 SWD_CLK
NC		4	3	TP_WLAN_JTAG_TMS	99 SWD_DIO
NC		6	5		NC
99 43	WLBT_WAKE	8	7	WLBT_CLKREQ_L	8 99
99 43 35	WLBT_PWR_EN	10	9	BT_TIME_SYNC	6 99
99 8	WLBT_RESET_L	12	11	PMU_CLK32K_WLBT	35 99

14 13 16 15

4388 SWD:

BOMOPTION=WLBT_DBG
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_DBG_CONN

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

Apple Inc.

DRAWING NUMBER 051-08242
SIZE D
REVISION 4.0.0
BRANCH dvt-2
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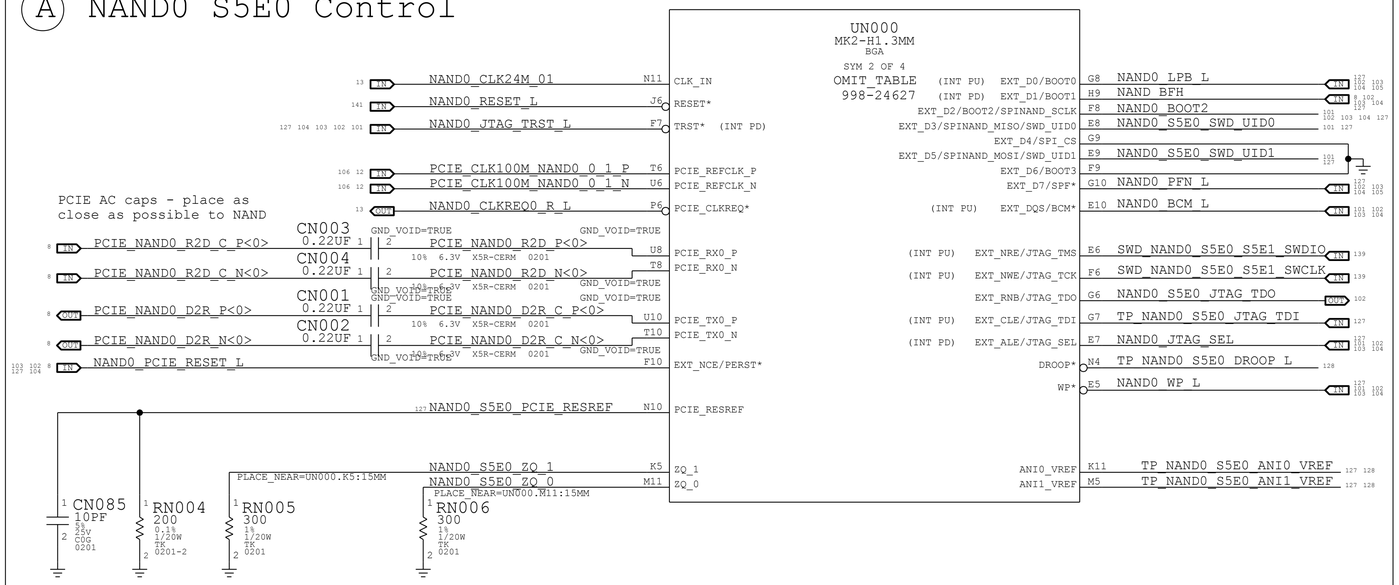
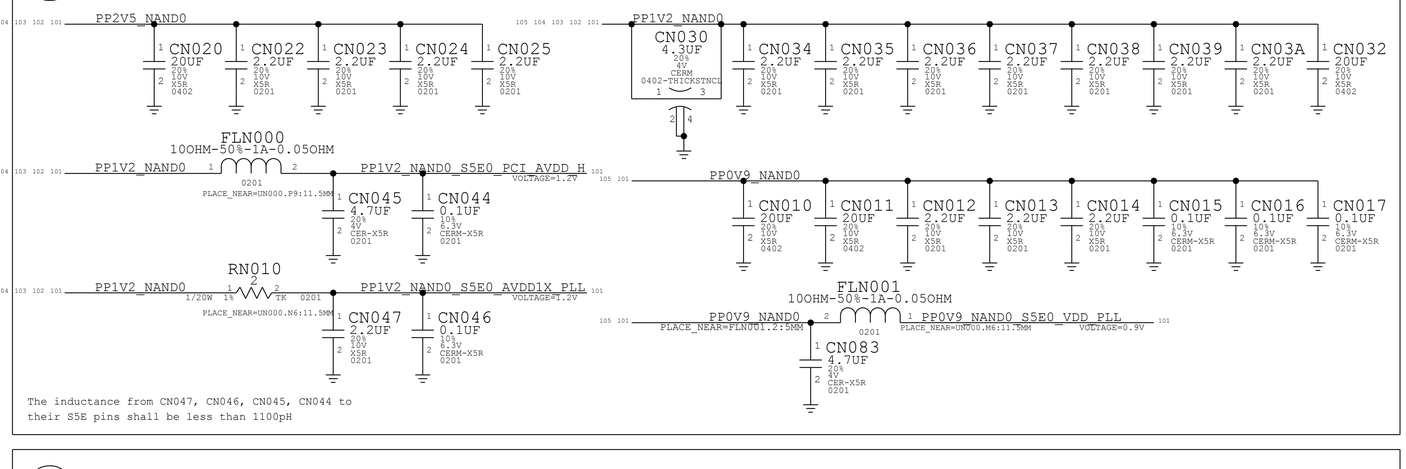
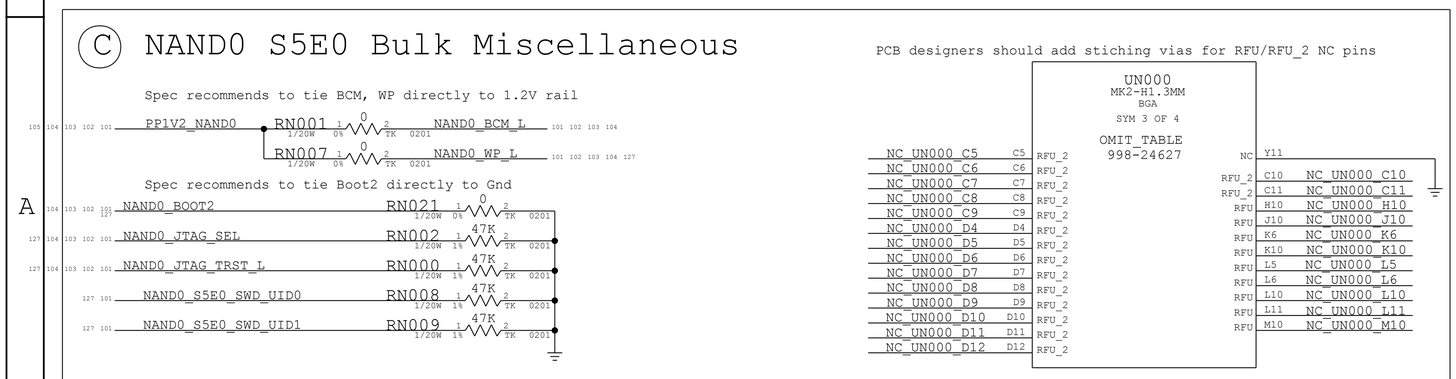
A NAND0 S5E0 Control



B NAND0 S5E0 Bulk Capacitance

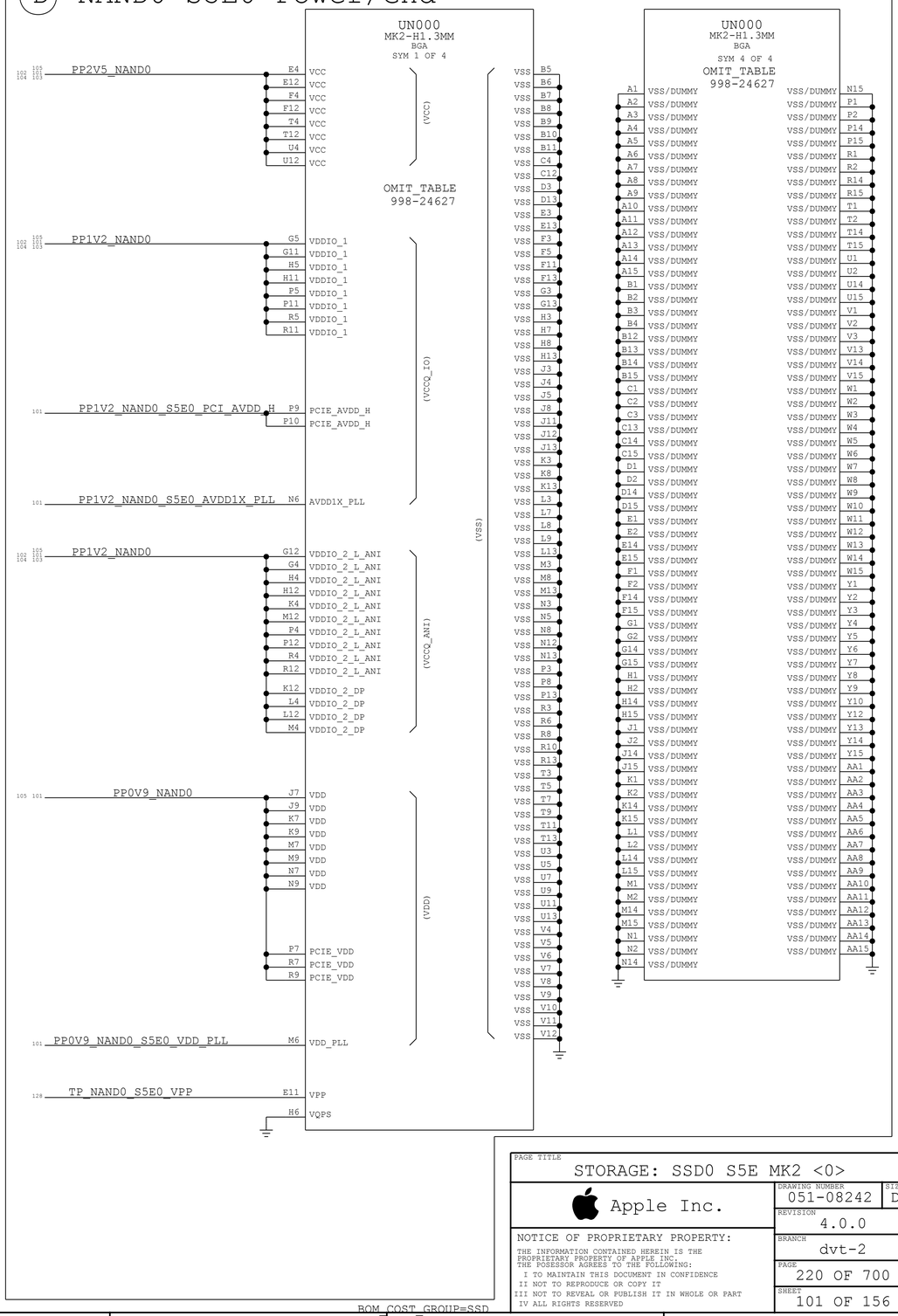


C NAND0 S5E0 Bulk Miscellaneous



PCB designers should add stiching vias for RFU/RFU_2 NC pins

D NAND0 S5E0 Power/Gnd



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 S5E MK2 <0>

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
REVISION 4.0.0
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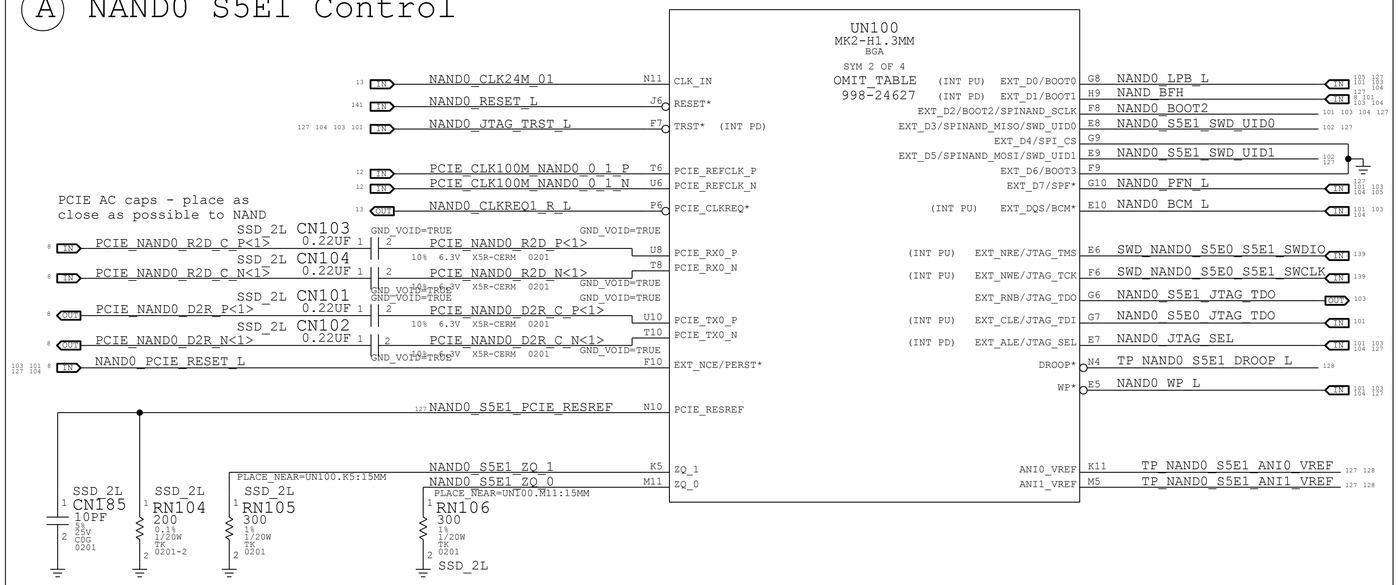
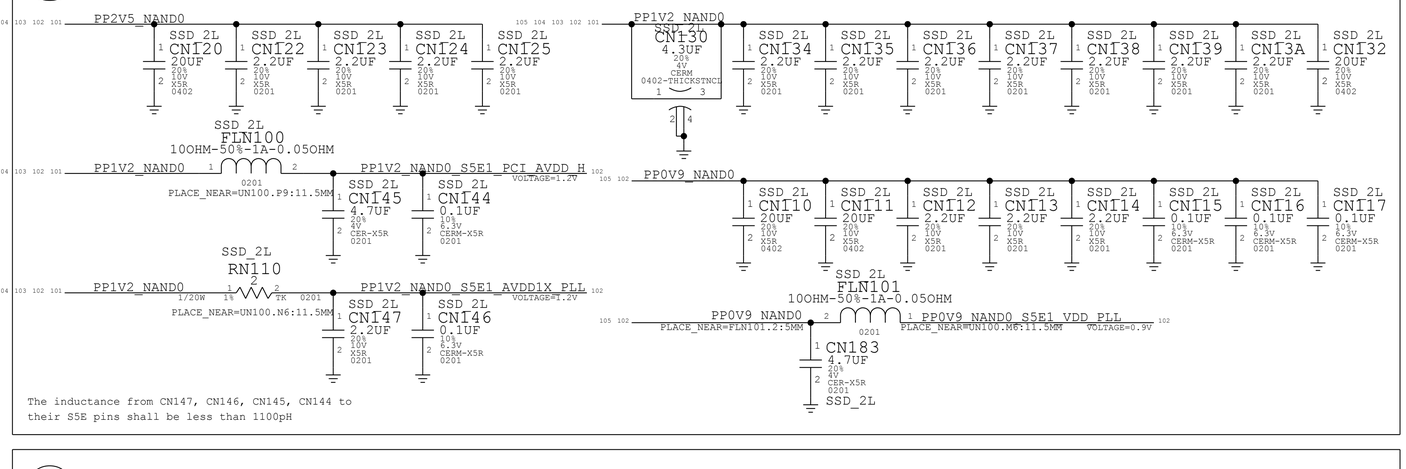
A NAND0 S5E1 Control

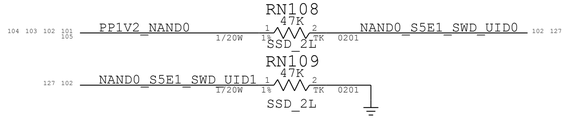


B NAND0 S5E1 Bulk Capacitance

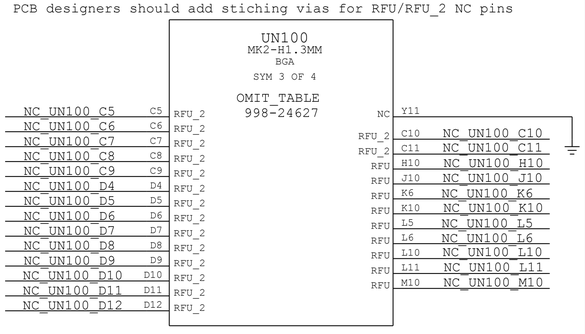


The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

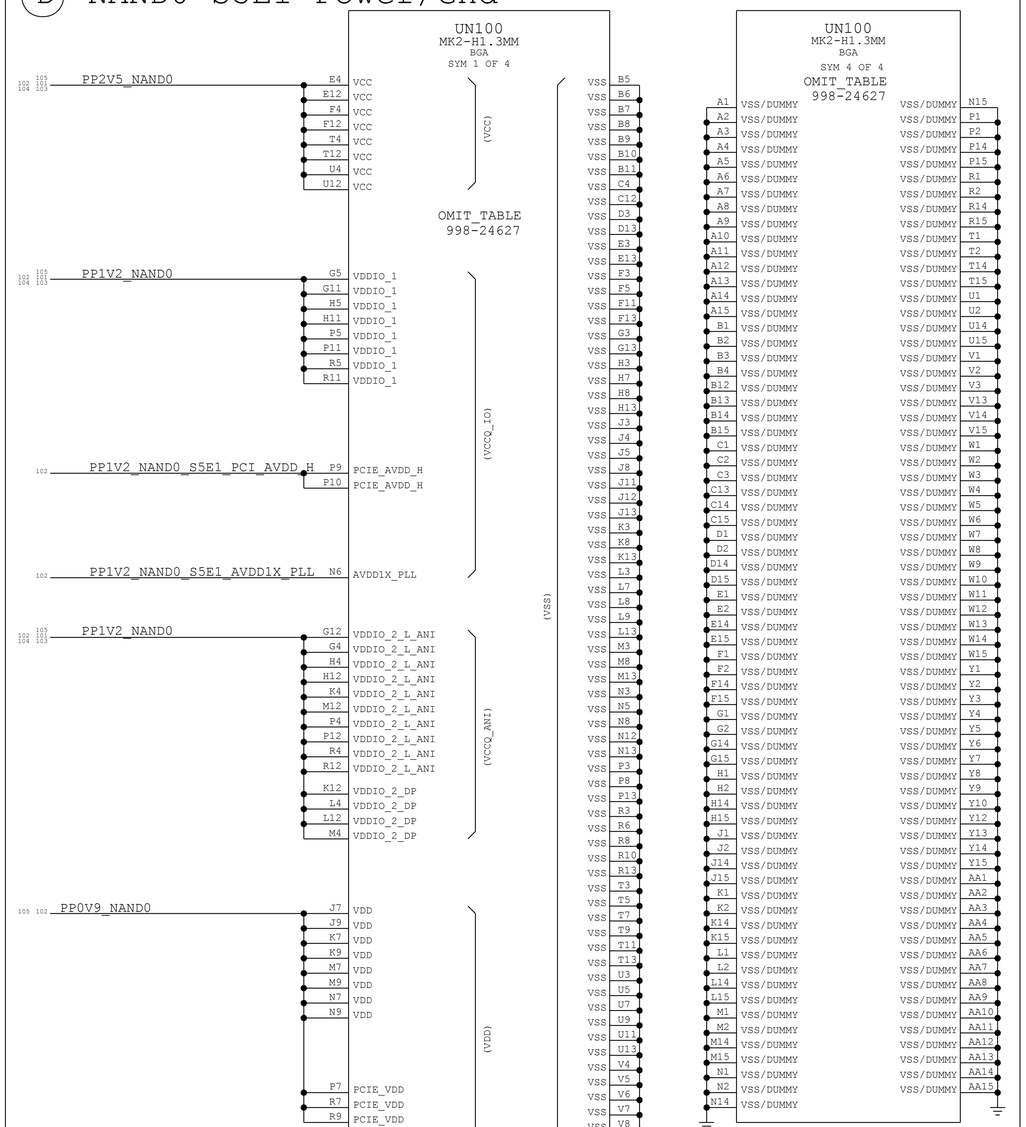
C NAND0 S5E1 Bulk Miscellaneous



PCB designers should add stiching vias for RFU/RFU_2 NC pins



D NAND0 S5E1 Power/Gnd



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 S5E MK2 <1>

Apple Inc.

DRAWING NUMBER 051-08242 SIZE D
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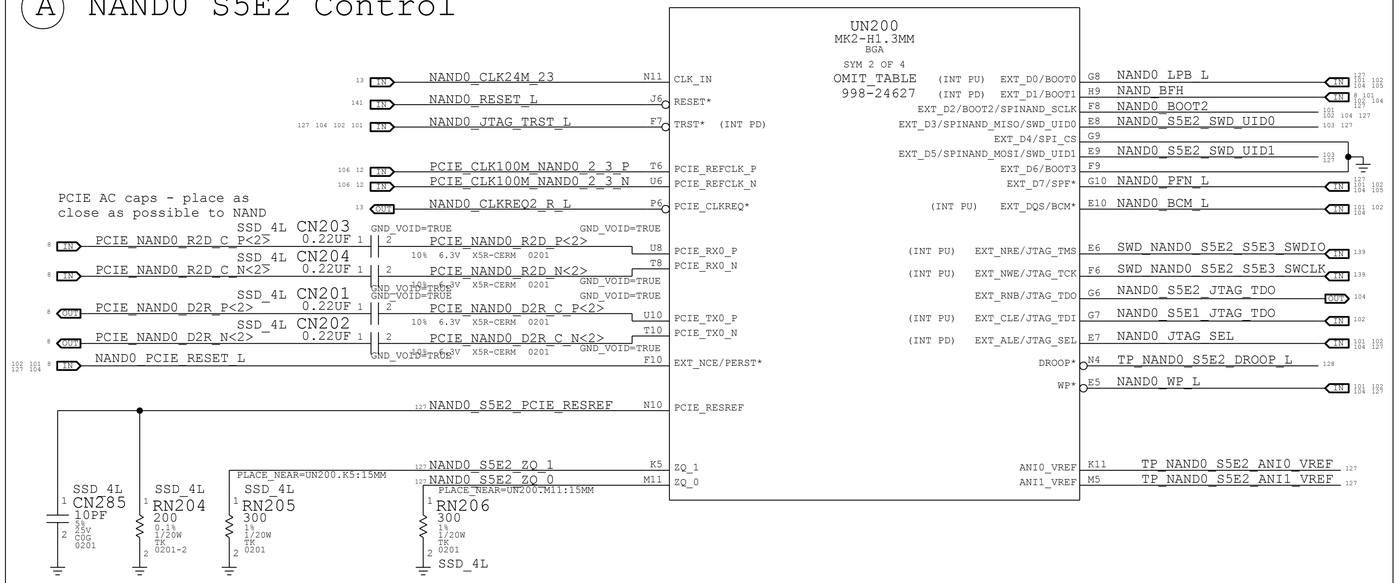
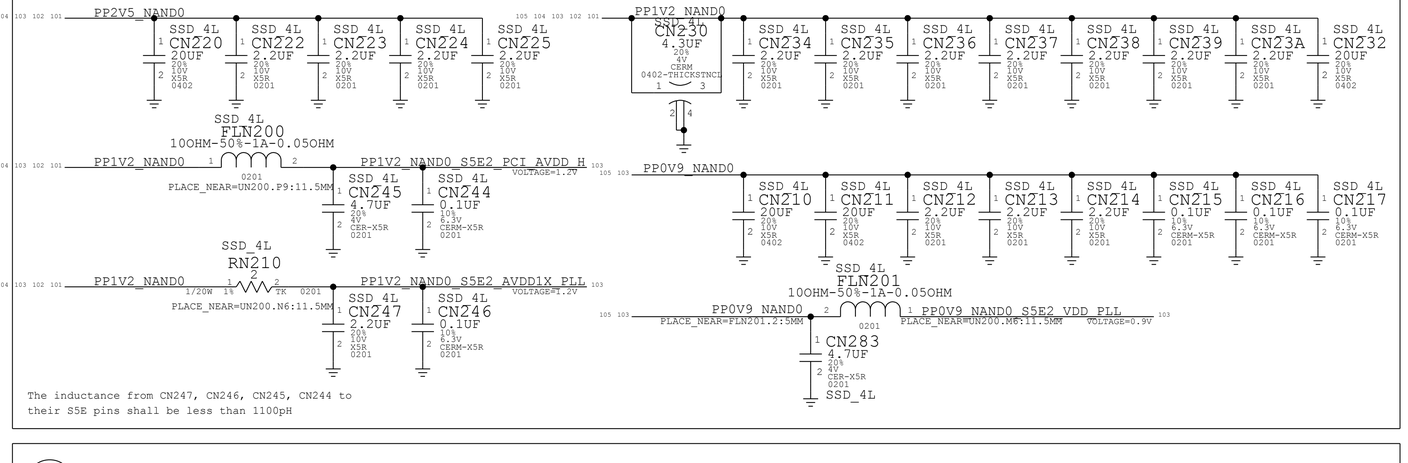
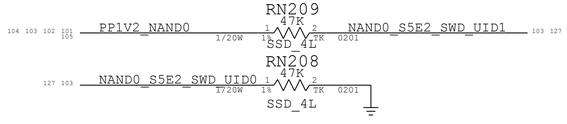
A NAND0 S5E2 Control



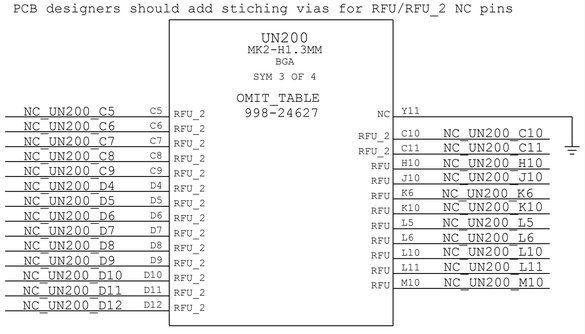
B NAND0 S5E2 Bulk Capacitance



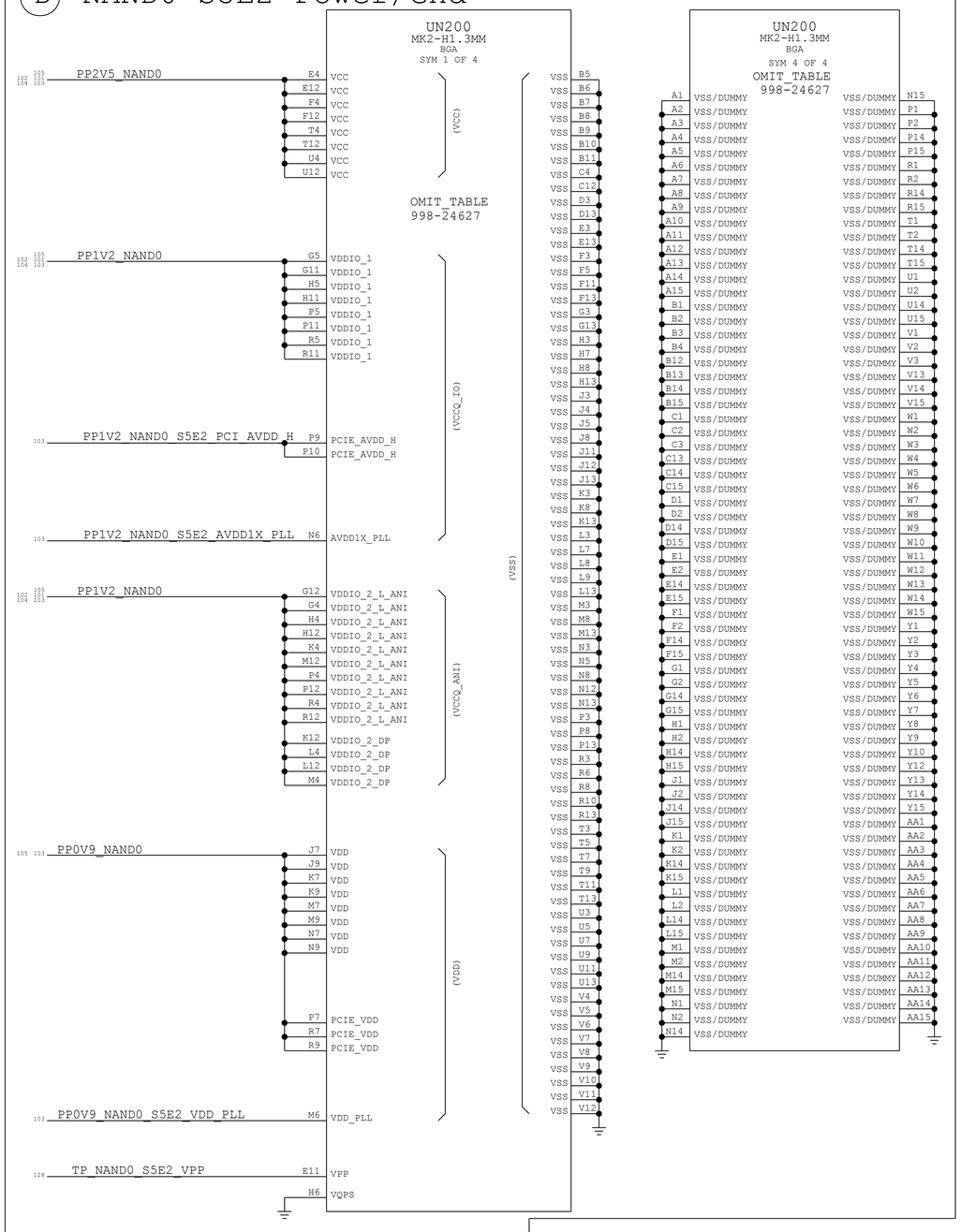
C NAND0 S5E2 Bulk Miscellaneous



PCB designers should add stiching vias for RFU/RFU_2 NC pins



D NAND0 S5E2 Power/Gnd



BOM_COST_GROUP=SSD

PAGE TITLE	STORAGE: SSD0 S5E MK2 <2>
Apple Inc.	DRAWING NUMBER 051-08242 SIZE D
	REVISION 4.0.0
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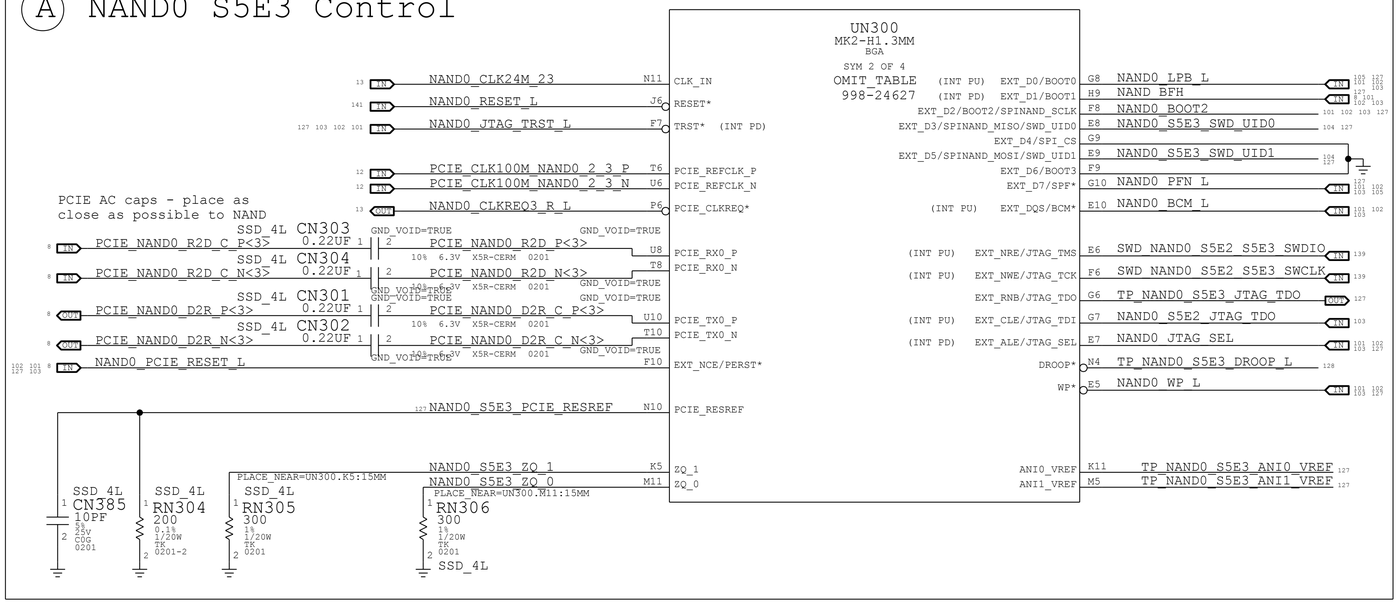
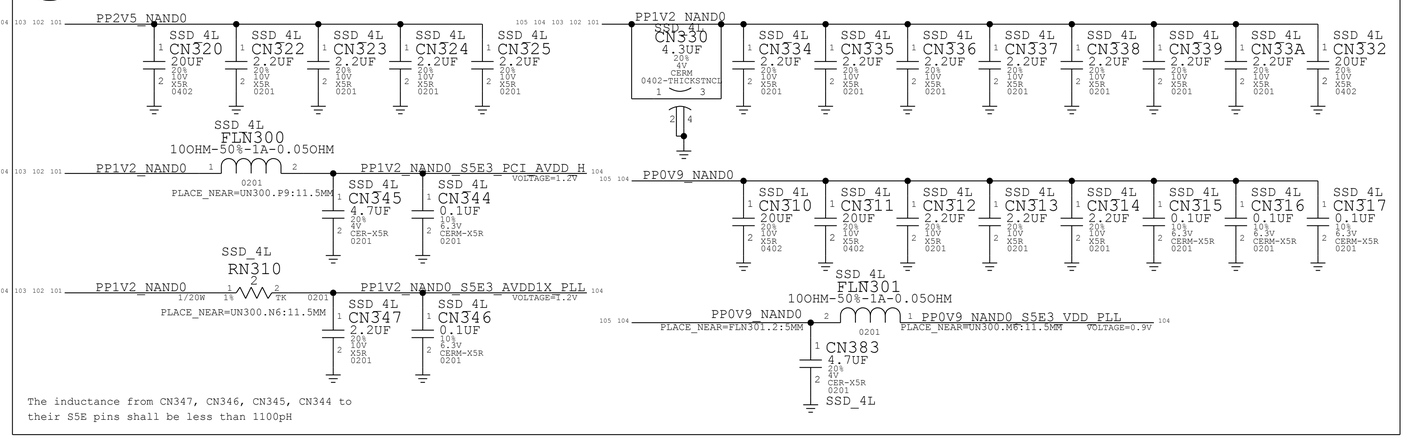
A NAND0 S5E3 Control

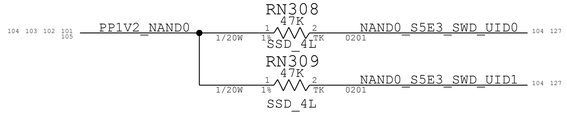


B NAND0 S5E3 Bulk Capacitance

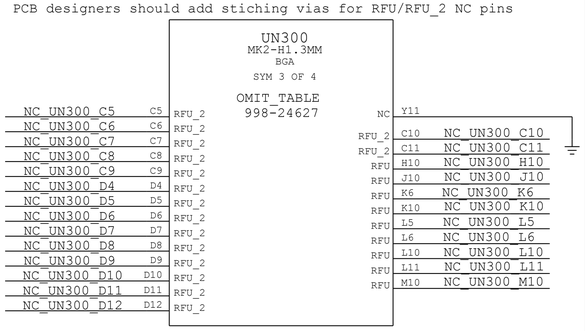


The inductance from CN347, CN346, CN345, CN344 to their S5E pins shall be less than 1100pH

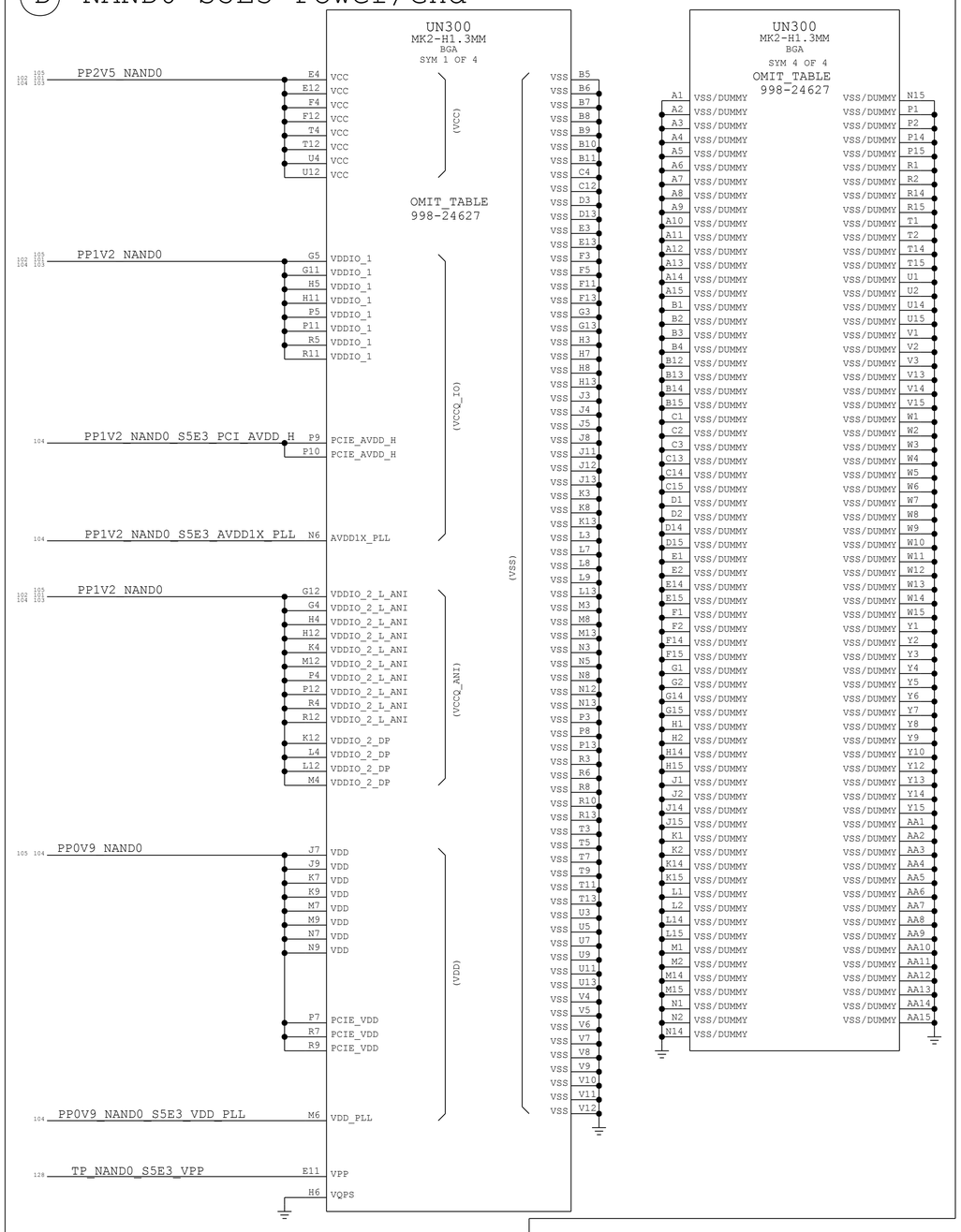
C NAND0 S5E3 Bulk Miscellaneous



PCB designers should add stiching vias for RFU/RFU_2 NC pins



D NAND0 S5E3 Power/Gnd



BOM_COST_GROUP=SSD

PAGE TITLE	STORAGE: SSD0 S5E MK2 <3>
Apple Inc.	DRAWING NUMBER 051-08242 SIZE D
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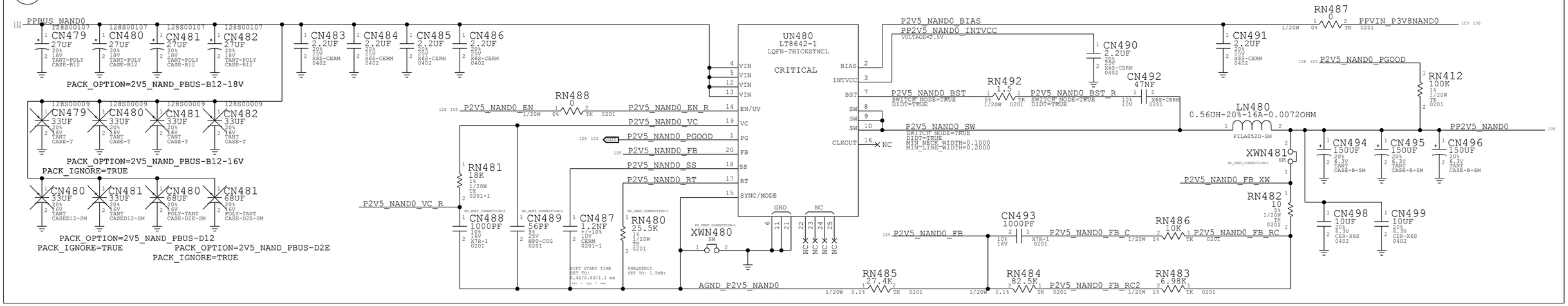
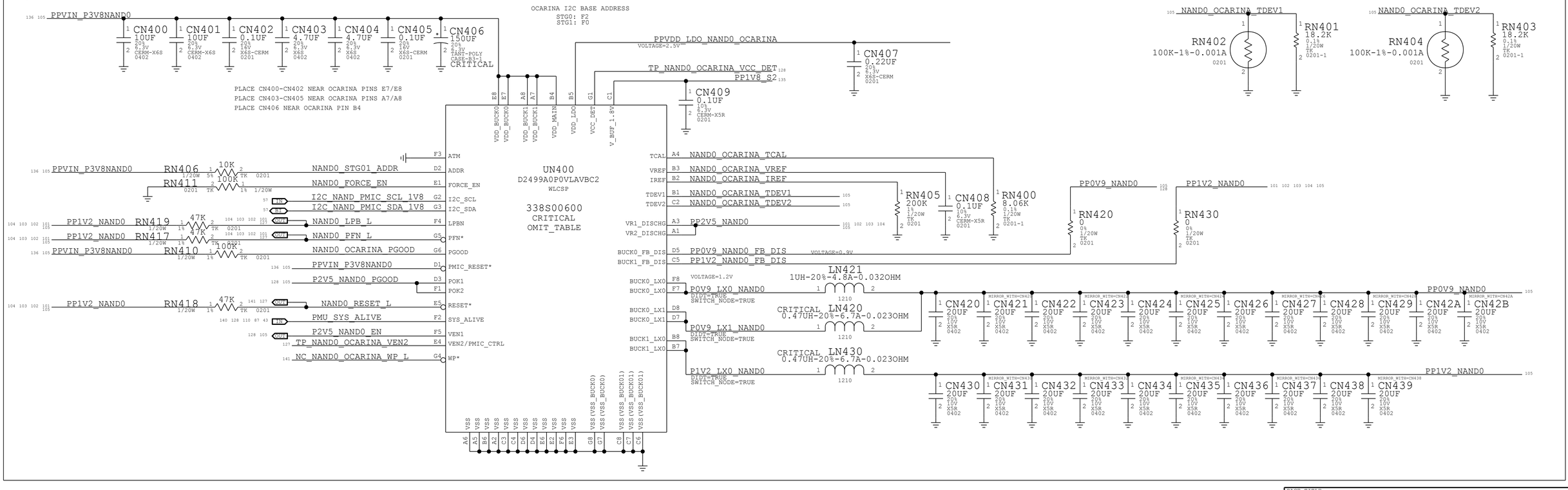
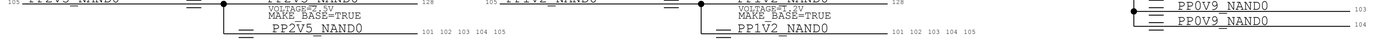
A NAND0 NAND VCC (2.5V)



B NAND0 Ocarina



C NAND0 Power Aliases



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 OCARINA & NAND VCC

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BRANCH	dvt-2
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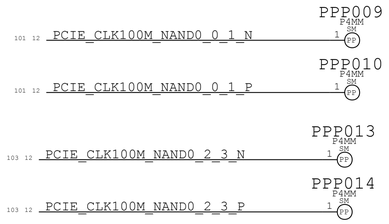
NAND CLK TEST POINTS



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD SUPPORT

Apple Inc.

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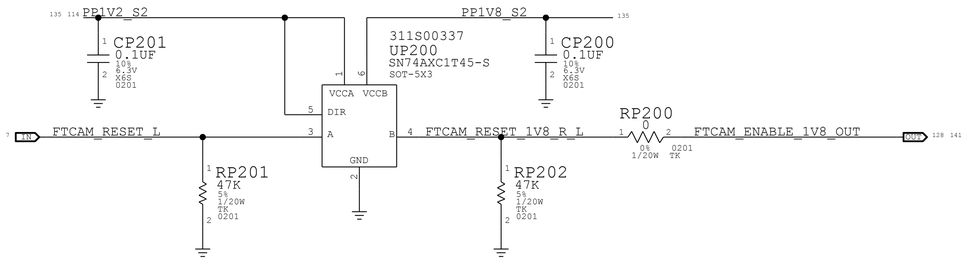
Level Shifter - FTCAM



PP CLOSE TO SOC FOR PROBING

PLACE_NEAR=U0600.BH24:5MM
PPP200
P2MM
108 7 LPDP_FTCAM_DATA_P<0> 1 SM FP

PLACE_NEAR=U0600.BG21:5MM
PPP201
P2MM
108 7 LPDP_FTCAM_DATA_N<0> 1 SM FP

BOM_COST_GROUP=CAMERA

PAGE TITLE
CAMERA-SUPPORT

Apple Inc.

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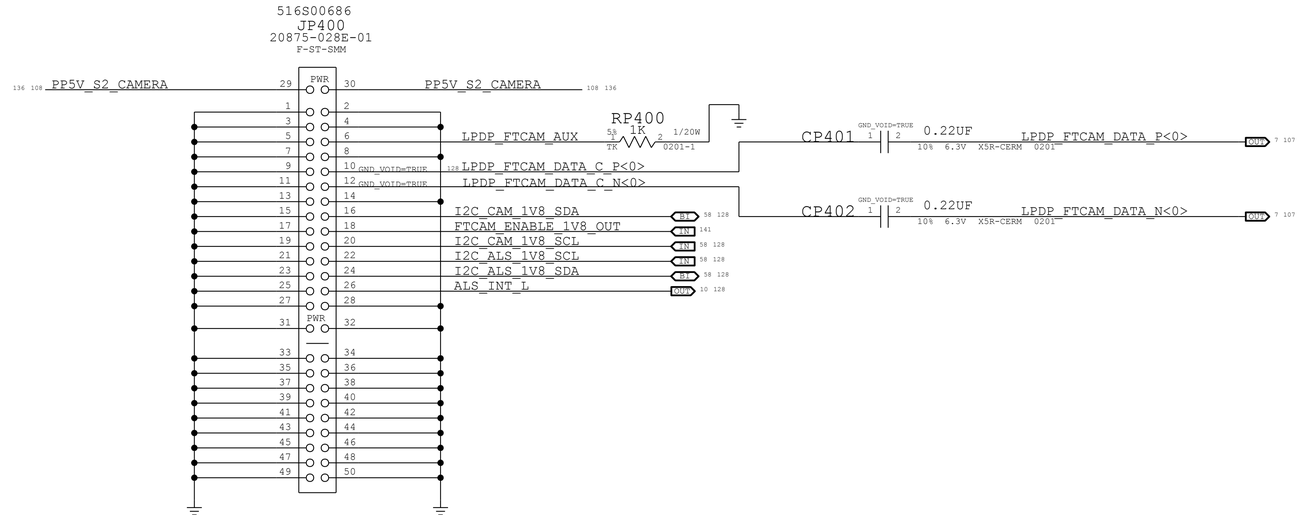

BOM_COST_GROUP=CAMERA

CAMERA: FLEX CONNECTOR

Apple Inc.

DRAWING NUMBER 051-08242

SIZE D

REVISION 4.0.0

BRANCH dvt-2

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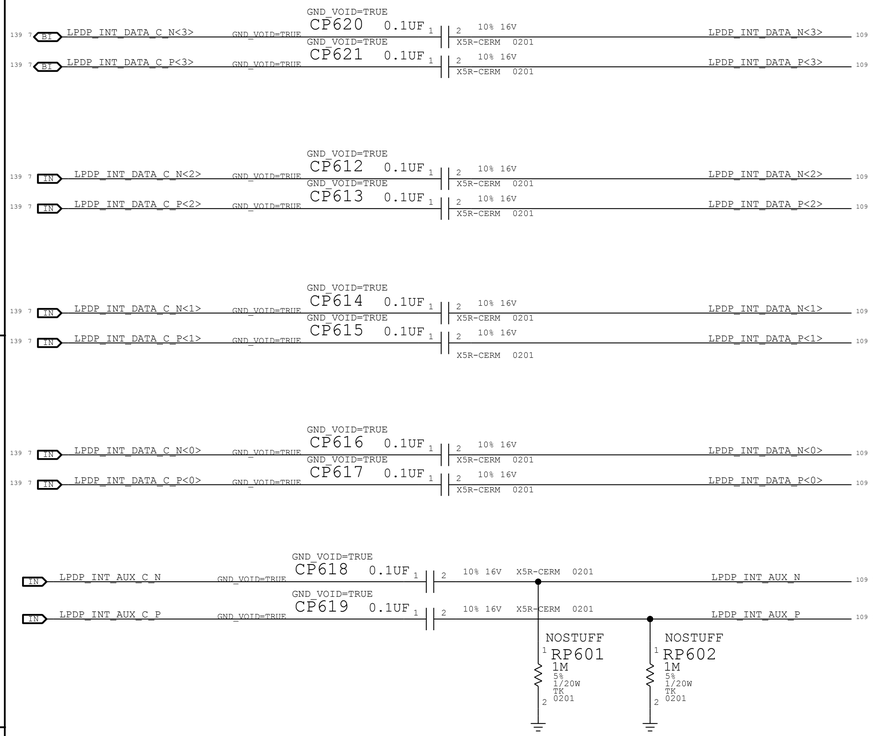
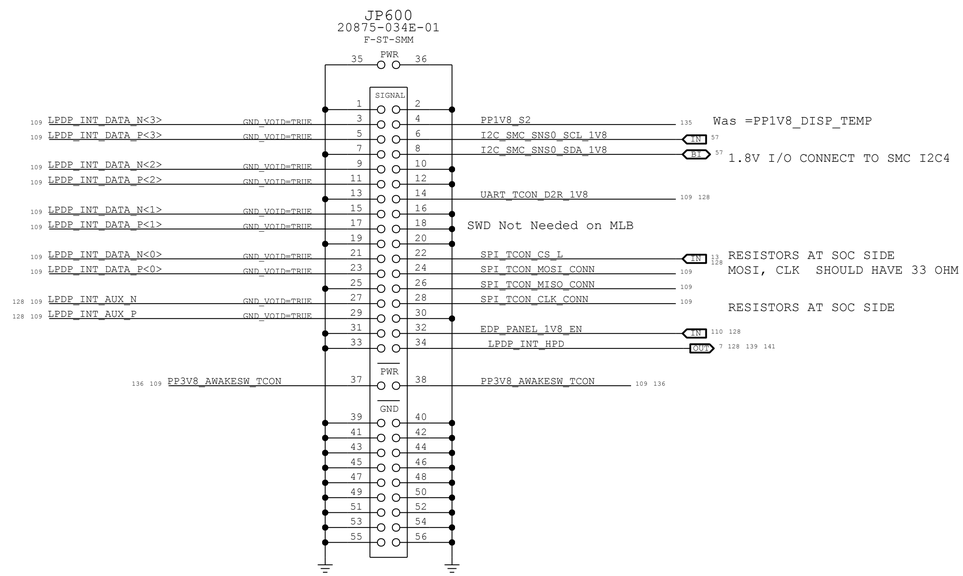
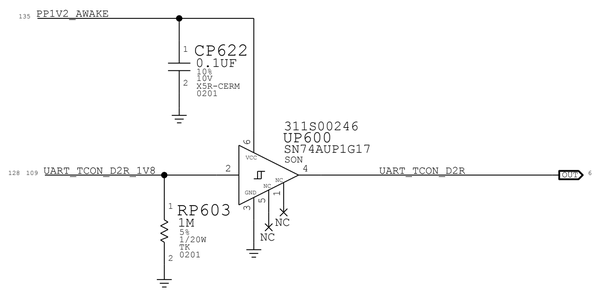


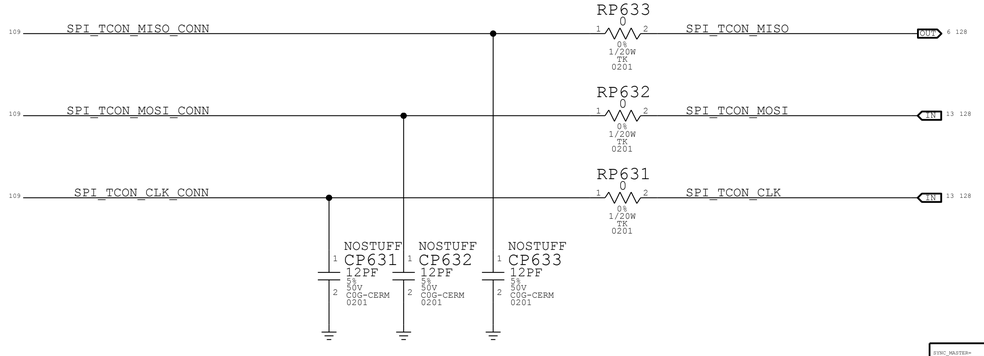
HPD NEEDS TO HAVE A 47K PD ON SOC SIDE

APN: 516S00682





RC FILTER



BOM_COST_GROUP=DISPLAY

SYNC_MASTER= SYNC_DATE=07/29/2022

PAGE TITLE
DISPLAY CONNECTOR

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*** OK2INTEGRATE ***

135 PP3V8_AON

CP730 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP730 TLV758P WSON-THICKSTNCL

IN, OUT, EN, FB, DNC, GND, EPAD

NC

RP732 49.9K 1% 1/20W TK 0201

FB_BLKT_2D

RP731 10K 1% 1/20W TK 0201

VOUT = VFB * (1 + R1/R2)
VOUT = 0.55 * (1 + 49.9/10)
VOUT = 3.2945

3V29 FEED TO BACKLIGHT

PPBCON_AWAKESW_BKLTCONN_VIN

CP731 0.1UF 10% 16V X5R-CERM 0201

CP732 10UF 20% 16V X5R-CERM 0402-7

NOSTUFF
RP730 0 0% 1/16W TK 0402

CP710 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP701 SLG5AP1564V STDFN

VDD, ON, D, S, PG, GND

NC

3V8 FEED TO MDB

PPMDB_AWAKESW_TCON 135

CP718 0.1UF 10% 16V X5R-CERM 0201

CP719 10UF 20% 16V X5R-CERM 0402-7

141 PP1V8_AON_FPMU

BYPASS=UP710::4MM
CP770 0.1UF 10% 10V X5R-CERM 0201

UP710 SLG4AP44015 STQFN

VDD, GND

35 IN LCD_PWR_EN → LCD_EN_IN

140 128 105 87 43 IN PMU_SYS_ALIVE → SYS_ALIVE

NC NC NC NC NC NC NC NC NC NC NC NC

LCD_EN_OUT → EDP_PANEL_1V8_EN OUT 109 128

PANEL_3V8_EN → EDP_PANEL_PWR_EN

BLC_1V29_EN → EDP_BKLT_1V29_EN OUT 35 129

CONTROLS 1.29V LDO IN PMIC

PANEL_DISCHARGE → EDP_PANEL_DISCHARGE

RP700 300 5% 1/16W TK 0402

PPPANEL_PANEL_DISCHARGE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=4V

DMN2250UFB DFN1006-3 QP700

RP701 100K 5% 1/20W TK 0201

BOM_COST_GROUP=DISPLAY

PAGE TITLE: DISPLAY POWER SEQUENCER

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
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BRANCH: dvt-2
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*** OK2INTEGRATE***

CP800 AND CP801 MUST BE MIRRORED

CP834 AND CP835 MUST BE MIRRORED

RP850 0.01 MF_LW 0.5% 0612-1-COMBO — VOLTAGE=13.1V

PPBUS_AON_LUXE

NOSTUFF CP800 10UF 20% 16V CER-X6S 0603

NOSTUFF CP801 10UF 20% 16V CER-X6S 0603

128S00009 CAPDERATE CP802 33UF 20% 16V TANT CASE-T POLY-TANT

128S00009 CAPDERATE CP803 33UF 20% 16V TANT CASE-T POLY-TANT

POLY-TANT PACK_OPTION=POLY_PBUS:16V PACK_OPTION=POLY_PBUS:16V

128S00107 CAPDERATE CP802 27UF 20% 18V TANT-POLY CASE-B12 POLY-TANT

128S00107 CAPDERATE CP803 27UF 20% 18V TANT-POLY CASE-B12 POLY-TANT

POLY-TANT PACK_OPTION=POLY_PBUS:18V PACK_OPTION=POLY_PBUS:18V

LUXE_ISH_P — RP801 0 0% 1/20W TK 0201 — LUXE_ISH_N

LUXE_ISH_R_P — RP802 0 0% 1/20W TK 0201 — LUXE_ISH_R_N

QP800 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL — 4LUXE_UG1 — RP832 2.49 1% 1/16W TK 0402

QP802 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL — 4LUXE_LG1 — RP831 2.49 1% 1/16W TK 0402

PPLUXE_LG1_S VOLTAGE=1V

QP801 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL — LUXE_UG2_R — RP833 2.49 1% 1/16W TK 0402

QP803 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL — LUXE_LG2_R — RP830 2.49 1% 1/16W TK 0402

LP800 2.2UH-20%-8.0A-0.0501OHM PIMS052T-SM — PPLUXE_LX1 — PPLUXE_LX2

PPVOUT_LUXE_XW VOLTAGE=15V — XWP801 SM — PPVOUT_LUXE VOLTAGE=15V

CP830 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP831 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP832 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP833 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP834 0.1UF 5% 50V COG 1206

CP835 0.1UF 5% 50V COG 1206

RP803 0 0% 1/20W TK 0201 — LUXE_ISL_R_P — LUXE_ISL_P

RP804 0 0% 1/20W TK 0201 — LUXE_ISL_R_N — LUXE_ISL_N

RP809 0.01 0.5% 1W MF 0612-1-COMBO

CP823 0.1UF 10% 25V X5R 402

CP822 0.1UF 10% 25V X5R 402

RP820 4.32K 1% 1/16W TK 0402 — LUXE_COMP_R

CP820 0.022UF 20% 16V X7R-CERM 0402

CP821 56PF 5% 50V CERM 0402 — LUXE_COMP — LUXE_AGND

RP881 0 0% 1/20W TK 0201 — BKLT_BOOST_THROTTLE_L — BKLT_BOOST_THROTTLE_R_L

OD SIGNAL.
47K PU IS ON THE BCON CONNECTOR PAGE

RP860 100K 5% 1/20W TK 0201 — LUXE_FAULT

PP5V_S2_HOLD — RP805 10 5% 1/16W TK 0402 — CP870 2.2UF 20% 25V X5R-CERM 0402-1 — PLACE_NEAR=UP800.C2:5MM

PVOUT_LUXE_R — RP880 0 0% 1/20W TK 0201

CP880 12PF 5% 50V COG-CERM 0201 NOSTUFF — LUXE_AGND

XWP800 SM — PGND PGND DGND AGND AGND AGND — LUXE_AGND VOLTAGE=0V

UP800 RAA209100B WLCSP OMIT_TABLE

VGD VGD — LUXE_C_VDD VOLTAGE=2.5V — PP5V_S2_LUXE_VDDA VOLTAGE=5V — PPBUS_AON_LUXE — PP1V2_AWAKE — LUXE_AGND

CP810 2.2UF 20% 25V X5R-CERM 0402-1

CP811 2.2UF 20% 25V X5R-CERM 0402-1

CP812 2.2UF 20% 25V X5R-CERM 0402-1

PP5V_S2_HOLD — RP840 100K 5% 1/20W TK 0201 NOSTUFF — LUXE_VPROG_TEST

PP1V2_AWAKE — RP842 100K 1/20W 5% TK 0201 — RP841 100K 1/20W 5% TK 0201

RP870 10K 5% 1/20W TK 0201 — LUXE_AGND

RP871 10K 5% 1/20W TK 0201 — LUXE_BYP

RP872 10K 5% 1/20W TK 0201 — LUXE_TEST

I2C_LUXE_DEBUG_SCL

I2C_LUXE_DEBUG_SDA

SPMI_DISP_BKLT_CLK

SPMI_DISP_BKLT_DATA

BL_PWR_EN — RP873 0 1/20W 0% TK 0201 — BL_PWR_EN_R — LUXE_AGND

NOSTUFF CP813 33PF 5% 25V NP0-C0G 0201

NOSTUFF CP814 33PF 5% 25V NP0-C0G 0201

NOSTUFF CP815 100PF 5% 50V C0G 0402

NOSTUFF CP816 100PF 5% 50V C0G 0402

CP817 100PF 5% 50V C0G 0402

CP818 100PF 5% 50V C0G 0402 — LUXE_AGND

BOM_COST_GROUP=DISPLAY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S02811	1	IC,RAA209100,A1,BUCK-BOOST CTRLR,WLCSP36	UP800	

PAGE TITLE: LUXE LCD Backlight Driver

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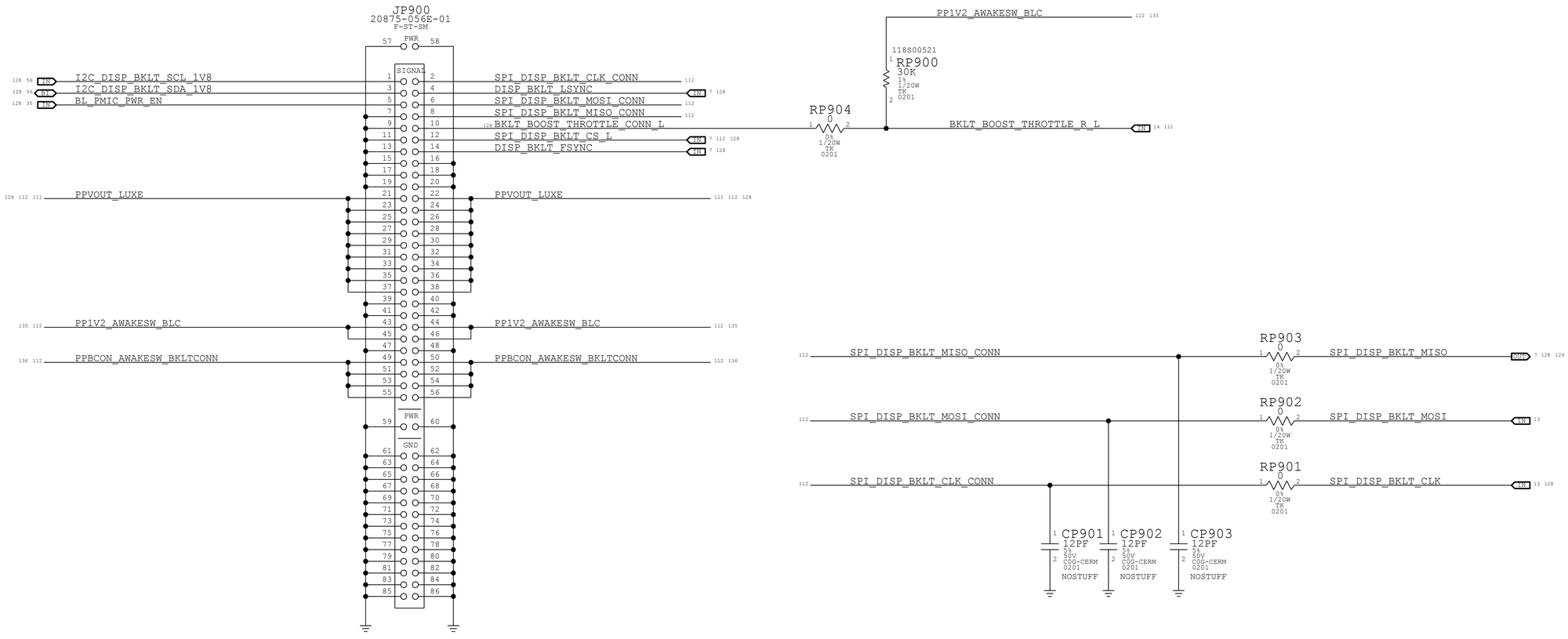

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=

SYNC_DATE=08/03/2022

PAGE TITLE

BCON CONNECTOR

Apple Inc.

DRAWING NUMBER 051-08242

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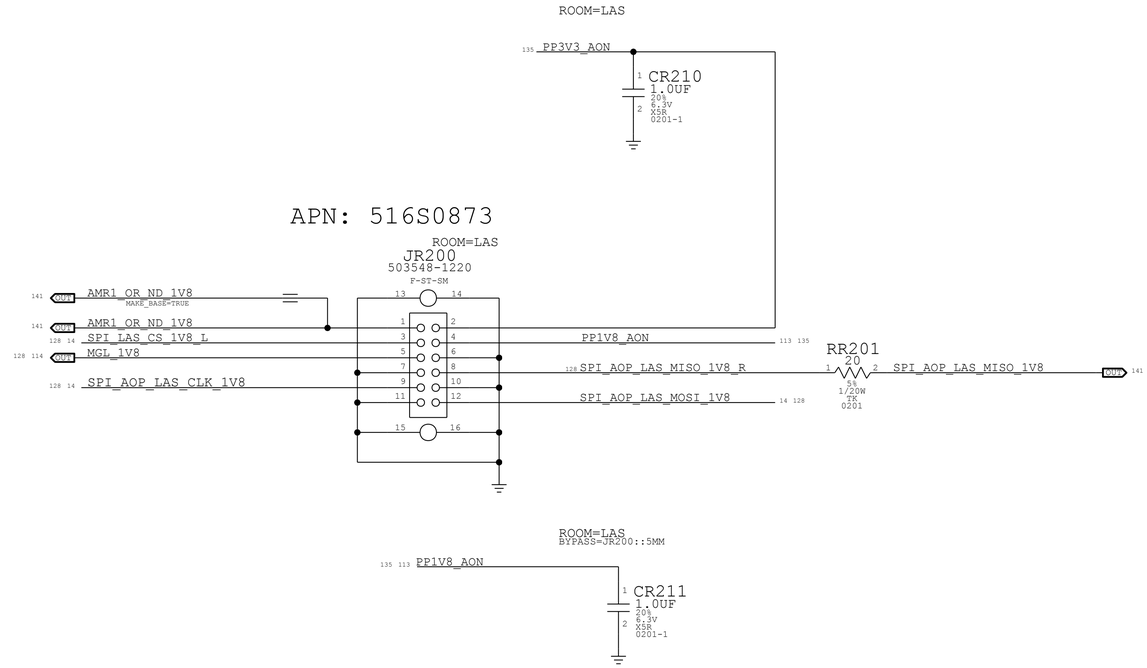
*** OK2INTEGRATE ***



CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	22UA	1.2MA
1.8 AON	30UA	8 MA
3.3 AON	1UA	10 MA

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: LID ANGLE SENSOR

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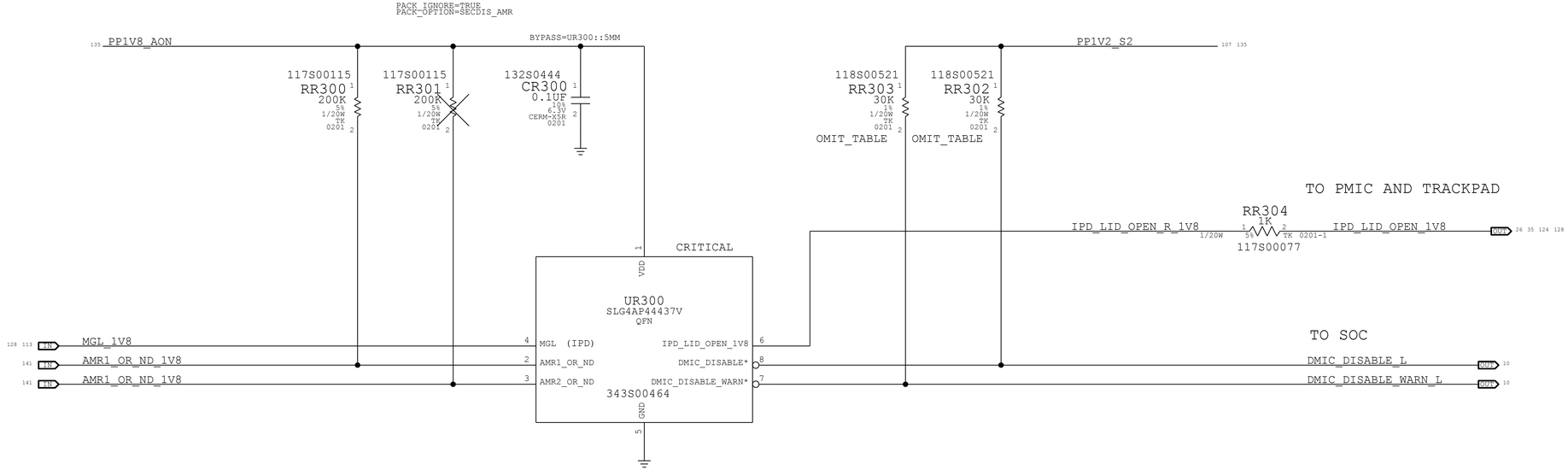
LID SECDIS LOGIC



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_SOC_PU:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_SOC_PU:30K

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: SAK

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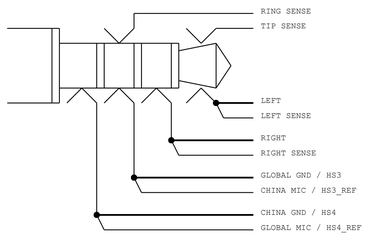
*** OK2INTEGRATE ***

CARLOW CODEC I2C ADDRESS	
ADDR PIN	ADDRESS
0R TO GND	0X48
100K TO GND	0X49
100K TO VDDIO	0X4A
0R TO VDDIO	0X4B <--

AUDIO JACK PINOUT



LR500 FERR-22-OHM-1A-0.055OHM 0201
PP1V2_AWAKE — EDC CURRENT = 20MA, TDC CURRENT = 10MA
PP1V2_CODEC_VL_VD — MIN_LINE_WIDTH=0.1500, MIN_NECK_WIDTH=0.1000, VOLTAGE=1.225V
BYPASS=UR500.A6:A7:5MM
CR500 1.0UF 20% 6.3V X5R 0201-1
BYPASS=UR500.A1:A2:5MM
CR501 0.1UF 10% 6.3V CERM-X5R 0201

LR503 FERR-22-OHM-1A-0.055OHM 0201
PP3V8_AON — EDC CURRENT = 850MA, TDC CURRENT = 110MA
PP3V8_CODEC_VP — MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
BYPASS=UR500.C7:A7:5MM
CR504 10UF 20% 10V X5R-CERM 0402-7

PP1V8_CODEC_VA — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=1.8V
LR501 FERR-22-OHM-1A-0.055OHM 0201 — PP1V8_AWAKE (* SEE NOTE) — EDC CURRENT = 400MA, TDC CURRENT = 150MA
NO_XNET_CONNECTION=1, BYPASS=UR500.B1:C2:4MM
CR502 2.2UF 20% 35V X5R-CERM 0402-0.1MM
CODEC_AGND
LR502 FERR-22-OHM-1A-0.055OHM 0201
PP1V8_CODEC_VCP — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500, VOLTAGE=1.8V
CODEC_CP_LDO_FILT — NO_XNET_CONNECTION=1, BYPASS=UR500.D5:F6:5MM
CR505 2.2UF 20% 35V X5R-CERM 0402-0.1MM
NO_XNET_CONNECTION=1, BYPASS=UR500.B6:F6:6MM
CR503 2.2UF 20% 35V X5R-CERM 0402-0.1MM
PLACE_NEAR=CR506.2:5MM
XWR500 SM
CODEC_VCP_FILT_GND — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500
CODEC_VCP_FILTP — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500
NO_XNET_CONNECTION=1, BYPASS=UR500.E6:F6:4MM
CR506 4.7UF 20% 25V X5R 0402
NO_XNET_CONNECTION=1, BYPASS=UR500.F6:G6:4MM
CR507 4.7UF 20% 25V X5R 0402
CODEC_VCP_FILTM — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1500

PP1V2_AWAKE
PP1V2_S2
NOSTUFF RR502 47K 5% 1/20W TK 0201
NOSTUFF RR503 47K 5% 1/20W TK 0201
CODEC_INT_L (OUT) 6 127 -> TO SOC
CODEC_WAKE_L (OUT) 43 127 -> TO PMU
CODEC_RESET_L (IN) 10 127 <- FROM SOC
RR504 47K 5% 1/20W TK 0201

AUDIO_JACK_LEFT_OUT (OUT) 119
AUDIO_JACK_RIGHT_OUT (OUT) 119 * SEE NOTE
NO_XNET_CONNECTION=1, NOSTUFF RR500 1K 5% 1/20W TK 0201-1
NO_XNET_CONNECTION=1, RR501 1K 5% 1/20W TK 0201-1 NOSTUFF
CODEC_AGND 115
AUDIO_JACK_LEFT_SNS (IN) 119
AUDIO_JACK_RIGHT_SNS (IN) 119
AUDIO_JACK_CH_GND (IN) 119
AUDIO_JACK_GB_GND (IN) 119 * SEE NOTE
AUDIO_JACK_GB_MIC (IN) 119 — CR512 0.1UF 10% 50V X7R 0603 — CODEC_GB_MIC
AUDIO_JACK_CH_MIC (IN) 119 * SEE NOTE — CR513 0.1UF 10% 50V X7R 0603 — CODEC_CH_MIC
AUDIO_JACK_RING_SNS (IN) 119
AUDIO_JACK_TIP_SNS (IN) 119

TO / FROM AUDIO JACK CONNECTOR

UR500 CS42L84A WLCSP — CRITICAL

		VDD_P C7	VDD_IO A1	VDD_D A6	VDD_A B1	VDD_CP D6	
HP_SENSEA	F5						CP_LDO_FILT D5
OUTA_HP	G5						CP_FILTP E6
HP_SENSEB	F4						CP_FILTN G6
OUTB_HP	G4						GND_CP F6
HS4	F1						LDO_EN C6
HS4_CLAMP	E2						IRQ* B7
HS3	G2						WAKE* C5
HS3_CLAMP	F2						RESET* D4
IN_HSP	D1						MCLK A4
IN_HSN	E1						ASP_FSYNC B2
HS4_REF	G3						ASP_DIN B3
HS3_REF	E4						ASP_DOUT B4
RING_SENSE	F3						ASP_BCLK A3
TIP_SENSE	E5						I2C_ADDR B5
HSBIAS_FILT	E3						I2C_SDA B6
HSBIAS_FILT_REF	D3						I2C_SCL A5
FILTP	C1						CP_FLY1P D7
							CP_FLY1N E7
							CP_FLY2P F7
							CP_FLY2N G7
		TSTI C3	GND_IO C4	GND_D A2	GND_HS A7	GND_A G1	C2 D2

TDM_CODEC_FSYNC (IN) 13 127
TDM_CODEC_D2R_R — RR505 33 5% 1/20W TK 0201 PLACE_NEAR=UR500.B4:5MM — TDM_CODEC_D2R (OUT) 6 127
TDM_CODEC_R2D (IN) 13 127
TDM_CODEC_BCLK (IN) 13 127
PP1V2_CODEC_VL_VD 115
I2C_CODEC_SDA (BI) 56 127
I2C_CODEC_SCL (IN) 56 127

CODEC_FLY1P, CODEC_FLY1M, CODEC_FLY2P, CODEC_FLY2M
CR508 4.7UF 20% 25V X5R 0402 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, NO_XNET_CONNECTION=1, BYPASS=UR500.D7:E7:4MM
CR509 4.7UF 20% 25V X5R 0402 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, NO_XNET_CONNECTION=1, BYPASS=UR500.F7:G7:4MM

CODEC_HSBIAS_FILT — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
BYPASS=UR500.E3:D3:4MM
CR510 4.7UF 20% 10V X5R-CERM 0402
CODEC_FILT — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
CODEC_HSBIAS_FILT_REF — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000
NO_XNET_CONNECTION=1, BYPASS=UR500.C1:C2:3 MM
CR511 10UF 20% 10V X5R 0603-1
CODEC_AGND 115

XWR501 SM — PLACE_NEAR=UR500.G1:2MM — CODEC_AGND 115

NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1

- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND

- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
  CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.

- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO
  COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP
  WHEN THE OTHER RAILS GO DOWN)
  VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  3.1UA (1V8 OFF, RST# LOW)
  TBD (1V8 ON, RST# LOW)
  37UA (1V8 OFF, RST# HIGH)

CARLOW B0 SILICON

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

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*** OK2INTEGRATE ***

AMP A

PP1V8_AWAKE
PP1V2_AWAKE
SPKRAMP_A_DREG
CR600 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR600.E5:5MM
CR601 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR600.F5:5MM
CR602 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR600.C2:5MM

OMIT_TABLE
UR600
SN012776B0YBH
DSBGA
SPKRAMP_A
TAWANG B0

I2C_SPKRAMP_L_SCL
I2C_SPKRAMP_L_SDA
SPKRAMP_A_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
TDM_SPKRAMP_L_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_A_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR600 33 5% 1/20W TK 0201 — SPKRAMP_A — PLACE_NEAR=UR600.D1:10MM — TDM_SPKRAMP_A_D2R_R
RR601 33 5% 1/20W TK 0201 — SPKRAMP_A — PLACE_NEAR=UR600.F5:10MM — SPKRAMP_A_ICC_R

PP3V8_AON
MAX CURRENT EDC = 1A (PER AMP)
PPBUS_AON_SPKRAMP_ABC
MAX CURRENT EDC = 4A (PER AMP)

CR603 0.1UF 10% 25V X5R 0201 — SPKRAMP_A — PLACE_NEAR=UR600.C5:5MM
CR604 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_A — PLACE_NEAR=UR600.C5:10MM
CR605 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_A — PLACE_NEAR=UR600.C5:10MM
CR606 0.1UF 10% 25V X5R 0201 — SPKRAMP_A — PLACE_NEAR=UR600.D5:5MM
CR607 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_A — PLACE_NEAR=UR600.D5:10MM

XWR600 SHORT-16L-0.1MM-SM * SEE NOTE — SPKRAMP_A

SPKRAMP_A_PVDD_SNS
SPKRAMP_A_VSENSEP * SEE NOTE
SPKRAMP_A_VSENSEN

SPKRAMP_A BYPASS=UR600.B2:B3:10MM NO_XNET_CONNECTION=1

SPKRAMP_A_BOOTP — MIN_LINE_WIDTH=0.1000 — CR608 0.1UF 10% 25V X5R 0201
SPKRAMP_A_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — * SEE NOTE — RR602 0 1% 1/20W TK 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE — SPKRAMP_A_OUTP * SEE NOTE
SPKRAMP_A_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — * SEE NOTE — RR603 0 1% 1/20W TK 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE — SPKRAMP_A_OUTN * SEE NOTE
SPKRAMP_A_BOOTN — MIN_LINE_WIDTH=0.1000 — CR609 0.1UF 10% 25V X5R 0201

CR610 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR611 12PF 5% 25V CERM 0201 — OMIT_TABLE

PP1V8_AWAKE
RR605 0 5% 1/20W TK 0201 — SPKRAMP_A_ADDR 0x70
RR635 470 5% 1/20W TK 0201 — SPKRAMP_B_ADDR 0x72
RR664 470 5% 1/20W TK 0201 — SPKRAMP_C_ADDR 0x74

AMP B

PP1V8_AWAKE
PP1V2_AWAKE
SPKRAMP_B_DREG
CR630 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR630.E5:5MM
CR631 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR630.F5:5MM
CR632 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR630.C2:5MM

OMIT_TABLE
UR630
SN012776B0YBH
DSBGA
SPKRAMP_B
TAWANG B0

I2C_SPKRAMP_L_SCL
I2C_SPKRAMP_L_SDA
SPKRAMP_B_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
TDM_SPKRAMP_L_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_B_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR630 33 5% 1/20W TK 0201 — SPKRAMP_B — PLACE_NEAR=UR630.D1:10MM — TDM_SPKRAMP_B_D2R_R
RR631 33 5% 1/20W TK 0201 — SPKRAMP_B — PLACE_NEAR=UR630.F5:10MM — SPKRAMP_B_ICC_R

PP3V8_AON
PPBUS_AON_SPKRAMP_ABC

CR633 0.1UF 10% 25V X5R 0201 — SPKRAMP_B — PLACE_NEAR=UR630.C5:5MM
CR634 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_B — PLACE_NEAR=UR630.C5:10MM
CR635 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_B — PLACE_NEAR=UR630.C5:10MM
CR636 0.1UF 10% 25V X5R 0201 — SPKRAMP_B — PLACE_NEAR=UR630.D5:5MM
CR637 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_B — PLACE_NEAR=UR630.D5:10MM

XWR601 SHORT-16L-0.1MM-SM * SEE NOTE — SPKRAMP_B

SPKRAMP_B_PVDD_SNS
SPKRAMP_B_VSENSEP * SEE NOTE
SPKRAMP_B_VSENSEN

SPKRAMP_B BYPASS=UR630.B2:B3:10MM NO_XNET_CONNECTION=1

SPKRAMP_B_BOOTP — MIN_LINE_WIDTH=0.1000 — CR638 0.1UF 10% 25V X5R 0201
SPKRAMP_B_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — * SEE NOTE — RR632 0 1% 1/20W TK 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE — SPKRAMP_B_OUTP * SEE NOTE
SPKRAMP_B_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — * SEE NOTE — RR633 0 1% 1/20W TK 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE — SPKRAMP_B_OUTN * SEE NOTE
SPKRAMP_B_BOOTN — MIN_LINE_WIDTH=0.1000 — CR639 0.1UF 10% 25V X5R 0201

CR640 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR641 12PF 5% 25V CERM 0201 — OMIT_TABLE

PP1V2_AWAKE
NOSTUFF
RR691 47K 5% 1/20W TK 0201
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR692 47K 5% 1/20W TK 0201

THIS RESISTOR TIES ICC SIGNAL
BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)

SPKRAMP_ICC_GB
RR693 0 5% 1/20W TK 0201 — SPKRAMP_ABC_ICC — SPKRAMP_ICC — SPKRAMP_ICC_GB

AMP C

PP1V8_AWAKE
PP1V2_AWAKE
SPKRAMP_C_DREG
CR660 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR660.E5:5MM
CR661 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR660.F5:5MM
CR662 1.0UF 20% 6.3V X5R 0201-1 — PLACE_NEAR=UR660.C2:5MM

OMIT_TABLE
UR660
SN012776B0YBH
DSBGA
SPKRAMP_C
TAWANG B0

I2C_SPKRAMP_L_SCL
I2C_SPKRAMP_L_SDA
SPKRAMP_C_ADDR
TDM_SPKRAMP_L_BCLK
TDM_SPKRAMP_L_FSYNC
TDM_SPKRAMP_L_R2D
TDM_SPKRAMP_L_D2R
SPKRAMP_ABC_ICC
TP_SPKRAMP_C_LV_EN
SPKRAMP_INT_L
SPKRAMP_RESET_L

RR660 33 5% 1/20W TK 0201 — SPKRAMP_C — PLACE_NEAR=UR660.D1:10MM — TDM_SPKRAMP_C_D2R_R
RR661 33 5% 1/20W TK 0201 — SPKRAMP_C — PLACE_NEAR=UR660.F5:10MM — SPKRAMP_C_ICC_R

PP3V8_AON
PPBUS_AON_SPKRAMP_ABC

CR663 0.1UF 10% 25V X5R 0201 — SPKRAMP_C — PLACE_NEAR=UR660.C5:5MM
CR664 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_C — PLACE_NEAR=UR660.C5:10MM
CR665 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_C — PLACE_NEAR=UR660.C5:10MM
CR666 0.1UF 10% 25V X5R 0201 — SPKRAMP_C — PLACE_NEAR=UR660.D5:5MM
CR667 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_C — PLACE_NEAR=UR660.D5:10MM

XWR602 SHORT-16L-0.1MM-SM * SEE NOTE — SPKRAMP_C

SPKRAMP_C_PVDD_SNS
SPKRAMP_C_VSENSEP * SEE NOTE
SPKRAMP_C_VSENSEN

SPKRAMP_C BYPASS=UR660.B2:B3:10MM NO_XNET_CONNECTION=1

SPKRAMP_C_BOOTP — MIN_LINE_WIDTH=0.1000 — CR668 0.1UF 10% 25V X5R 0201
SPKRAMP_C_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — * SEE NOTE — RR662 0 1% 1/20W TK 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE — SPKRAMP_C_OUTP * SEE NOTE
SPKRAMP_C_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — * SEE NOTE — RR663 0 1% 1/20W TK 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE — SPKRAMP_C_OUTN * SEE NOTE
SPKRAMP_C_BOOTN — MIN_LINE_WIDTH=0.1000 — CR669 0.1UF 10% 25V X5R 0201

CR670 12PF 5% 25V CERM 0201 — OMIT_TABLE
CR671 12PF 5% 25V CERM 0201 — OMIT_TABLE

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

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BRANCH dvt-2
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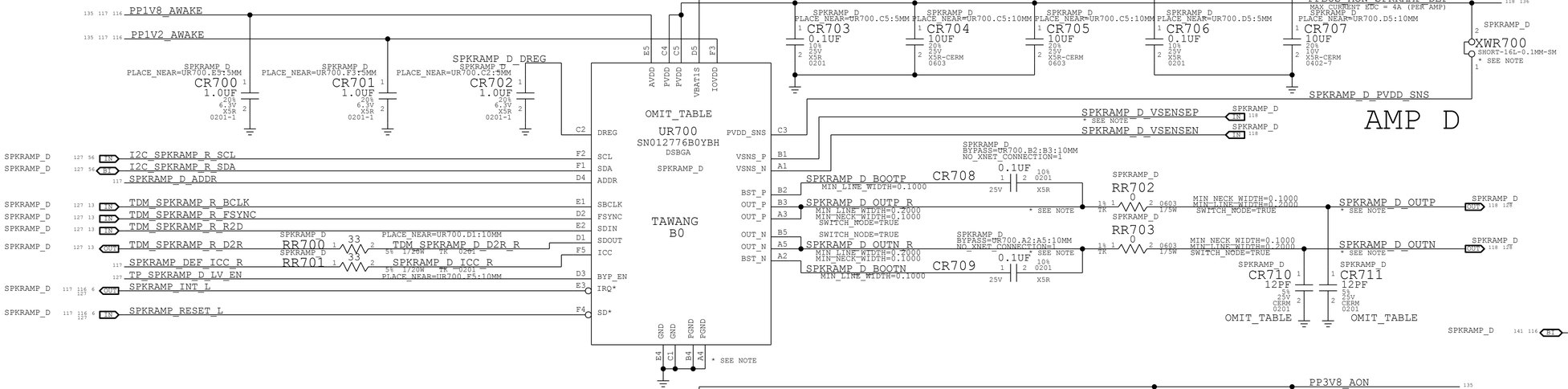
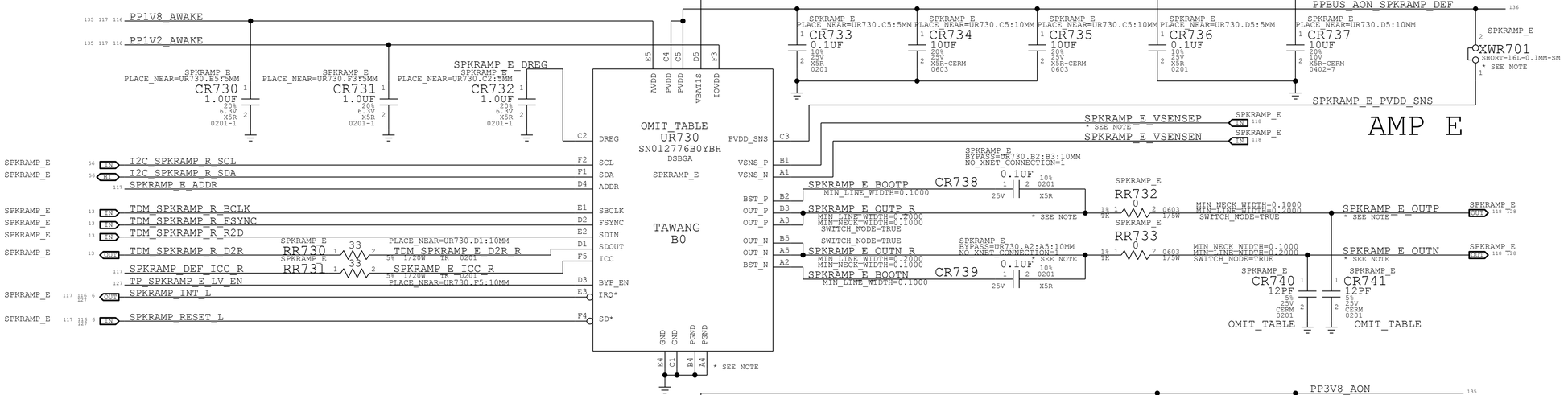
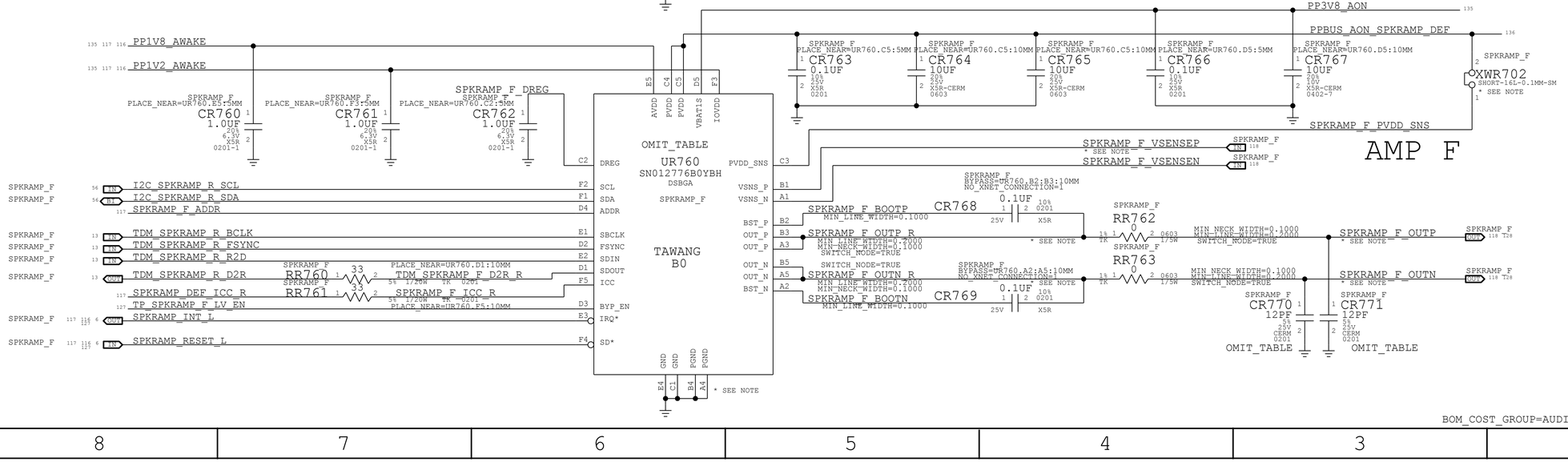
SHEET 116 OF 156

*** OK2INTEGRATE ***







NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (2/2)

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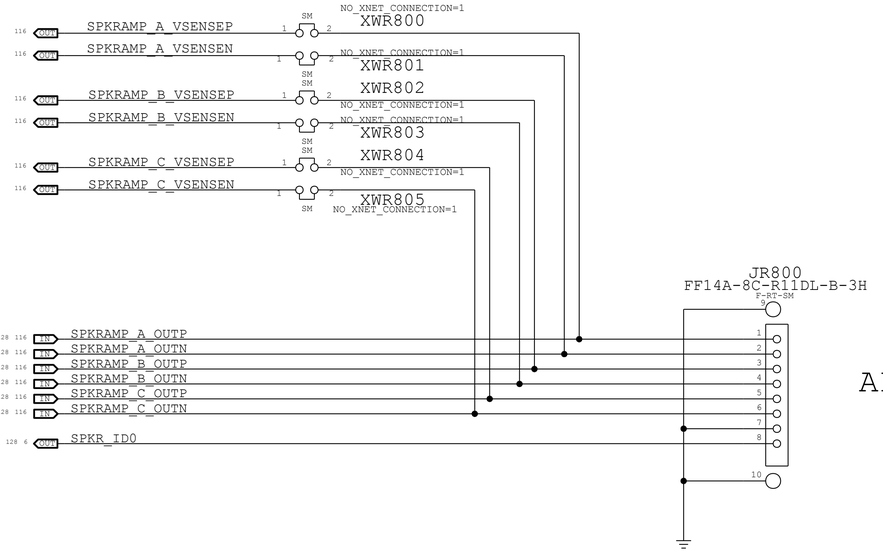
LEFT AUDIO SPEAKER CONNECTOR

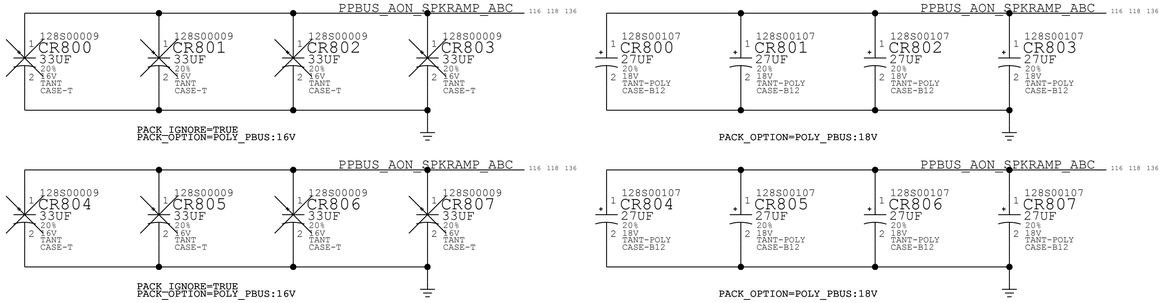


L Woofer 1

L Woofer 2

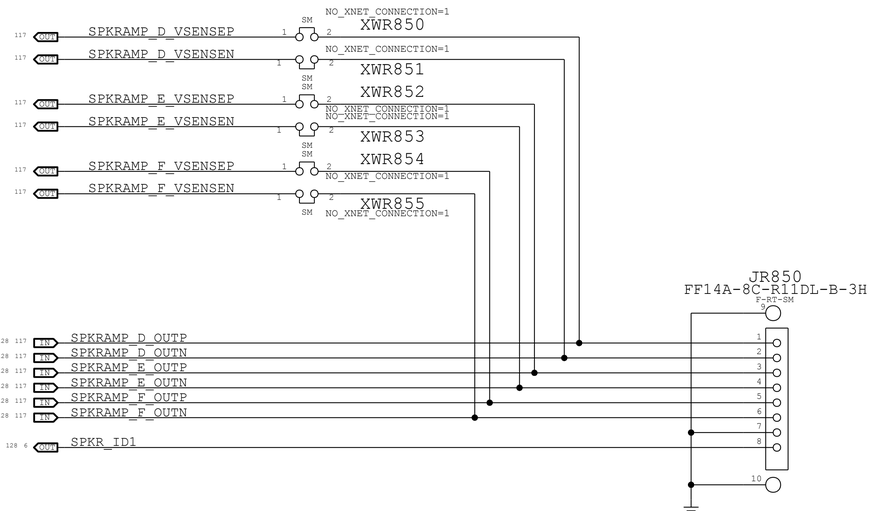
L Tweeter

LEFT AMPLIFIERS BULK CAPACITANCE



APN: 518S00164

RIGHT AUDIO SPEAKER CONNECTOR

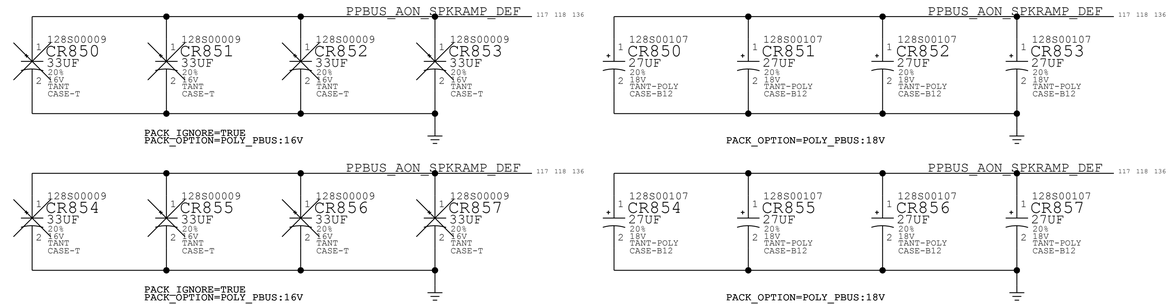


R Woofer 1

R Woofer 2

R Tweeter

RIGHT AMPLIFIERS BULK CAPACITANCE



APN: 518S00164

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO CONNECTORS: AMPS

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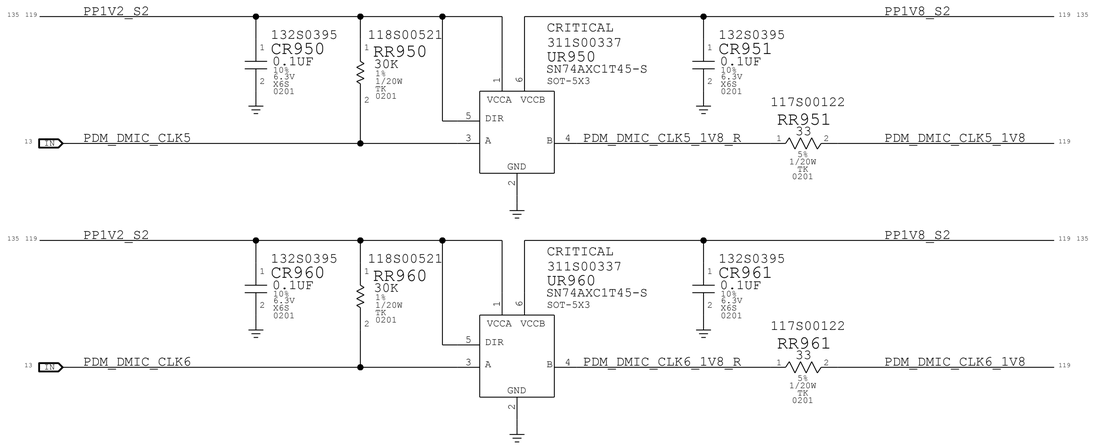
LEVEL SHIFTERS: DMIC CLOCK

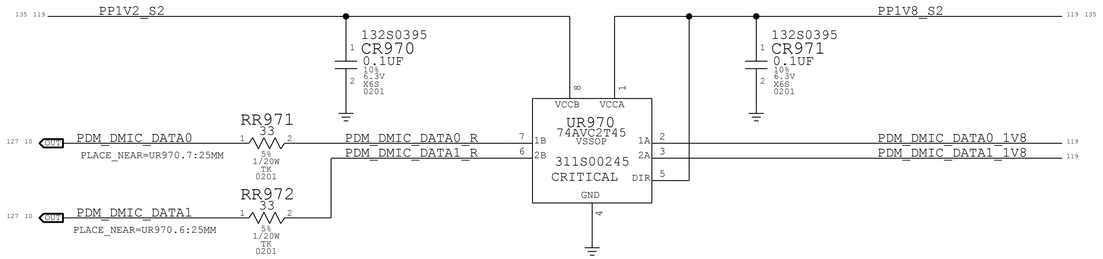
TWO SEPARATE SINGLE BIT LS FOR XTALK CONCERNS <RDAR://70058941> -- MAY CHANGE TO DUAL SHIFTER



LEVEL SHIFTER: DMIC DATA

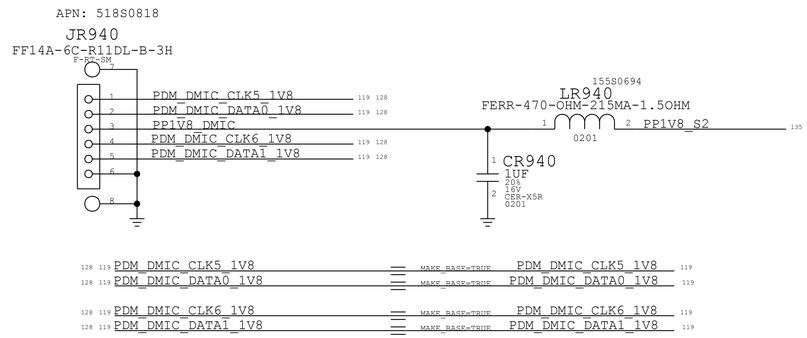
HIGH ON DIR IS A -> B

BOTH A AND B SIDE CAN BE ANY VOLTAGE FROM 0.8 TO 3.6

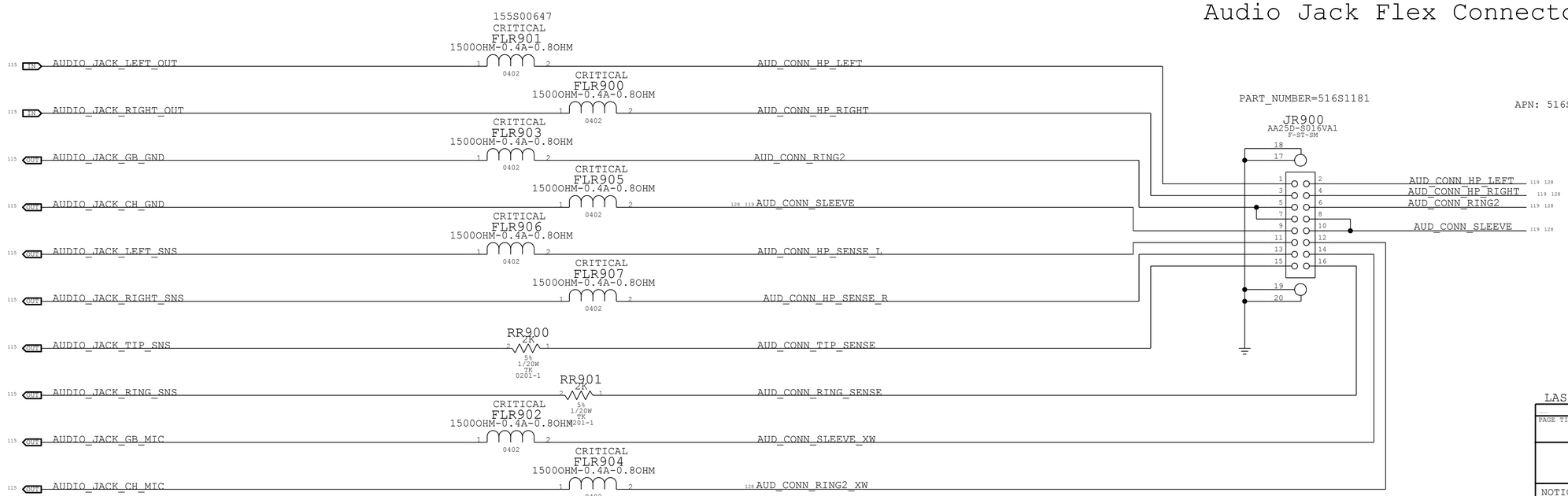


Digital Mic Flex Connector

APN: 518S0818



Audio Jack Flex Connector



LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE: AUDIO FLEX CONNECTORS

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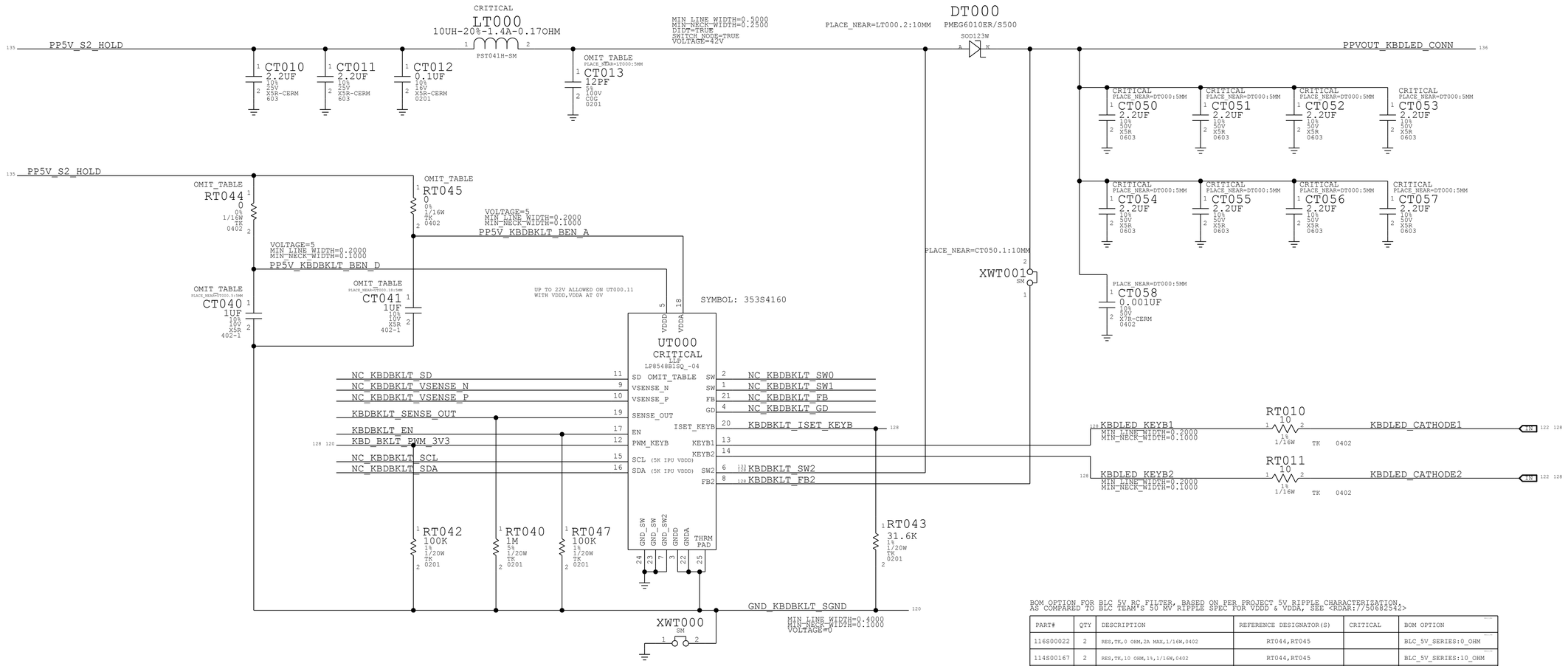
*** OK2INTEGRATE ***

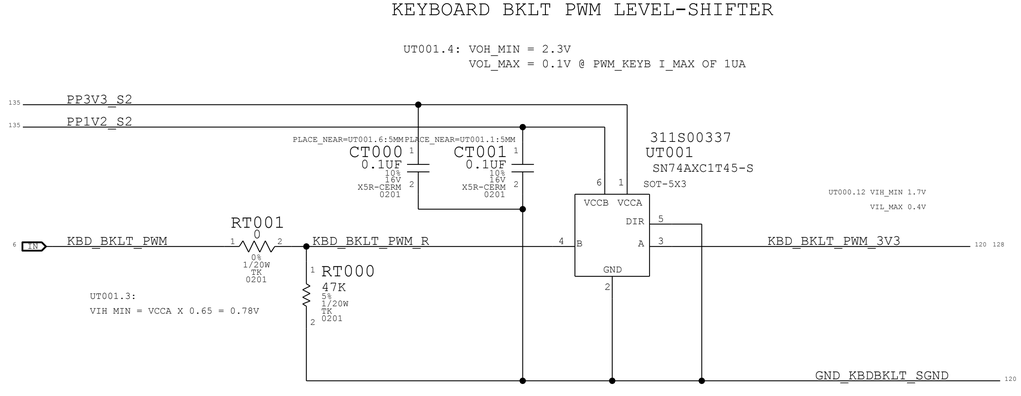
BEN IC: KEYBOARD LED DRIVER



BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION, AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR://7506825 42>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RT044,RT045		BLC_5V_SERIES:0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/16W,0402	RT044,RT045		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CT040,CT041		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CT040,CT041		BLC_5V_CAP:4P7_UF

KEYBOARD BKLT PWM LEVEL-SHIFTER



BEN IC VERSION 4 VS 6 DEPENDS ON WHICH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01615	1	IC,LP8548B1-04,DC/DC CVTR,BST,AISH,QFN-24	UT000		BLC_BEN_IC:V4
353S01685	1	IC,LP8548B1-06,DC/DC CVTR,BST,QFN24	UT000		BLC_BEN_IC:V6

ALTERNATE PART FOR BEN IC VERSION 4

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4160	353S01615	BLC_BEN_IC:V4	ALL	RECOMMENDED BY LOUISA

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,COG,12PF,5%,100V,0201	CT013		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BEN: KEYBD BKLT

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*** OK2PLACE ***

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0665	311S00405		ALL	RDAR://91779789

TO/FROM TRACKPAD

KEYBAORD IOX1

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

PP3V3_S2_HOLD_IPD — CT110 1.0UF 20% 6.3V X5R 0201-1 138S0692 — CT112 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

PP1V85_S2_HOLD_KBD — CT113 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 — CT114 10UF 20% 10V X5R-CERM 0402-7

IOX1 DOESN'T SEND THE INTERRUPT INSTEAD, IOX2 SENDS INT WHEN A KEY IS PRESSED

IOXP1_INT_L → INT*

IOXP1_RESET_L → CT111 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 → RESET*

UT101 TCAL6416 WQFN-COMBO

VCCI, VCCP

P00	KBD_DRIVE_Y0	OUT
P01	KBD_DRIVE_Y1	OUT
P02	KBD_DRIVE_Y2	OUT
P03	KBD_DRIVE_Y3	OUT
P04	KBD_DRIVE_Y4	OUT
P05	KBD_DRIVE_Y5	OUT
P06	KBD_DRIVE_Y6	OUT
P07	KBD_DRIVE_Y7	OUT
P10	KBD_DRIVE_Y8	OUT
P11	KBD_DRIVE_Y9	OUT
P12	KBD_DRIVE_Y10	OUT
P13	KBD_DRIVE_Y11	OUT
P14	NC	
P15	KBD_ID_DETECT2	
P16	KBD_LAYOUT_DETECT	
P17	CAPSLOCK_LED_EN	

311S0665
ALT:311S00405
WRITE: 0X40
READ: 0X41

ADD 4X NEW IO,Y8,Y9,Y10,Y11 FOR ALL 34-PIN KBD
CONNECT THE NEW IO FROM KBD ZIF CONN TO NEARBY ESD DIODES

GND, EPAD

I2C_KBD_SCL — RT110 33 1% 1/20W TK 0201 — IOXP_I2C_SCL (CKPLUS_WAIVE=I2C_PULLUP)
PLACE_NEAR=JT400.8:10MM
DZT110 5.5V-0.28PF 0201-THICKSTNCL

I2C_KBD_SDA — RT111 33 1% 1/20W TK 0201 — IOXP_I2C_SDA (CKPLUS_WAIVE=I2C_PULLUP)
PLACE_NEAR=JT400.9:10MM
DZT111 5.5V-0.28PF 0201-THICKSTNCL

KBD_INT_L — RT112 33 1% 1/20W TK 0201 — IOXP2_INT_L
PLACE_NEAR=JT400.9:10MM
DZT112 5.5V-0.28PF 0201-THICKSTNCL

KEYBAORD IOX2

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

PP3V3_S2_HOLD_IPD — RT121 100K 5% 1/20W TK 0201 — CT120 1.0UF 20% 6.3V X5R 0201-1 13BS0692 — CT121 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

PP1V85_S2_HOLD_KBD — CT122 0.1UF 10% 10V X5R-CERM 0201

IOXP2_ADDR

IOXP2_RESET_L → CT123 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UT102 TCAL6416 WQFN-COMBO

VCCI, VCCP

P00	KBD_SENSE_X0	IN
P01	KBD_SENSE_X1	IN
P02	KBD_SENSE_X2	IN
P03	KBD_SENSE_X3	IN
P04	KBD_SENSE_X4	IN
P05	KBD_SENSE_X5	IN
P06	KBD_SENSE_X6	IN
P07	KBD_SENSE_X7	IN
P10	KBD_SENSE_X8	IN
P11	KBD_SENSE_X9	IN
P12	KBD_SENSE_X10	IN
P13	KBD_SENSE_X11	IN
P14	KBD_SENSE_X12	IN
P15	KBD_CONTROL_L	
P16	KBD_LEFT_OPTION_L	
P17	KBD_RIGHT_SHIFT_L	

WRITE: 0X42
READ: 0X43

GND, EPAD

PP1V85_S2_HOLD_KBD
RT130 10K KBD_SENSE_X0
RT131 10K KBD_SENSE_X1
RT132 10K KBD_SENSE_X2
RT133 10K KBD_SENSE_X3
RT134 10K KBD_SENSE_X4
RT135 10K KBD_SENSE_X5
RT136 10K KBD_SENSE_X6
RT137 10K KBD_SENSE_X7
RT138 10K KBD_SENSE_X8
RT139 10K KBD_SENSE_X9
RT140 10K KBD_SENSE_X10
RT141 10K KBD_SENSE_X11
RT142 10K KBD_SENSE_X12
RT143 1K IOXP2_ADDR
(5% 1/20W TK 0201)

PP3V3_S2_HOLD_IPD
RT120 10K IOXP2_RESET_L
RT122 10K IOXP1_RESET_L
RT123 1.3K I2C_KBD_SCL
RT124 1.3K I2C_KBD_SDA
RT125 100K IOXP1_INT_L
(5% 1/20W TK 0201; 1% 1/20W TK 0201)

3V3 KBD CONN SERIES R

KBD DRI REQUEST, TO MEASURE CAPSLOCK LED CURRENT

PP3V3_AON — RT103 0 0% 1/20W TK 0201 — PP3V3_AON_KBD_CONN (TO KBD CONN AND ESD)
MIN_NECK_WIDTH=0.1500
MIN-LINE-WIDTH=0.2000
VOLTAGE=3.3V

ID_DETECT SERIES R

KBD_LAYOUT_DETECT — RT117 1K 5% 1/20W TK 0201-1 — KBD_ID1
KBD_ID 1 PIN ON KBD CONNECTOR
ANSI: NO CONNECT
ISO: TIED HIGH TO PP1V8
JIS: TIED LOW TO GND

KBD_ID_DETECT2 — RT119 1K 5% 1/20W TK 0201-1 — KBD_ID2
KBD_ID 2 PIN ON KBD CONNECTOR
TIED LOW TO GND FOR 34-PIN KBD

3.3V RSLOC ISOLATION KEYS/ASIC RESET

PP3V3_AON — CT150 1.0UF 20% 6.3V X5R 0201-1 138S0692 (PLACE_NEAR=UT103.10:5MM) — CT151 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 (PLACE_NEAR=UT103.10:2MM)

PP1V85_S2_HOLD_KBD — RT190 0 0% 1/20W TK 0201 (117S00073) → OUT123_EN

UT103 SLG4AP45306 QFN-THICKSTNCL 343S00532 (2.97 < VDD < 3.63)
IN_X: VIH_MIN 2.0V VIL_MAX 0.8V 100K IPD
OUT_X: VOH_MIN 2.4V VOL_MAX 0.4V 12.5K IPU OE

KBD_RIGHT_SHIFT_KEY	IN 1	OUT 1	KBD_RIGHT_SHIFT_L
KBD_LEFT_OPTION_KEY	IN 2	OUT 2	KBD_LEFT_OPTION_L
KBD_CONTROL_KEY	IN 3	OUT 3	KBD_CONTROL_L
OUT123_EN	OE 4	OUT_ALL* 6	RSLOC_RST_L → RT152 33 1% 1/20W TK 0201 → PMU_RSLOC_RST_L

GND, EPAD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00879	353S00754		UT108	RDAR://32477358

USE SAME POWER RAIL AS TPAD 3V3 LDO INPUT

PP3V8_IPDLDO_VIN — CT180 1.0UF 20% 6.3V X5R 0201-1 138S0692

LP5907SNX-1.825 X2SON-COMBO-THICKSTNCL UT108

IPD_PWR_EN → EN
VIN ← PP3V8_IPDLDO_VIN
VOUT → PP1V85_S2_HOLD_KBD — CT181 1.0UF 20% 6.3V X5R 0201-1 138S0692
GND EPAD

THE LDO OUTPUT SUPPLY POWER OF KBD IO EXPANDER IO PIN.
EVENTUALLY SHOUULD BE CONNECTED TO PP1V8_S2_KBD

CAPSLOCK LED DRIVER

CONSTANT CURRENT LED DRIVER

NOTE: THIS CAN BE THE SAME RAIL AS THE CAPSLOCK LED (3V3_AON), OR A RAIL THAT COMES UP AFTER (3V3_S2)

PP3V3_S2_HOLD_IPD — CT105 1.0UF 20% 6.3V X5R 0201-1 138S0692

UT105 FAN5622 SSOT23
VIH_MIN 1.2V VIL_MAX 0.4V

CAPSLOCK_LED_EN — RT161 1K 5% 1/20W TK 0201-1 — LED_CTRL
LED_ISET — RT162 200K 5% 1/20W TK 0201 (<R_SET>) — RT160 19.1K 1% 1/20W TK 0201
GND

LED1, LED2 → KBD_LED1 — RT118 1 1% 1/20W TK 0201 (R_SET 19.1K 15 MA SINK) — KBD_CAP_CATHODE

BOM_COST_GROUP=KEYBOARD

PAGE TITLE: KEYBOARD IOX, SUPPORT

Apple Inc.

DRAWING NUMBER: 051-08242 SIZE: D
REVISION: 4.0.0
BRANCH: dvt-2
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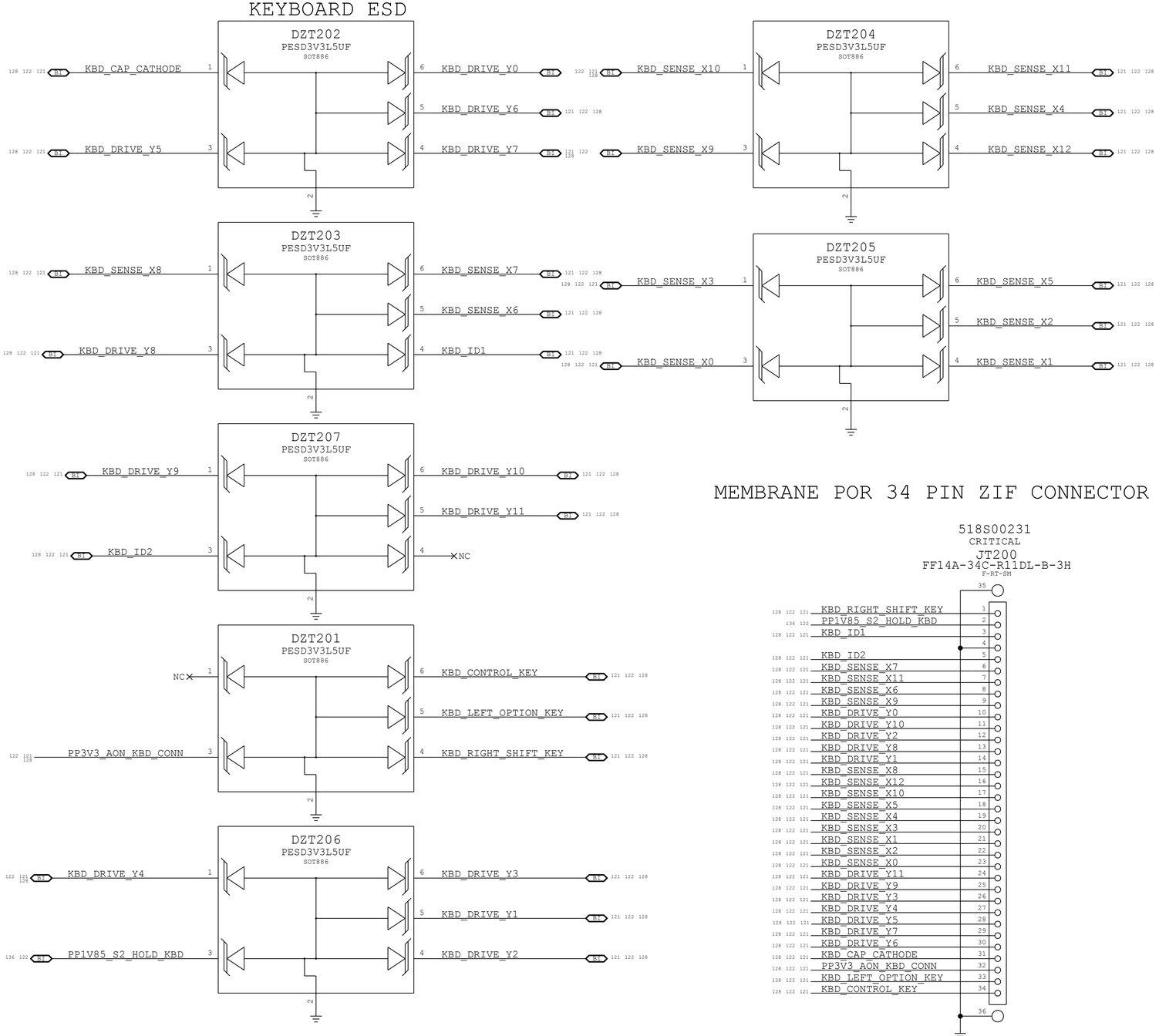
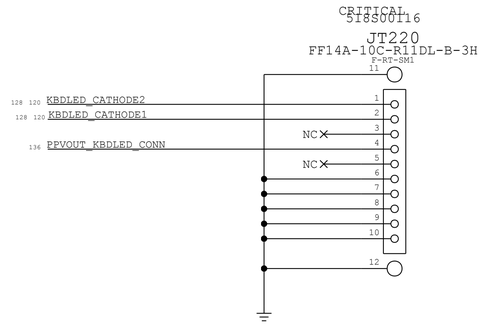
KEYBOARD ESD



MEMBRANE POR 34 PIN ZIF CONNECTOR

KBDLED Connector



BOM_COST_GROUP=KEYBOARD

PAGE TITLE
KEYBOARD SIGNAL CONNECTOR, ESD

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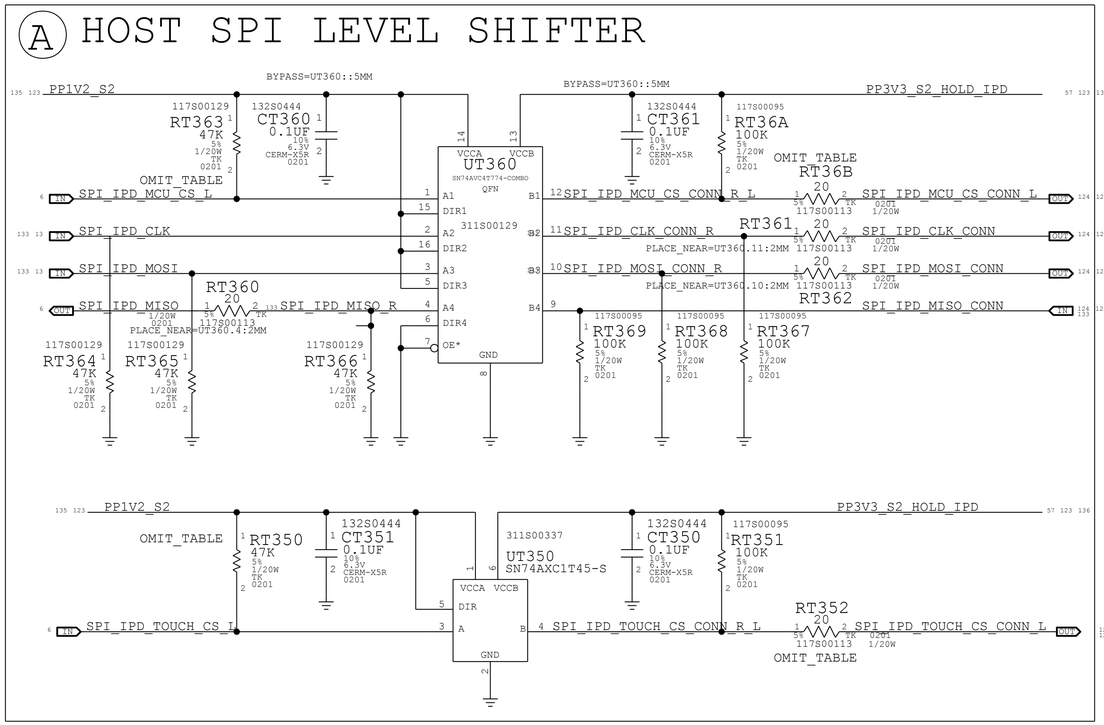

PAGE TITLE	TRACKPAD SUPPORT
	Apple Inc.
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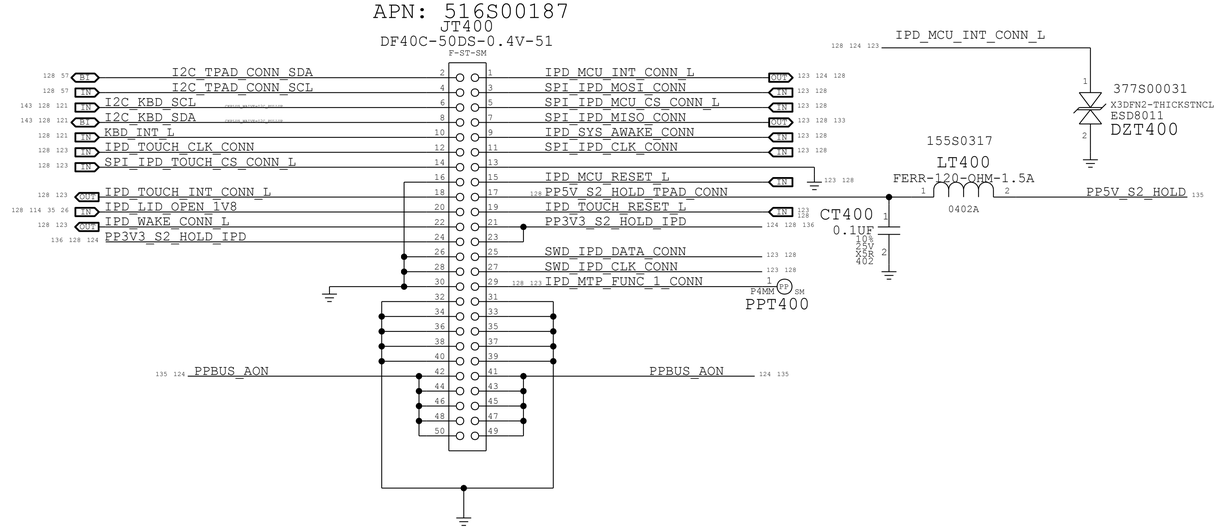
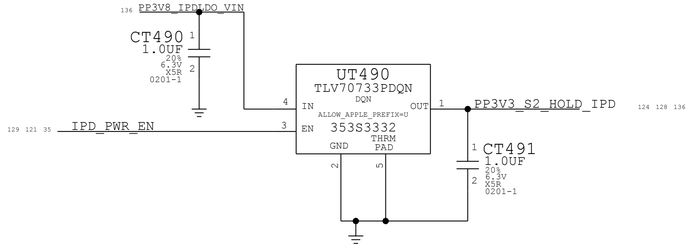
MATES WITH 518S00080
APN: 516S00187



3.3V LDO (LOCAL TO IPD)

Current Limit = 200mA



BOM_COST_GROUP=TRACKPAD

PAGE TITLE
TRACKPAD SUPPORT 2

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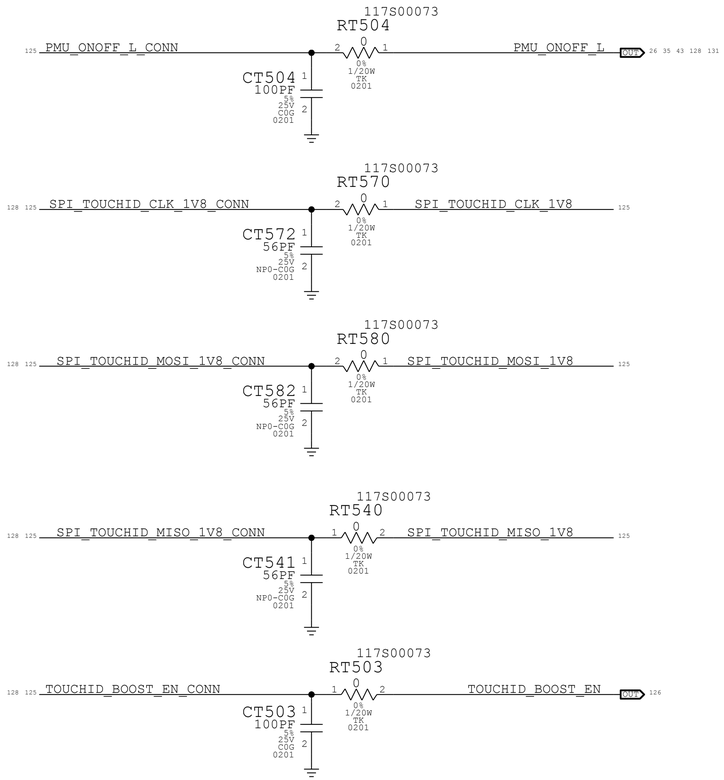

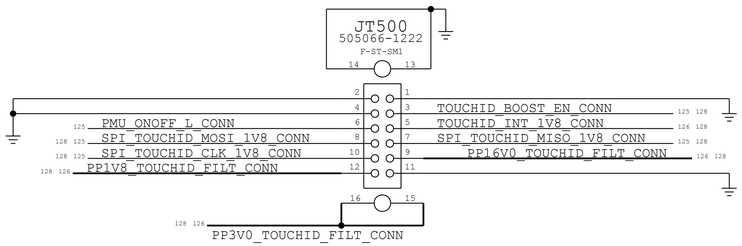

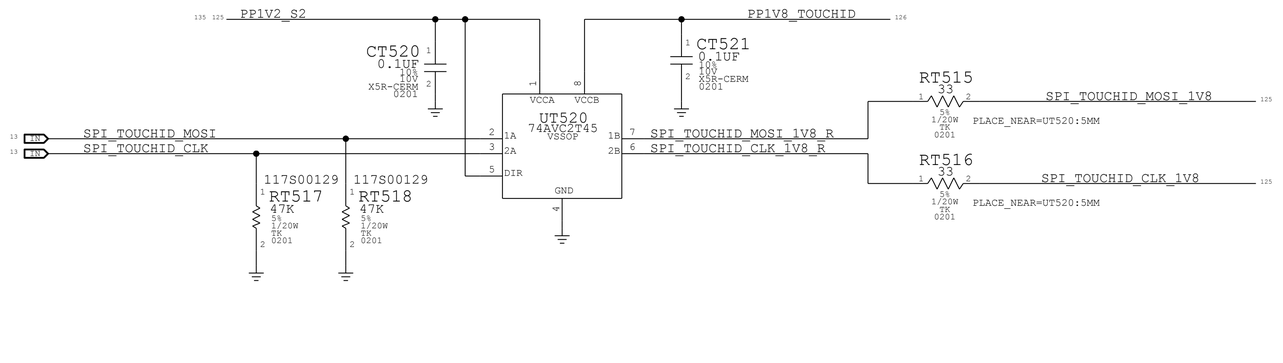

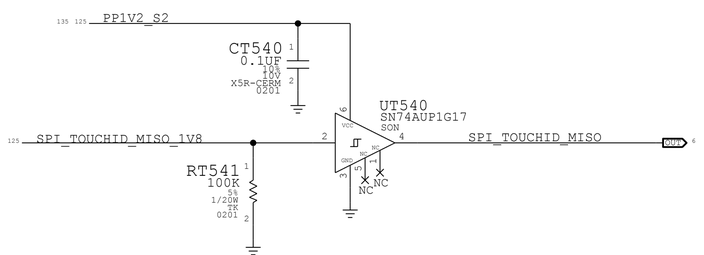

BOM_COST_GROUP=TOUCHID

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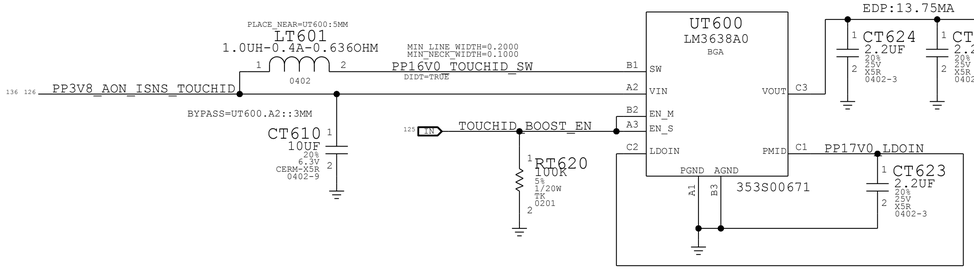
*** OK2INTEGRATE ***

TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0

16V BOOST



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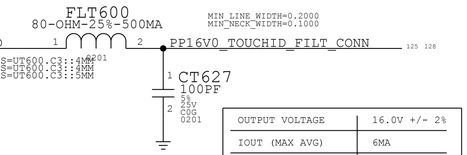
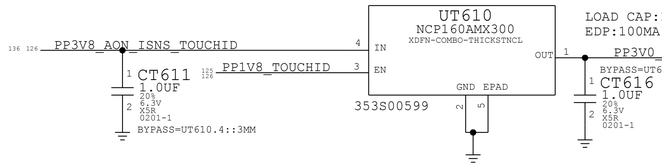


OUTPUT VOLTAGE	16.0V +/- 2%
IOUT (MAX AVG)	6MA
OCP (MIN)	13 MA
ACTIVE DISCHARGE	15 MA SINK
MAX OUTPUT CAP	0.5UF @ 16V

3.0V LDO



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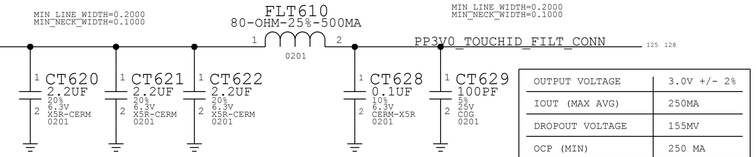
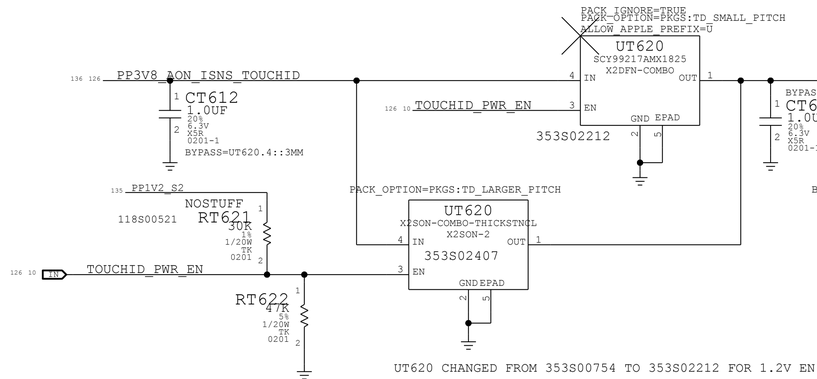
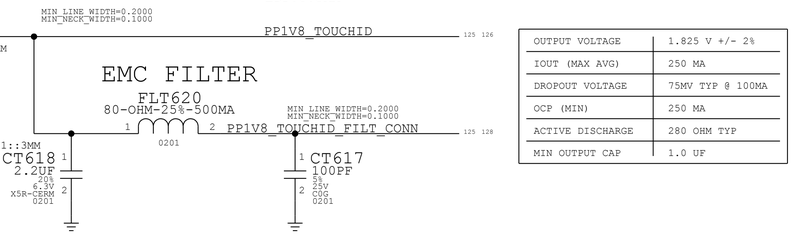


OUTPUT VOLTAGE	3.0V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	155MV
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP

1.8V LDO

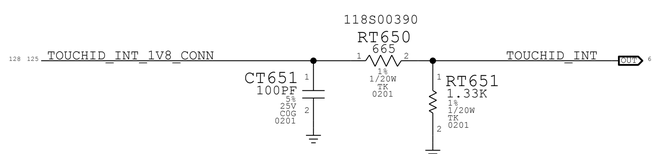


LOAD CAP:3.4UF NOM
EDP:0.5MA



OUTPUT VOLTAGE	1.825 V +/- 2%
IOUT (MAX AVG)	250 MA
DROPOUT VOLTAGE	75MV TYP @ 100MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MIN OUTPUT CAP	1.0 UF

UT620 CHANGED FROM 353S00754 TO 353S02212 FOR 1.2V EN SIGNAL SUPPORT.
N.B.: TOUCHID_PWR_EN REQUIRES 47K PULL-UP TO PP1V25_S2 AT THE SOC



BOM_COST_GROUP=TOUCHID

SYNC_MASTER=X2681_*
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NAND0 TEST POINTS

105 104 103 102 101 IN NAND0_LPB_L TOP TP TPU603 TP-P4
104 103 102 101 8 IN NAND_BFH TOP TP TPU604 TP-P4
104 103 102 101 IN NAND0_BOOT2 TOP TP TPU605 TP-P4
101 IN NAND0_S5E0_SWD_UID0 TOP TP TPU606 TP-P4
102 IN NAND0_S5E1_SWD_UID0 TOP TP TPU607 TP-P4
103 IN NAND0_S5E2_SWD_UID0 TOP TP TPU608 TP-P4
104 IN NAND0_S5E3_SWD_UID0 TOP TP TPU609 TP-P4
101 IN NAND0_S5E0_SWD_UID1 TOP TP TPU610 TP-P4
102 IN NAND0_S5E1_SWD_UID1 TOP TP TPU611 TP-P4
103 IN NAND0_S5E2_SWD_UID1 TOP TP TPU612 TP-P4
104 IN NAND0_S5E3_SWD_UID1 TOP TP TPU613 TP-P4
105 104 103 102 101 IN NAND0_PFN_L TOP TP TPU614 TP-P4
104 103 102 101 8 IN NAND0_PCIE_RESET_L TOP TP TPU615 TP-P4
12 IN SWD_NAND0_SWDIO TOP TP TPU616 TP-P4
12 IN SWD_NAND0_SWCLK TOP TP TPU617 TP-P4
104 103 102 101 IN NAND0_WP_L TOP TP TPU618 TP-P4
13 8 IN NAND0_CLKREQ0_L TOP TP TPU619 TP-P4
13 8 IN NAND0_CLKREQ1_L TOP TP TPU620 TP-P4
13 8 IN NAND0_CLKREQ2_L TOP TP TPU621 TP-P4
13 8 IN NAND0_CLKREQ3_L TOP TP TPU622 TP-P4
101 IN NAND0_S5E0_PCIE_RESREF TOP TP TPU623 TP-P4
102 IN NAND0_S5E1_PCIE_RESREF TOP TP TPU624 TP-P4
103 IN NAND0_S5E2_PCIE_RESREF TOP TP TPU625 TP-P4
104 IN NAND0_S5E3_PCIE_RESREF TOP TP TPU626 TP-P4
141 105 IN NAND0_RESET_L TOP TP TPU627 TP-P4

103 IN NAND0_S5E2_ZQ_0 TOP TP TPU632 TP-P4
103 IN NAND0_S5E2_ZQ_1 TOP TP TPU633 TP-P4

101 IN TP_NAND0_S5E0_JTAG_TDI TOP TP TPU668 TP-P4
104 IN TP_NAND0_S5E3_JTAG_TDO TOP TP TPU669 TP-P4
104 103 102 101 IN NAND0_JTAG_SEL TOP TP TPU670 TP-P4
104 103 102 101 IN NAND0_JTAG_TRST_L TOP TP TPU671 TP-P4
128 101 IN TP_NAND0_S5E0_ANI1_VREF TOP TP TPU672 TP-P4
128 101 IN TP_NAND0_S5E0_ANI0_VREF TOP TP TPU673 TP-P4
128 102 IN TP_NAND0_S5E1_ANI1_VREF TOP TP TPU674 TP-P4
128 102 IN TP_NAND0_S5E1_ANI0_VREF TOP TP TPU675 TP-P4

103 IN TP_NAND0_S5E2_ANI1_VREF TOP TP TPU676 TP-P4
103 IN TP_NAND0_S5E2_ANI0_VREF TOP TP TPU677 TP-P4
104 IN TP_NAND0_S5E3_ANI1_VREF TOP TP TPU678 TP-P4
104 IN TP_NAND0_S5E3_ANI0_VREF TOP TP TPU679 TP-P4

105 IN TP_NAND0_OCARINA_VEN2 TOP TP TPU600 TP-P4

TEST POINTS REQUESTED BY BY AUDIO TEAM

115 PP3V8_CODEC_VP TPU6B0 TP-P4
115 PP1V8_CODEC_VCP TPU6B1 TP-P4
115 10 CODEC_RESET_L TPU6B2 TP-P4
115 6 CODEC_INT_L TPU6B_3 TP-P4
115 13 TDM_CODEC_FSYNC TPU6B4 TP-P4
115 13 TDM_CODEC_R2D TPU6B5 TP-P4
PLACE_NEAR=U0600.D51:30MM
115 6 TDM_CODEC_D2R TPU6B6 TP-P4
115 13 TDM_CODEC_BCLK TPU6B7 TP-P4
115 56 I2C_CODEC_SDA TPU6B8 TP-P4
115 56 I2C_CODEC_SCL TPU6B9 TP-P4
117 116 6 SPKRAMP_RESET_L TPU6E0 TP-P4
117 116 6 SPKRAMP_INT_L TPU6E1 TP-P4
116 13 TDM_SPKRAMP_L_BCLK TPU6E2 TP-P4
116 13 TDM_SPKRAMP_L_FSYNC TPU6E3 TP-P4
116 13 TDM_SPKRAMP_L_R2D TPU6E4 TP-P4
PLACE_NEAR=U0600.P51:20MM
116 13 TDM_SPKRAMP_L_D2R TPU6E5 TP-P4
141 SPKRAMP_ICC TPU6E6 TP-P4
116 56 I2C_SPKRAMP_L_SCL TPU6E7 TP-P4
116 56 I2C_SPKRAMP_L_SDA TPU6E8 TP-P4
116 TP_SPKRAMP_A_LV_EN TPU6E9 TP-P4
116 TP_SPKRAMP_B_LV_EN TPU6F0 TP-P4
116 TP_SPKRAMP_C_LV_EN TPU6F1 TP-P4
117 13 TDM_SPKRAMP_R_BCLK TPU6F2 TP-P4
117 13 TDM_SPKRAMP_R_FSYNC TPU6F3 TP-P4
117 13 TDM_SPKRAMP_R_R2D TPU6F4 TP-P4
PLACE_NEAR=U0600.T51:20MM
117 13 TDM_SPKRAMP_R_D2R TPU6F5 TP-P4
117 56 I2C_SPKRAMP_R_SCL TPU6F6 TP-P4
117 56 I2C_SPKRAMP_R_SDA TPU6F7 TP-P4
117 TP_SPKRAMP_D_LV_EN TPU6F8 TP-P4
117 TP_SPKRAMP_E_LV_EN TPU6F9 TP-P4
117 TP_SPKRAMP_F_LV_EN TPU6A6 TP-P4

PLACE_SIDE=BOTTOM
128 127 74 6 UART_DEBUGPRT_D2R TPU6A4 TP-P4
PLACE_SIDE=BOTTOM
128 127 74 6 UART_DEBUGPRT_R2D TPU6A5 TP-P4

PLACE_SIDE=TOP
128 127 14 10 SMC_FIXTURE_MODE_L TPU6A0 TP-P4

TPU6A1
32 I2C_P3V8AON_SCL TP-P4
TPU6A2
32 I2C_P3V8AON_SDA TP-P4

119 10 PDM_DMIC_DATA0 TOP TP TP-P4 TPU6G8
PLACE_NEAR=U0600.AG13:20MM
119 10 PDM_DMIC_DATA1 TOP TP TP-P4 TPU6G9
PLACE_NEAR=U0600.BD11:20MM

PP3V42_G3H CODEC_WAKE_L TRUE 43 115

SoC Misc Debug TPs

5 IN TP_ANALOGMUX_POS TOP TP TPU6612 TP-P4
5 IN TP_ANALOGMUX_NEG TOP TP TPU6613 TP-P4
128 127 74 6 IN UART_DEBUGPRT_D2R BOTTOM TP TPU6614 TP-P4
128 127 74 6 IN UART_DEBUGPRT_R2D BOTTOM TP TPU6615 TP-P4
128 43 10 5 IN PMU_RESET_L BOTTOM TP TPU6616 TP-P4
141 128 5 IN SOC_FORCE_DFU BOTTOM TP TPU6617 TP-P4

140 130 128 43 5 IN PMU_ACTIVE_READY BOTTOM TP TPU6621 TP-P4
128 5 IN SOC_HOLD_RESET BOTTOM TP TPU6622 TP-P4
5 IN SOC_KIS_DFU_SELECT TOP TP TPU6623 TP-P4
5 IN SOC_DBG_PROBE_VALID BOTTOM TP TPU6624 TP-P4
35 10 IN PMU_CLK32K_SOC BOTTOM TP TPU6600 TP-P4
128 127 14 10 IN SMC_FIXTURE_MODE_L BOTTOM TP TPU6603 TP-P4

TPT_SOC_DOCK_ATTENTION
MAKE_BASE=TRUE
TPT_SOC_DOCK_ATTENTION 10
TOP TP TPU6601 TP-P4

TPT_TST_CLKOUT
MAKE_BASE=TRUE
TPT_TST_CLKOUT TRUE PPU6602
BOTTOM 1 PP SM P3MM

6 IN TP_SOC_MASTER_SYNC_GEN_7 TOP TP TPU6625 TP-P4

SoC JTAG TPs

10 IN SOC_JTAG_SEL PLACE_NEAR=UF400:20mm TP TPU6604 TP-P4
128 74 12 IN SWD_SOC_SWCLK PLACE_NEAR=UF400:20mm TP TPU6605 TP-P4
128 74 12 IN SWD_SOC_SWDIO PLACE_NEAR=UF400:20mm TP TPU6608 TP-P4
143 10 SOC_JTAG_TDI TP TPU6606 TP-P4
143 10 SOC_JTAG_TDO TP TPU6607 TP-P4

TPT_JTAG_SOC_TRST_L
MAKE_BASE=TRUE
10 TPT_JTAG_SOC_TRST_L TP TPU6609 TP-P4

121 KBD_RIGHT_SHIFT_L PLACE_NEAR=UT102.17:10MM PPU600 P4MM SM PP
121 KBD_LEFT_OPTION_L PLACE_NEAR=UT102.16:10MM PPU601 P4MM SM PP
121 KBD_CONTROL_L PLACE_NEAR=UT102.15:10MM PPU602 P4MM SM PP
GND PLACE_NEAR=UT101.9:10MM PPU603 P4MM SM PP
13 TDM_SPKRAMP_R_BCLK PPU604 P4MM SM PP
13 TDM_SPKRAMP_R_R2D PPU605 P4MM SM PP
13 TDM_SPKRAMP_R_FSYNC PPU606 P4MM SM PP

140 9 EUSB_ATC0_P PPU610 P4MM SM PP
PPU611 P2MM SM PP
140 9 EUSB_ATC0_N PPU612 P4MM SM PP
PPU613 P2MM SM PP
140 9 EUSB_ATC1_P PPU614 P4MM SM PP
PPU615 P2MM SM PP
140 9 EUSB_ATC1_N PPU616 P4MM SM PP
PPU617 P2MM SM PP
140 9 EUSB_ATC2_P PPU618 P4MM SM PP
PPU619 P4MM SM PP
140 9 EUSB_ATC2_N PPU620 P4MM SM PP
PPU621 P4MM SM PP

140 9 EUSB_DBG_N PPU624 P4MM SM PP
PPU625 P2MM SM PP
140 9 EUSB_DBG_P PPU622 P4MM SM PP
PPU623 P2MM SM PP

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DFU, Debug

		FUNC_TEST	
J1	USBC0_USB_TOP_P	TRUE	69 75
J2	USBC0_USB_TOP_N	TRUE	69 75
J3	USB2_ATC0_LS_P	TRUE	143
J4	USB2_ATC0_LS_N	TRUE	143
J5	USB_DBG_LS_N	TRUE	143
J6	USB_DBG_LS_P	TRUE	143
J7	SOC_FORCE_DFU	TRUE	5 127 141
J8	SOC_DFU_STATUS	TRUE	5 74 130
J9	SOC_FORCE_DFU_DBG	TRUE	131
J10	UART_DEBUGPRT_R2D	TRUE	6 74 127
J11	UART_DEBUGPRT_D2R	TRUE	6 74 127
J12	SWD_SOC_SWCLK	TRUE	12 74 127
J13	SWD_SOC_SWDIO	TRUE	12 74 127
J14	TP_SMC_UART0_R2D	TRUE	10
J15	TP_SMC_UART0_D2R	TRUE	10
J16	SMC_FIXTURE_MODE_L	TRUE	10 14 127

J17	PMU_SYS_ALIVE	TRUE	43 87 105 110 140
J18	PMU_ACTIVE_READY	TRUE	5 43 127 130 140
J19	PMU_ONOFF_L	TRUE	26 35 43 125 131
J20	PMU_RSLOC_RST_L	TRUE	35 43 121 131
J21	SOC_SOCHOT_L	TRUE	5 43
J22	PMU_RESET_L	TRUE	5 10 43 127
J23	PMU_SHDN	TRUE	35 43 131

Battery

135	J24 PPVBAT_AON	TOP 1 TP	TPU700 TP-P4
		TOP 1 TP	TPU701 TP-P4
		TOP 1 TP	TPU702 TP-P4
		TOP 1 TP	TPU703 TP-P4
		TOP 1 TP	TPU704 TP-P4
		TOP 1 TP	TPU705 TP-P4
		TOP 1 TP	TPU706 TP-P4
		TOP 1 TP	TPU707 TP-P4
		TOP 1 TP	TPU708 TP-P4
		TOP 1 TP	TPU709 TP-P4
		TOP 1 TP	TPU710 TP-P4 135 133 128
		TOP 1 TP	TPU711 TP-P4
		TOP 1 TP	TPU712 TP-P4
		TOP 1 TP	TPU713 TP-P4
		TOP 1 TP	TPU714 TP-P4
		TOP 1 TP	TPU715 TP-P4
		TOP 1 TP	TPU716 TP-P4

J25	SMBUS_BATT_SDA	TRUE	26 57
J26	SMBUS_BATT_SCL	TRUE	26 57
J27	SYS_DETECT_L	TRUE	26
J28	SYS_DETECT	TRUE	26 131
	GND TOP 1 TP		TPU717 TP-P4

Charger

135	J29 PPDCIN_AON	TOP 1 TP	TPU718 TP-P4
		TOP 1 TP	TPU719 TP-P4
		TOP 1 TP	TPU720 TP-P4
		TOP 1 TP	TPU721 TP-P4
		TOP 1 TP	TPU722 TP-P4
		TOP 1 TP	TPU723 TP-P4
		TOP 1 TP	TPU724 TP-P4
		TOP 1 TP	TPU725 TP-P4
		TOP 1 TP	TPU726 TP-P4
		TOP 1 TP	TPU727 TP-P4
		TOP 1 TP	TPU728 TP-P4

J30	PPDCIN_AON_CHGR_R	TRUE	27
J31	PPHV_INT5_AONSW	TRUE	31
30 29	J32 PPVBUS_USBC5	TOP 1 TP	TPU729 TP-P4
		TOP 1 TP	TPU730 TP-P4
		TOP 1 TP	TPU731 TP-P4
		TOP 1 TP	TPU732 TP-P4
		TOP 1 TP	TPU733 TP-P4
		TOP 1 TP	TPU734 TP-P4
		TOP 1 TP	TPU735 TP-P4
		TOP 1 TP	TPU736 TP-P4
		TOP 1 TP	TPU737 TP-P4
		TOP 1 TP	TPU738 TP-P4
		TOP 1 TP	TPU739 TP-P4
	GND TOP 1 TP		TPU740 TP-P4
		TOP 1 TP	TPU741 TP-P4
		TOP 1 TP	TPU742 TP-P4
		TOP 1 TP	TPU743 TP-P4
		TOP 1 TP	TPU744 TP-P4
		TOP 1 TP	TPU745 TP-P4
		TOP 1 TP	TPU746 TP-P4
		TOP 1 TP	TPU747 TP-P4
		TOP 1 TP	TPU748 TP-P4
		TOP 1 TP	TPU749 TP-P4
		TOP 1 TP	TPU750 TP-P4

Power rails

		FUNC_TEST	
135 55 46	J52 PPBUS_AON	TOP 1 TP	TPU751 TP-P4
		TOP 1 TP	TPU752 TP-P4
		TOP 1 TP	TPU753 TP-P4
		TOP 1 TP	TPU754 TP-P4
		TOP 1 TP	TPU755 TP-P4
		TOP 1 TP	TPU756 TP-P4
		TOP 1 TP	TPU757 TP-P4
		TOP 1 TP	TPU758 TP-P4
		TOP 1 TP	TPU759 TP-P4
		TOP 1 TP	TPU760 TP-P4
		TOP 1 TP	TPU761 TP-P4

J53	PP3V8_AON	TRUE	135
J54	PPVDD_DISP_S1	TRUE	138
J57	PP1V8_S2SW_VDD1	TRUE	130 133 138
J62	PPVDD_AMPH1_S2SW	TRUE	138
J63	PPVDD_AMPH0_S2SW	TRUE	138
J67	PPVDD_FIXED_S1	TRUE	138
J68	PPVDD_SOC_S1	TRUE	130 138
J70	PP1V8_S2	TRUE	128 135 138
J71	PP1V8_S2	TRUE	128 135 138
J72	PP1V2_S2	TRUE	89 135 138
J74	PP1V8_AON	TRUE	135 138
J75	PP1V2_AWAKE	TRUE	135 138
J76	PPVDD2H_S2SW	TRUE	138

ACE OTP

		FUNC_TEST	
J78	I2C_UPC01_3V3_SDA	TRUE	89 141
J79	I2C_UPC01_3V3_SCL	TRUE	89 141
J80	I2C_UPC2_3V3_SDA	TRUE	82 83 89
J81	I2C_UPC2_3V3_SCL	TRUE	82 83 89
J83	PP0V9_NAND0	TRUE	105
J84	PP1V2_NAND0	TRUE	105
J85	PP2V5_NAND0	TRUE	105

J92	PP5V_S2SW_USBC01	TRUE	136
J93	PP5V_S2SW_USBC23	TRUE	136
J94	PPMDB_AWAKESW_TCON	TRUE	135
J95	PP3V3_AON	TRUE	130 135 138
J96	PP3V3_S2	TRUE	130 135 138
J97	PP5V_S2_HOLD TOP 1 TP	TRUE	TPU762 TP-P4
	TOP 1 TP		TPU763 TP-P4
J98	PP3V3_UPC0_LDO	TRUE	73 74 75
J99	PP5V0_HDMI_DDC_CONN	TRUE	90 94
J100	PPVBAT_AON_CHGR_R	TRUE	27
J101	PPBUS_AON		135

J158	PPBUS_NAND0	TRUE	136
J159	PPVIN_P3V8NAND0	TRUE	136
J160	PP3V8_ATC01_LDO	TRUE	136
J161	PP3V8_AON_LPMU	TRUE	136

Fan

		FUNC_TEST	
J103	PP5V_S2_HOLD		128 133 135
	TOP 1 TP		TPU767 TP-P4
	TOP 1 TP		TPU768 TP-P4
	TOP 1 TP		TPU769 TP-P4
J102	FAN_0_PWM_5V	TRUE	68
J104	FAN_0_TACH	TRUE	68
J105	FAN_1_PWM_5V	TRUE	68
J106	FAN_1_TACH	TRUE	68
J107	I2C_FAN_L_SCL	TRUE	58 68
J108	I2C_FAN_L_SDA	TRUE	58 68
J109	I2C_FAN_R_SCL	TRUE	58 68
J110	I2C_FAN_R_SDA	TRUE	58 68
	GND TOP 1 TP		TPU773 TP-P4
	GND TOP 1 TP		TPU774 TP-P4
	GND TOP 1 TP		TPU775 TP-P4
	GND TOP 1 TP		TPU776 TP-P4

HDMI

		FUNC_TEST
J111	HDMI_CEC_CONN	TRUE 90
J112	HDMI_DDC_5V_CONN_SCL	TRUE 90
J113	HDMI_DDC_5V_CONN_SDA	TRUE 90
J114	HDMI_HPD_IN_CONN	TRUE 90
J115	HDMI_RSVD	TRUE 90

Mirabeau SWD

		FUNC_TEST

Misc

		FUNC_TEST	
J155	SOC_HOLD_RESET	TRUE	5 127
J156	SOC_DOCK_CONNECT	TRUE	10 134
J157	DFUMUX_SEL	TRUE	134
J524	RTMRMUX_OE_L	TRUE	134
J523	ATCRTMR0_RESET_1V2_1V8_MCW	TRUE	143
	GND TOP 1 TP		TPU7G6 TP-P4

USB-C

		FUNC_TEST	
J312	PPVBUS_USBC0		69 75
	TOP 1 TP		TPU778 TP-P4
	TOP 1 TP		TPU779 TP-P4
	TOP 1 TP		TPU781 TP-P4
	TOP 1 TP		TPU783 TP-P4
J313	USBC0_SBU1	TRUE	69 75
J314	USBC0_SBU2	TRUE	69 75
J680	USBC0_CC1	TRUE	69 74 75
J690	USBC0_CC2	TRUE	69 74 75
J605	USBC5_CC1	TRUE	29 30
J317	USBC0_LDCM	TRUE	69 75
	TOP 1 TP		TPU782 TP-P4
J697	USBC0_LDCM_LB	TRUE	69 74 75
	TOP 1 TP		TPU780 TP-P4
	GND TOP 1 TP		TPU784 TP-P4
J319	PPVBUS_USBC1		69 76
	TOP 1 TP		TPU785 TP-P4
	TOP 1 TP		TPU786 TP-P4
	TOP 1 TP		TPU787 TP-P4
	TOP 1 TP		TPU788 TP-P4
	TOP 1 TP		TPU789 TP-P4
	TOP 1 TP		TPU790 TP-P4
J691	USBC1_CC1	TRUE	69 74 76
J692	USBC1_CC2	TRUE	69 74 76
J322	USBC1_SBU1	TRUE	69 76
J323	USBC1_SBU2	TRUE	69 76
J324	USBC1_LDCM	TRUE	69 76
J696	USBC1_LDCM_LB	TRUE	69 74 76
	GND TOP 1 TP		TPU791 TP-P4
J326	PPVBUS_USBC2		70 84
	TOP 1 TP		TPU792 TP-P4
	TOP 1 TP		TPU793 TP-P4
	TOP 1 TP		TPU794 TP-P4
	TOP 1 TP		TPU795 TP-P4
	TOP 1 TP		TPU796 TP-P4
	TOP 1 TP		TPU797 TP-P4
J693	USBC2_CC1	TRUE	70 83 84
J694	USBC2_CC2	TRUE	70 83 84
J329	USBC2_SBU1	TRUE	70 84
J330	USBC2_SBU2	TRUE	70 84
J331	USBC2_LDCM	TRUE	70 84
J695	USBC2_LDCM_LB	TRUE	70 83 84
	GND TOP 1 TP		TPU798 TP-P4

SSD

		FUNC_TEST	
J133	TP_NAND0_S5E0_ANT0_VREF	TRUE	101 127
J134	TP_NAND0_S5E0_ANT1_VREF	TRUE	101 127
J135	TP_NAND0_S5E1_ANT0_VREF	TRUE	102 127
J136	TP_NAND0_S5E1_ANT1_VREF	TRUE	102 127

Camera

		FUNC_TEST	
J141	PP5V_S2_CAMERA	TRUE	136
J142	I2C_CAM_1V8_SDA	TRUE	58 108
J143	I2C_ALS_1V8_SDA	TRUE	58 108
J144	I2C_CAM_1V8_SCL	TRUE	58 108
J145	I2C_ALS_1V8_SCL	TRUE	58 108
J146	FTCAM_ENABLE_1V8_OUT	TRUE	107 141
J147	ALS_INT_L	TRUE	10 108
	GND TOP 1 TP		TPU799 TP-P4
J301	LPDP_FTCAM_DATA_C_P<0>	TRUE	108
J302	LPDP_FTCAM_DATA_C_N<0>	TRUE	108

Display

		FUNC_TEST	
J149	PP3V8_AWAKESW_TCON	TRUE	136
J150	I2C_SMC_SNS0_SCL_1V8	TRUE	57
J151	I2C_SMC_SNS0_SDA_1V8	TRUE	57
J152	UART_TCON_D2R_1V8	TRUE	109
J153	EDP_PANEL_1V8_EN	TRUE	109 110
J154	LPDP_INT_HPD	TRUE	7 109 139 141
J155	SPI_TCON_CS_L	TRUE	13 109
J156	SPI_TCON_MISO	TRUE	6 109
J157	SPI_TCON_MOSI	TRUE	13 109
J158	SPI_TCON_CLK	TRUE	13 109
J631	LPDP_INT_AUX_P	TRUE	109
J632	LPDP_INT_AUX_N	TRUE	109
	GND TOP 1 TP		TPU7A0 TP-P4

BCON

		FUNC_TEST	
J160	I2C_DISP_BKLT_SCL_1V8	TRUE	56 112
J161	I2C_DISP_BKLT_SDA_1V8	TRUE	56 112
J162	BL_PMIC_PWR_EN	TRUE	35 112
J163	PPVOUT_LUXE	TRUE	111 112 128
	TOP 1 TP		TPU7A1 TP-P4
	TOP 1 TP		TPU7A2 TP-P4
	TOP 1 TP		TPU7A3 TP-P4
	TOP 1 TP		TPU7A4 TP-P4
	TOP 1 TP		TPU7A5 TP-P4
	TOP 1 TP		TPU7A6 TP-P4
J164	PP1V2_AWAKESW_BLC	TRUE	135
J165	PPRCON_AWAKESW_BKLTCONN	TRUE	136
J166	DISP_BKLT_LSYNC	TRUE	7 112
J167	BKLT_BOOST_THROTTLE_CONN_L	TRUE	112
J168	DISP_BKLT_FSYNC	TRUE	7 112

J169	SPI_DISP_BKLT_CS_L	TRUE	7 112
J170	SPI_DISP_BKLT_MISO	TRUE	7 112 129
J171	SPI_DISP_BKLT_CLK	TRUE	13 112
	GND TOP 1 TP		TP807 TP-P4

AMR

		FUNC_TEST	
J172	MGL_1V8	TRUE	113 114
J173	SPI_LAS_CS_1V8_L	TRUE	14 113
J174	SPI_AOP_LAS_CLK_1V8	TRUE	14 113
J175	SPI_AOP_LAS_MISO_1V8_R	TRUE	113
J176	SPI_AOP_LAS_MOSI_1V8	TRUE	14 113
	GND TOP 1 TP		TPU7A8 TP-P4

Audio Jack

		FUNC_TEST	
J177	AUD_CONN_HP_LEFT	TRUE	119
J178	AUD_CONN_SLEEVE	TRUE	119
J179	AUD_CONN_HP_RIGHT	TRUE	119
J180	AUD_CONN_RING2	TRUE	119
J181	AUD_CONN_TIP_SENSE	TRUE	119
J182	AUD_CONN_HP_SENSE_L	TRUE	119
J183	AUD_CONN_RING2_XW	TRUE	119
J184	AUD_CONN_RING_SENSE	TRUE	119
J185	AUD_CONN_HP_SENSE_R	TRUE	119
J186	AUD_CONN_SLEEVE_XW	TRUE	119
	GND TOP 1 TP		TPU7A9 TP-P4

Touch ID

		FUNC_TEST	
J187	PP1V8_TOUCHID_FILT_CONN	TRUE	125 126
J188	SPI_TOUCHID_MISO_1V8_CONN	TRUE	125
J189	SPI_TOUCHID_MOSI_1V8_CONN	TRUE	125
J190	TOUCHID_INT_1V8_CONN	TRUE	125 126
J191	SPI_TOUCHID_CLK_1V8_CONN	TRUE	125
J192	TOUCHID_BOOST_EN_CONN	TRUE	125
J193	PP16V0_TOUCHID_FILT_CONN	TRUE	125 126
J194	PP3V0_TOUCHID_FILT_CONN	TRUE	125 126
	TOP 1 TP		TPU7B0 TP-P4
	TOP 1 TP		TPU7B1 TP-P4
	TOP 1 TP		TPU7B2 TP-P4
	GND TOP 1 TP		TPU7B3 TP-P4

Digital mic

PLACE_NEAR=JR940:20MM

119	J200 PDM_DMIC_CLK5_1V8	TOP 1 TP	TPU7G5 TP-P4
	J201 PDM_DMIC_DATA0_1V8	TRUE	119
	J202 PP1V8_DMIC	TRUE	119
	J203 PDM_DMIC_CLK6_1V8	TRUE	119
	J204 PDM_DMIC_DATA1_1V8	TRUE	119
	GND TOP 1 TP		TPU7B4 TP-P4

Audio speaker amp

		FUNC_TEST	
J205	SPKRAMP_A_OUTP		116 118
	TOP 1 TP		TPU7B5 TP-P4
	TOP 1 TP		TPU7B6 TP-P4
	TOP 1 TP		TPU7B7 TP-P4
J207	SPKRAMP_A_OUTN		116 118
	TOP 1 TP		TPU7B8 TP-P4
	TOP 1 TP		TPU7B9 TP-P4
	TOP 1 TP		TPU7C0 TP-P4
J208	SPKRAMP_B_OUTP		116 118
	TOP 1 TP		TPU7C1 TP-P4
	TOP 1 TP		TPU7C2 TP-P4
	TOP 1 TP		TPU7C3 TP-P4
J209	SPKRAMP_B_OUTN		116 118
	TOP 1 TP		TPU7C4 TP-P4
	TOP 1 TP		TPU7C5 TP-P4
	TOP 1 TP		TPU7C6 TP-P4
J210	SPKRAMP_C_OUTP		116 118
	TOP 1 TP		TPU7C7 TP-P4
	TOP 1 TP		TPU7C8 TP-P4
	TOP 1 TP		TPU7G4 TP-P4
J211	SPKRAMP_C_OUTN		116 118
	TOP 1 TP		TPU7C9 TP-P4
	TOP 1 TP		TPU7D0 TP-P4
	TOP 1 TP		TPU7D1 TP-P4
J214	SPKR_ID0	TRUE	6 118
	GND TOP 1 TP		TPU7D2 TP-P4
	GND TOP 1 TP		TPU7D3 TP-P4
	GND TOP 1 TP		TPU7D4 TP-P4
	GND TOP 1 TP		TPU7D5 TP-P4
J215	SPKRAMP_D_OUTP		117 118
	TOP 1 TP		TPU7D6 TP-P4
	TOP 1 TP		TPU7D7 TP-P4
	TOP 1 TP		TPU7D8 TP-P4
J216	SPKRAMP_D_OUTN		117 118
	TOP 1 TP		TPU7D9 TP-P4
	TOP 1 TP		TPU7E0 TP-P4
	TOP 1 TP		TPU7E1 TP-P4
J217	SPKRAMP_E_OUTP		117 118
	TOP 1 TP		TPU7E2 TP-P4
	TOP 1 TP		TPU7E3 TP-P4
	TOP 1 TP		TPU7E4 TP-P4
J220	SPKRAMP_E_OUTN		117 118
	TOP 1 TP		TPU7E5 TP-P4
	TOP 1 TP		TPU7E6 TP-P4
	TOP 1 TP		TPU7E7 TP-P4

J221	SPKRAMP_F_OUTP		117 118
	TOP 1 TP		TPU7E8 TP-P4
	TOP 1 TP		TPU7E9 TP-P4
	TOP 1 TP		TPU7F0 TP-P4
J222	SPKRAMP_F_OUTN		117 118
	TOP 1 TP		TPU7F1 TP-P4
	TOP 1 TP		TPU7F2 TP-P4
	TOP 1 TP		TPU7F3 TP-P4
J223	SPKR_ID1	TRUE	6 118
	GND TOP 1 TP		TPU7F4 TP-P4
	GND TOP 1 TP		TPU7F5 TP-P4
	GND TOP 1 TP		TPU7F6 TP-P4

Keyboard

		FUNC_TEST	
J224	KBD_ID1	TRUE	121 122
J225	KBD_DRIVE_Y8	TRUE	121 122
J226	KBD_DRIVE_Y2	TRUE	121 122
J227	KBD_DRIVE_Y1	TRUE	121 122
J228	KBD_DRIVE_Y3	TRUE	121 122
J229	KBD_DRIVE_Y4	TRUE	121 122
J230	KBD_SENSE_X0	TRUE	121 122
J231	KBD_SENSE_X1	TRUE	121 122
J232	KBD_SENSE_X2	TRUE	121 122
J233	KBD_SENSE_X5	TRUE	121 122
J234	KBD_SENSE_X3	TRUE	121 122
J235	KBD_SENSE_X9	TRUE	121 122
J236	KBD_SENSE_X12	TRUE	121 122
J237	KBD_SENSE_X4	TRUE	121 122
J238	KBD_SENSE_X11	TRUE	121 122
J239	KBD_SENSE_X10	TRUE	121 122
J240	KBD_SENSE_X6	TRUE	121 122
J241	KBD_SENSE_X7	TRUE	121 122
J242	KBD_SENSE_X8	TRUE	121 122
J243	KBD_DRIVE_Y5	TRUE	121 122
J244	KBD_DRIVE_Y7	TRUE	121 122
J245	KBD_DRIVE_Y6	TRUE	121 122
J246	KBD_DRIVE_Y0	TRUE	121 122
J247	KBD_DRIVE_Y9	TRUE	121 122
J248	KBD_DRIVE_Y10	TRUE	121 122
J249	KBD_DRIVE_Y11	TRUE	121 122
J250	KBD_ID2	TRUE	121 122
J251	KBD_CAP_CATHODE	TRUE	121 122
J252	PP3V3_AON_KBD_CONN	TRUE	121 122
J253	KBD_RIGHT_SHIFT_KEY	TRUE	121 122
J254	KBD_LEFT_OPTION_KEY	TRUE	121 122
J255	KBD_CONTROL_KEY	TRUE	121 122
	GND TOP 1 TP		TPU7F7 TP-P4
J256	PPVOUT_KBDLED_CONN	TRUE	136
J257	KBDLED_CATHODE1	TRUE	120 122
J258	KBDLED_CATHODE2	TRUE	120 122
	GND TOP 1 TP		TPU7F8 TP-P4
	GND TOP 1 TP		TPU7F9 TP-P4

Trackpad

		FUNC_TEST	
J259	IPD_LID_OPEN_1V8	TRUE	26 35 114 124
J260	I2C_TPAD_CONN_SCL	TRUE	57 124
J261	I2C_TPAD_CONN_SDA	TRUE	57 124
J262	IPD_WAKE_CONN_L	TRUE	123 124
J263	KBD_INT_L	TRUE	121 124
J264	I2C_KBD_SDA	TRUE	121 124 143
J265	I2C_KBD_SCL	TRUE	121 124 143
	GND TOP 1 TP		TPU7G0 TP-P4
J266	IPD_TOUCH_CLK_CONN	TRUE	123 124
J267	SPI_IPD_TOUCH_CS_CONN_L	TRUE	123 124
J268	SPI_IPD_MISO_CONN	TRUE	123 124 133
J269	SPI_IPD_MOSI_CONN	TRUE	123 124
J270	SPI_IPD_MCU_CS_CONN_L	TRUE	123 124
J271	IPD_TOUCH_INT_CONN_L	TRUE	123 124
J272	IPD_MCU_INT_CONN_L	TRUE	123 124
J273	IPD_SYS_AWAKE_CONN	TRUE	123 124
J274	SPI_IPD_CLK_CONN	TRUE	123 124
J275	IPD_MCU_RESET_L	TRUE	123 124
J276	IPD_TOUCH_RESET_L	TRUE	123 124
J277	SWD_IPD_DATA_CONN	TRUE	123 124
J278	SWD_IPD_CLK_CONN	TRUE	123 124
J279	IPD_MTP_FUNC_1_CONN	TRUE	123 124
J280	PP3V3_S2_HOLD_IPD	TRUE	124 136
J281	PP5V_S2_HOLD_TPAD_CONN	TRUE	124

Card Reader

		FUNC_TEST	
J289	SDCONN_CMD_R_FL	TRUE	96
J290	PP3V3_GL_SDCONN	TRUE	95 96
J291	SDCONN_WP_R	TRUE	96
J292	SDCONN_DETECT_R	TRUE	96
J293	PP1V8_GL_SDCONN	TRUE	95 96
	GND TOP 1 TP		TPU7G1 TP-P4

LUXE

		FUNC_TEST	
J294	I2C_LUXE_DEBUG_SCL	TRUE	56 111
J295	I2C_LUXE_DEBUG_SDA	TRUE	56 111
J296	LUXE_VPROG_TEST	TRUE	111
J297	PPBUS_AON_LUXE	TRUE	136
J298	PPLUXE_INPUT_R_V	TRUE	111 128 133
J299	PPVOUT_LUXE	TRUE	111 112 128
J300	PPLUXE_LX1	TRUE	111 133
J301	PPLUXE_LX2	TRUE	111 133
J302	LUXE_UG1	TRUE	111
J303	LUXE_LG1	TRUE	111
J304	LUXE_UG2	TRUE	111
J305	LUXE_LG2	TRUE	111
J306	BL_PWR_EN	TRUE	35 111
J308	BKLT_BOOST_THROTTLE_LUXE_L	TRUE	111
J309	PVOUT_LUXE_R	TRUE	111
J310	PPLUXE_INPUT_R_V	TRUE	111 128 133
J311	LUXE_AGND	TRUE	111
	GND TOP 1 TP		TPU7G2 TP-P4

KBD Backlight

		FUNC_TEST	
J312	KBDBKLT_SW2	TRUE	120 133
J313	KBDBKLT_FB2	TRUE	120
J314	KBDLED_KEYB1	TRUE	120
J315	KBDLED_KEYB2	TRUE	120
J316	KBD_BKLT_PWM_3V3	TRUE	120
J317	KBDBKLT_TSET_KEYB	TRUE	120
	GND TOP 1 TP		TPU7G3 TP-P4

NAND

		FUNC_TEST	
J641	P2V5_NAND0_PGOOD	TRUE	105
J642	P2V5_NAND0_EN	TRUE	105
J555	TP_NAND0_OCARINA_VCC_DET	TRUE	105
J550	TP_NAND0_S5E0_DROOP_L	TRUE	101
J553	TP_NAND0_S5E0_VPP	TRUE	101
J554	TP_NAND0_S5E1_DROOP_L	TRUE	102
J552	TP_NAND0_S5E1_VPP	TRUE	102
J556	TP_NAND0_S5E2_DROOP_L	TRUE	103
J551	TP_NAND0_S5E2_VPP	TRUE	103
J555	TP_NAND0_S5E3_DROOP_L	TRUE	104
J547	TP_NAND0_S5E3_VPP	TRUE	104

SMC ISENSE

		FUNC_TEST	
66 60	J644 LPMU_3V8_ISENSE	PLACE_NEAR=CD601.1:3MM TOP 1 TP	TPU7H0 TP-P4
	GND	PLACE_NEAR=CD601.2:3MM TOP 1 TP	TPU7H1 TP-P4
66 60	J645 FPMU_3V8_ISENSE	PLACE_NEAR=CD631.1:3MM TOP 1 TP	TPU7H2 TP-P4
	GND	PLACE_NEAR=CD631.2:3MM TOP 1 TP	TPU7H3 TP-P4
66 59	J670 BMON_ISENSE	PLACE_NEAR=CD580.1:3MM TOP 1 TP	TPU7H6 TP-P4
	GND	PLACE_NEAR=CD580.2:3MM TOP 1 TP	TPU7H7 TP-P4

PAGE TITLE: FCT 2

Apple Inc.

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SPMU/MPMU PPs HAVE MOVED TO PROJECT CSAs

USBC Debug 3mm PPs

PPU8C7
P3MM SM PP 1 PPHV_INT0_AONSW 73

PPU8C0
P3MM SM PP 1 PPHV_INT1_AONSW 73

PPU8C6
P3MM SM PP 1 PPHV_INT2_AONSW 82

USB2 DEBUG PPs

PPU800
P3MM SM PP 1 TPT_MACAW0_DEBUG_SWDCLK 77 141

PPU801
P3MM SM PP 1 TPT_MACAW0_DEBUG_SWDDAT 77 141

PPU802
P3MM SM PP 1 TPT_MACAW1_DEBUG_SWDCLK 77 141

PPU803
P3MM SM PP 1 TPT_MACAW1_DEBUG_SWDDAT 77 141

PPU804
P3MM SM PP 1 TPT_MACAW2_DEBUG_SWDCLK 85 141

PPU805
P3MM SM PP 1 TPT_MACAW2_DEBUG_SWDDAT 85 141

SoC TP Nets

6 TP_AP_GPIO37 BOTTOM TP TPU880 TP-P4
6 TP_AP_GPIO38 BOTTOM TP TPU881 TP-P4

6 TP_AP_I2C0_SCL BOTTOM TP TPU870 TP-P4
6 TP_AP_I2C0_SDA BOTTOM TP TPU871 TP-P4
6 TP_AP_I2C05_SCL BOTTOM TP TPU883 TP-P4
6 TP_AP_I2C05_SDA BOTTOM TP TPU884 TP-P4
6 TP_MTP_I2C0_SCL BOTTOM TP TPU885 TP-P4
6 TP_MTP_I2C0_SDA BOTTOM TP TPU886 TP-P4

6 TP_MTR_FUNC2 BOTTOM TP TPU888 TP-P4
6 TP_MTR_FUNC6 BOTTOM TP TPU889 TP-P4
6 TP_MTR_FUNC7 BOTTOM TP TPU890 TP-P4
10 TP_AOP_SCM_IO0 BOTTOM TP TPU891 TP-P4
10 TP_AOP_SCM_IO1 BOTTOM TP TPU892 TP-P4
10 TP_AOP_I2S1_LRCK BOTTOM TP TPU893 TP-P4
10 TP_AON_SLEEP1_RESET_L BOTTOM TP TPU894 TP-P4
10 TP_AOP_LEAP_MADI_IN BOTTOM TP TPU895 TP-P4
10 TP_AOP_LEAP_MADI_OUT BOTTOM TP TPU896 TP-P4
10 TP_NUB_GPIO7 BOTTOM TP TPU897 TP-P4

EKARA PPs

PPU830
P3MM SM PP 1 TPT_AP_UART2_R2D 6 142

PPU831
P3MM SM PP 1 TPT_AP_UART2_D2R 6 142

PPU832
P3MM SM PP 1 TPT_AP_UART2_R2D_RTS_L 6 142

PPU833
P3MM SM PP 1 TPT_AP_UART2_D2R_CTS_L 6 142

Power Sequencing PPs

PPU8A5
P3MM SM PP 1 DBL_CLICK_DET 6 43

PPU8A6
P3MM SM PP 1 P5VS2HOLD_PWR_EN 35 43

TP-P4 TPU8A7 TP 1 P5VS2HOLD_PWR_EN 35 94 141

PPU8A8
P3MM SM PP 1 P5VS2HOLD_PGOOD 34 141

PPU8B0
P3MM SM PP 1 IPD_PWR_EN 35 121 124

PPU8B2
P3MM SM PP 1 FPMU_CRASH0_L 35 39

PPU8B6
P3MM SM PP 1 P3V8AON_LPM 32 35

PPU8B7
P3MM SM PP 1 P3V8AON_PWR_EN 26 28 32

TP-P4 TPU8B8 TP 1 CHGR_AUX_OK 26 27 35

PPU8B9
P3MM SM PP 1 FPMU_CRASH1_L 35 39

PPU8C1
P3MM SM PP 1 GPUVR_SCRASH_L 35 138

PPU8C2
P3MM SM PP 1 PCPUVR_SCRASH_L 35 129 138

PPU8C4
P3MM SM PP 1 EDP_BKLT_1V29_EN 35 110

PPU8C5
P3MM SM PP 1 UPC_PMU_RESET_1V2 43 131 134 141

PPU851
P3MM SM PP 1 PCPUVR_SCRASH_L 35 129 138

SI PP

PPU8E1 PLACE_SIDE=BOTTOM PLACE_NEAR=U0600.AU51:17MM
P3MM SM PP 1 SPI_DISP_BKLT_MISO 7 112 128

PMU Serial PPs for characterization

Other PMU serial nets are accessible to probe within 50mm of their RX, on their series R pads or test vias

removed 05/16/2022

NO TESTs

PPVDD_PCPU_AWAKE 46 63 137

PPVDD_FIXED_S1_DCS_0 20
PPVDD_FIXED_S1_DCS_2 20
PPVDD_FIXED_S1_DDR_0 20
PPVDD_FIXED_S1_DDR_2 20
PP1V2_S2_AOP_S2 21

PPVDD_PCPU_SRAM_AWAKE 46 63 137

PP1V2_S2_ULPPLL 21

PPVDD_LOW_S2_ULPPLL 16
PPVDD_LOW_S2_FLPPLL 16

PPVDD_FABRIC_S1 138

PP1V2_AWAKE_GRP0 21
PPVDD_GPU_AWAKESW 46 63 137
PP1V2_AWAKE_GRP1 21
PP1V2_AWAKE_FMON 21
PPVDD_FIXED_S1_DCS_1 20
PPVDD_FIXED_S1_DDR_1 20

PCIE_WLBT_R2D_P 99
PCIE_WLBT_R2D_N 99
PCIE_WLBT_D2R_C_P 99
PCIE_WLBT_D2R_C_N 99

PAGE TITLE
PMU AND OTHER TEST POINTS

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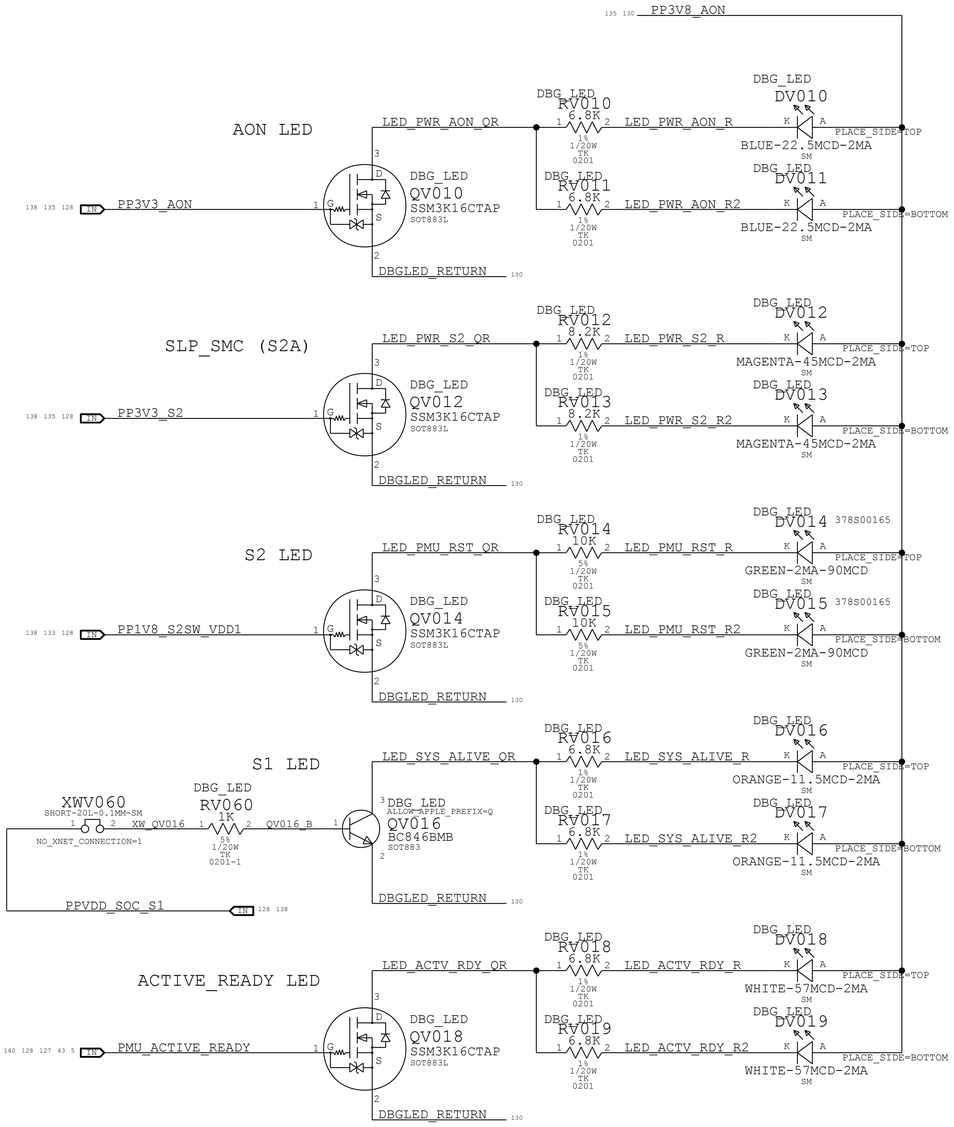
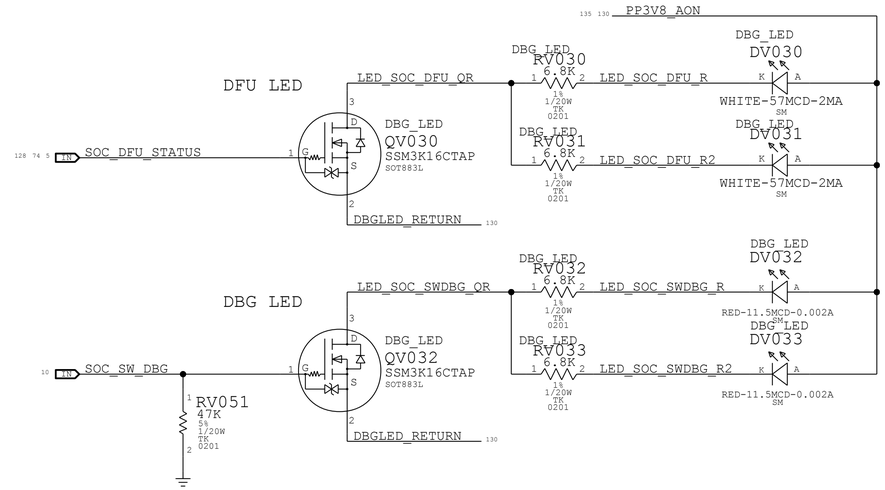
Debug LEDs



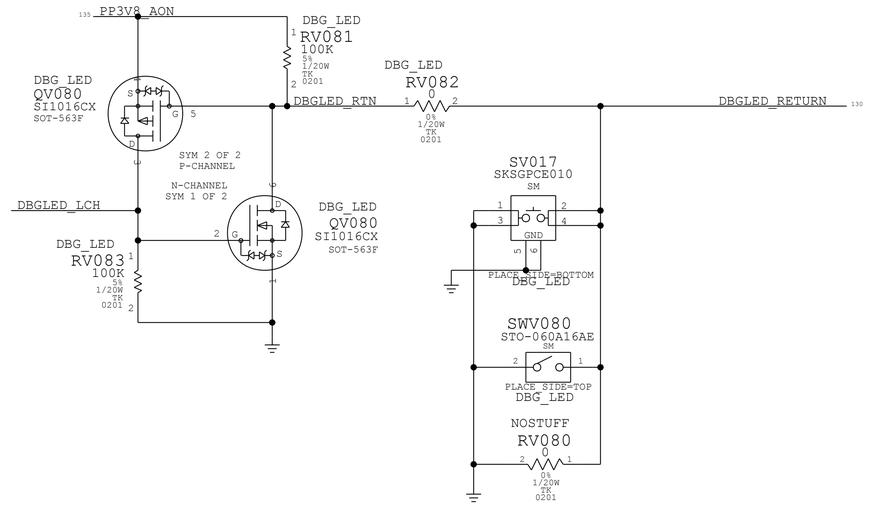


Debug LED Latch

Press button once to engage.

Remove power to disengage.

Debug LED Enable



BOM_COST_GROUP=DEBUG

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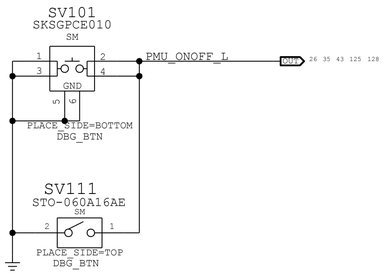
POWER BUTTON

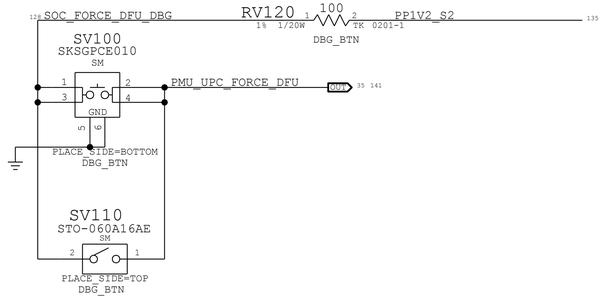
Imitate a user-facing Power Button press, many functions:

- Press to Wake from any state
- Combine with RSLOC (see RSLOC)
- Hold for 8sec to trigger "one-finger reset"
- - Similar to PMU RESET, except SW gets a warning to initiate panic-flow



FORCE DFU

Hold during OFF->AWAKE transition to enter SOC's "Debug Firmware Update" mode

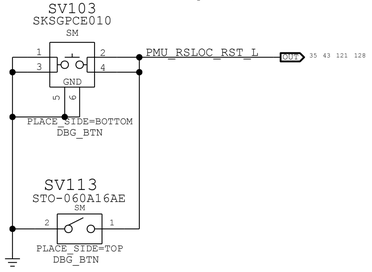


RSLOC BUTTON

Imitate a user-facing key combo Right-Shift + Left-Option + Control:

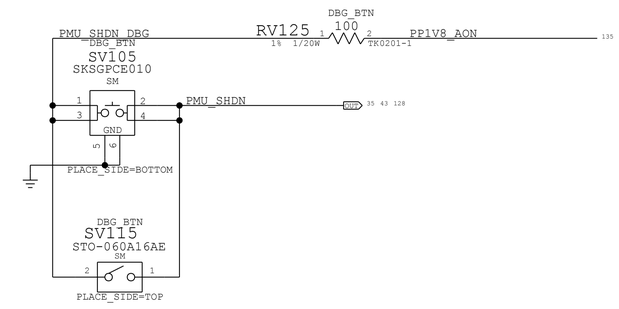
- Hold RSLOC 4sec, then press Power Button to initiate PMU RESET
- Hold RSLOC 4sec, then hold Power Button 4sec to power-cycle P3V8AON VR
- Hold Power Button 1sec

Then hold RSLOC 10sec (a PMU RESET will trigger at some point)
Then release RSLOC, and continue holding Power Button for at least 6 secs
(Board will boot to DFU during the final 6 sec hold)



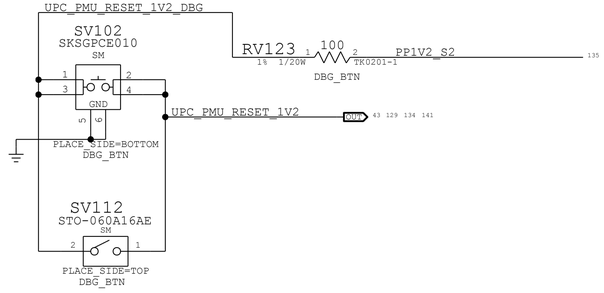
PMU SHUTDOWN

PMU transitions to OFF state and stays there while this is asserted, then waits for a WAKE source* to boot



PMU RESET

PMU transitions to OFF and automatically proceeds up to AWAKE

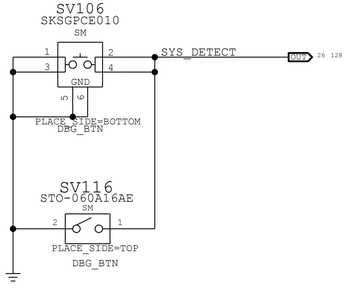


SYS_DETECT (Battery Disconnect)

Imitate unplugging the battery signal flex, to disconnect MLB from Battery power

- Disconnect all DCIN sources, then hold SYS_DETECT for 30sec*. MLB will completely power down

*Time depends on 3V8AON and PBUS decay rate, and should be quantified in system



*WAKE sources in OFF:
CHGR_AUX_OK (DCIN present)
IPD_LID_OPEN_1V8 (Lid is open)
PMU_ONOFF_L (User Power Button)

BOM_COST_GROUP=DEBUG

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rdar://102436359 (s MLB Add 5x dummy parts for underfill mitigation)

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV301
20
5%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV302
20
5%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV303
20
5%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV304
20
5%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV305
20
5%
1/20W
TK
0201

rdar://111071887 (DVT2: Change PMU VPP & CFG pack options to :GND option)

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV330
20
5%
1/20W
TK
0201

NAND ASSEMBLY PROTECTION PURPOSES

CKPLUS_WAIVE=TERMSHORTED
RV3012
0
0%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
RV3013
0
0%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
RV3017
0
0%
1/20W
TK
0201

CKPLUS_WAIVE=TERMSHORTED
RV3018
0
0%
1/20W
TK
0201

FOR ASSEMBLY PROTECTION PURPOSES ONLY

CKPLUS_WAIVE=TERMSHORTED
RV300
10K
1%
1/16W
TK
0402

rdar://103272673

CKPLUS_WAIVE=TERMSHORTED
117S00113
RV320
20
5%
1/20W
TK
0201

BOM_COST_GROUP=DEBUG

PAGE TITLE
SUPPORT

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Temp desense caps

PPBUS_AON_LUXE
- CW120 12PF 25V NP0-C0G 5% 0201
- CW121 12PF 25V NP0-C0G 5% 0201
- CW122 12PF 25V NP0-C0G 5% 0201
- CW124 1.8PF 25V C0G +/-0.1PF 201
- CW125 1.8PF 25V C0G +/-0.1PF 201
- CW126 12PF 25V NP0-C0G 5% 0201
- CW127 3.0PF 25V NP0-C0G +/-0.1PF 0201

PPLUXE_LX1
- OMIT
- CW123 12PF 25V NP0-C0G 5% 0201

PPVOUT_LUXE_XW
- CW110 12PF 25V NP0-C0G 5% 0201
- CW111 12PF 25V NP0-C0G 5% 0201
- CW117 12PF 25V NP0-C0G 5% 0201
- CW113 1.8PF 25V C0G +/-0.1PF 201
- CW115 12PF 25V NP0-C0G 5% 0201
- CW118 3.0PF 25V NP0-C0G +/-0.1PF 0201

PPLUXE_LX1
- OMIT
- CW112 12PF 25V NP0-C0G 5% 0201

PPLUXE_LX2
- OMIT
- CW114 12PF 25V NP0-C0G 5% 0201

PPLUXE_INPUT_R_V
- CW116 12PF 25V NP0-C0G 5% 0201
- CW119 1.8PF 25V C0G +/-0.1PF 201
- CW128 3.0PF 25V NP0-C0G +/-0.1PF 0201

PP3V8_AON_WLBT
- CW1A2 1.8PF 25V C0G +/-0.1PF 201
- CW1A3 1.8PF 25V C0G +/-0.1PF 201
- CW1A4 1.8PF 25V C0G +/-0.1PF 201
- CW1A5 1.8PF 25V C0G +/-0.1PF 201

PP1V8_S2
- CW1A6 1.8PF 25V C0G +/-0.1PF 201
- CW1A7 1.8PF 25V C0G +/-0.1PF 201

PPVIN_P3V8AON
- CW150 12PF 25V NP0-C0G 5% 0201
- CW151 12PF 25V NP0-C0G 5% 0201
- CW152 12PF 25V NP0-C0G 5% 0201
- CW153 12PF 25V NP0-C0G 5% 0201
- CW154 12PF 25V NP0-C0G 5% 0201
- CW155 12PF 25V NP0-C0G 5% 0201
- CW156 12PF 25V NP0-C0G 5% 0201
- CW157 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW158 1.8PF 25V C0G +/-0.1PF 201
- CW159 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW140 1.8PF 25V C0G +/-0.1PF 201

PP3V8_AON
- CW144 1.8PF 25V C0G +/-0.1PF 201
- CW145 12PF 25V NP0-C0G 5% 0201
- CW146 12PF 25V NP0-C0G 5% 0201
- CW147 12PF 25V NP0-C0G 5% 0201
- CW148 1.8PF 25V C0G +/-0.1PF 201
- CW149 12PF 25V NP0-C0G 5% 0201
- CW143 3.0PF 25V NP0-C0G +/-0.1PF 0201

P3V8AON_VSW1
- CW160 12PF 25V NP0-C0G 5% 0201

P3V8AON_SW2
- CW161 12PF 25V NP0-C0G 5% 0201

P3V8AON_SW3
- CW162 12PF 25V NP0-C0G 5% 0201

PPVIN_P5VS2
- CW180 12PF 25V NP0-C0G 5% 0201
- CW181 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW184 1.8PF 25V C0G +/-0.1PF 201

PP5V_S2_HOLD
- CW182 12PF 25V NP0-C0G 5% 0201
- CW183 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW185 1.8PF 25V C0G +/-0.1PF 201

PPBUS_NAND0
- CW131 12PF 25V NP0-C0G 5% 0201
- CW132 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW133 1.8PF 25V C0G +/-0.1PF 201

KBDBKLT_SW2
- NOSTUFF CW134 1.8PF 100V C0G +/-0.1PF 0201

PP1V2_S2
- CW190 1.8PF 25V C0G +/-0.1PF 201
- CW191 12PF 25V NP0-C0G 5% 0201
- CW192 3.0PF 25V NP0-C0G +/-0.1PF 0201

PPVDD_CIO_S2SW
- CW193 1.8PF 25V C0G +/-0.1PF 201
- CW194 12PF 25V NP0-C0G 5% 0201
- CW195 3.0PF 25V NP0-C0G +/-0.1PF 0201

PPVDD_SRAM_S1
- 131S0198
- CW196 1.8PF 25V C0G +/-0.1PF 201
- CW197 12PF 25V NP0-C0G 5% 0201
- CW198 3.0PF 25V NP0-C0G +/-0.1PF 0201

rdar://92307078
[X2681 add Desense caps to SPI_TPAD

SPI_IPD_MOSI_CONN_R
- 131S0445 CW135 12PF 25V NP0-C0G 5% 0201

SPI_IPD_MISO_CONN
- 131S0445 CW136 12PF 25V NP0-C0G 5% 0201

SPI_IPD_CLK_CONN_R
- 131S0445 CW137 12PF 25V NP0-C0G 5% 0201

SPI_IPD_CLK
- NOSTUFF 131S0445 CW163 12PF 25V NP0-C0G 5% 0201

SPI_IPD_MOSI
- NOSTUFF 131S0445 CW164 12PF 25V NP0-C0G 5% 0201

SPI_IPD_MISO_R
- NOSTUFF 131S0445 CW165 12PF 25V NP0-C0G 5% 0201

ICEMAN DESENSE rdar://102614479

ICEMAN PHASE2

P3V8AON_DRVL2_R
- 131S0445 CW138 12PF 25V NP0-C0G 5% 0201

P3V8AON_DRVL2_R
- 131S0445 CW13A 12PF 25V NP0-C0G 5% 0201

ICEMAN PHASE3

P3V8AON_DRVL3_R
- 131S0445 CW13C 12PF 25V NP0-C0G 5% 0201

P3V8AON_DRVL3_R
- 131S0445 CW13D 12PF 25V NP0-C0G 5% 0201

ICEMAN PHASE1 GATE DRIVER desense caps

PP1V8_S2SW_VDD1
- CW166 1.8PF 25V C0G +/-0.1PF 201
- CW167 3.0PF 25V NP0-C0G +/-0.1PF 0201
- CW168 12PF 25V NP0-C0G 5% 0201

P3V8AON_DRVL1_R
- CW171 12PF 100V CERM 2% 0201

P3V8AON_DRVH1_R
- NOSTUFF CW172 12PF 100V CERM 2% 0201 P3V8AON_SW1

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SOC USB DFU MUX

117S00098
PACK_OPTION=VITAMINC

135 PP3V3_AON

20K LIMITS USB MINI-B
FROM BACK POWERING MLB

VITAMIN-C:YES
RX412
20K
5% 1/20W TK 0201

PACK_OPTION=VITAMINC
VITAMIN-C:YES
BYPASS=UX410::5MM
CX410 1
0.1UF 10% 10V X5R-CERM 0201 2

PP3V3_AON_DFUMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.1500
MIN_NECK_WIDTH=0.1500

2UA MAX IDD

117S00095
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX410
100K
5% 1/20W TK 0201

VIT-C CONN

134 USB2_ATC0_VITC_CONN_P
134 USB2_ATC0_VITC_CONN_N

143 134 BI USB2_ATC0_LS_P
143 134 BI USB2_ATC0_LS_N

DEBUG SPI ACE

PACK_OPTION=VITAMINC
5363S4037
UX410
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES

VCC 9
M+ 5
M- 4
D+ 7
D- 6
OE* 8
GND 3
Y+ 1
Y- 2
SEL 10

LVL SHFTR

BI 134 143 USB2_ATC0_LS_MUX_P
BI 134 143 USB2_ATC0_LS_MUX_N

DFUMUX_SEL 128 134

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

PACK_OPTION=VITAMINC
VITAMIN-C:NO
RX414
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1

143 134 USB2_ATC0_LS_P — USB2_ATC0_LS_MUX_P 134 143

VITAMIN-C:NO
RX416
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1
PACK_OPTION=VITAMINC

143 134 USB2_ATC0_LS_N — USB2_ATC0_LS_MUX_N 134 143

SOC DBG MUX

117S00098
PACK_OPTION=VITAMINC

135 134 PP3V3_AON

20K LIMITS USB MINI-B
FROM BACK POWERING MLB

VITAMIN-C:YES
RX413
20K
5% 1/20W TK 0201

PACK_OPTION=VITAMINC
VITAMIN-C:YES
BYPASS=UX411::5MM
CX411 1
0.1UF 10% 10V X5R-CERM 0201 2

PP3V3_AON_DBGMUX_VC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

2UA MAX IDD

117S00095
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX411
100K
5% 1/20W TK 0201

VIT-C CONN

134 USB_DBG_VITC_CONN_P
134 USB_DBG_VITC_CONN_N

134 BI USB_DBG_LS_P
134 BI USB_DBG_LS_N

DEBUG SPI ACE

PACK_OPTION=VITAMINC
UX411
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES

VCC 9
M+ 5
M- 4
D+ 7
D- 6
OE* 8
GND 3
Y+ 1
Y- 2
SEL 10

LVL SHFTR(MACAW)

BI 134 143 USB_DBG_LS_MUX_P
BI 134 143 USB_DBG_LS_MUX_N

KISMUX_SEL 134

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

PACK_OPTION=VITAMINC
VITAMIN-C:NO
RX415
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1

143 134 USB_DBG_LS_P — USB_DBG_LS_MUX_P 134 143

VITAMIN-C:NO
RX417
0
0% 1/20W TK 0201
NO_XNET_CONNECTION=1
PACK_OPTION=VITAMINC

143 134 USB_DBG_LS_N — USB_DBG_LS_MUX_N 134 143

MACAW DBG MUX

USING PI3USB102 FOR SINGLE ENDED CONTROL SIGNAL: <RDAR://72709253>

135 134 PP3V3_AON

20K LIMITS USB MINI-B
FROM BACK POWERING MLB

117S00098
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX418
20K
5% 1/20W TK 0201

PACK_OPTION=VITAMINC
VITAMIN-C:YES
BYPASS=UX412::10MM
CX415 1
0.1UF 10% 10V X5R-CERM 0201 2

PP3V3_AON_DBGMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000

2UA MAX IDD

(1V2 IF DRIVEN BY MLB, 1V8 BY VITAMIN C)
<RDAR://75096896> J404: 1.8V ON PARROT RESET W/ VIOSEL=GND

VIT-C CONN

134 VITC_RTMR_RESET_1V8_L
141 134 TPT_VITC_RTMR_PWR_EN

134 75 73 71 IN ATCRTMR0_RESET_L
141 NC_USBC0_3V3LDO_EN

SEL	OUTPUT
L	VIT-C (M)
H	TYPE-C (D)

VCC 9
M+ 5
M- 4
D+ 7
D- 6
OE* 8
GND 3
Y+ 1
Y- 2
SEL 10

353S4037
UX412
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
VITAMIN-C:YES

ATCRTMR0_RESET_1V2_1V8_MCW_L OUT 77 134 143
TP_USB0_3V3_LDO_EN_VITC 141

DFUMUX_SEL 128 134

117S00098
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX422
20K
5% 1/20W TK 0201

128 RTMRMUX_OE_L
PACK_OPTION=VITAMINC
PACK_OPTION=VITAMINC

VITAMIN-C:NO
RX420
0
0201 0% 1/20W TK

134 75 73 71 ATCRTMR0_RESET_L — ATCRTMR0_RESET_1V2_1V8_MCW_L 143

NO_XNET_CONNECTION=1
PACK_OPTION=VITAMINC

VITAMIC-C MK2 CONNECTOR

PACK_OPTION=VITAMINC
516S00116
SILK_PART=VITAMIN-C
VITAMIN-C:YES
JX401
AA27D-S038VA1
F-ST-SM

SOC ATC0 DFU

134 USB2_ATC0_VITC_CONN_P
134 USB2_ATC0_VITC_CONN_N
134 USB_DBG_VITC_CONN_P
134 USB_DBG_VITC_CONN_N

SOC KIS DBG

RFU
RFU
RFU

VITC_RESET_L
DFUMUX_SEL 128 134
KISMUX_SEL 134
SOC_DOCK_CONNECT_VITAMINC 134
NC_DC_MUX_SEL 143
SWD_SOC_SWDIO BI 74 75
SWD_SOC_SWCLK OUT 74 75
SOC_JTAG_TDO IN 143
SOC_JTAG_TDI OUT 143
UART_DEBUGPRT_R2D IN 74 75
UART_DEBUGPRT_D2R OUT 74 75
VITC_RTMR_RESET_1V8_L 134
TPT_VITC_RTMR_PWR_EN 134 141
PP1V8_S2 135
PP1V2_S2 134 135

KOBA
SOC UART
SMC UART

PACK_OPTION=VITAMINC
NOSTUFF
RX402
1/20W TK 0% 0 0201

135 PP3V3_S2

PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX403
1/20W TK 0% 0 0201

135 134 PP1V2_S2

VOLTAGE=1.2V
PP1V2_S2_VITAMINC_Q
117S00095
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX430
100K
5% 1/20W TK 0201

VITAMIN-C:YES
PACK_OPTION=VITAMINC
QX400
DMP2160UWQ
SOT323

UPC_PMU_RESET_1V2
SWD_SOC_SWDIOT
SWD_SOC_SWCLK
JTAG_SOC_TDO
JTAG_SOC_TDI
IN 41 129 131 141

135 PP3V8_AON

VITAMIN-C:YES CX405 1
0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=JX401::10MM
PACK_OPTION=VITAMINC

VITAMIN-C:YES CX406 1
0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=JX401::10MM
PACK_OPTION=VITAMINC

PP5V_S2_HOLD 135
VITAMIN-C:YES
CX404 1
2.2UF 20% 25V X6S-CERM 0402 2
BYPASS=JX401::5MM
PACK_OPTION=VITAMINC

VITAMIN-C:YES CX401 1
0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=JX401::5MM
PACK_OPTION=VITAMINC

VITAMIN-C:YES CX402 1
0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=JX401::5MM
PACK_OPTION=VITAMINC

VITAMIN-C:YES CX403 1
0.1UF 10% 16V X5R-CERM 0201 2
BYPASS=JX401::5MM
PACK_OPTION=VITAMINC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-27266	998-23347	VITAMIN-C:YES	QX400	<RDAR://82683097>

TO SOC
1V2 NUB AOP, S2
47K PD ON SOC PAGE
128 10 OUT SOC_DOCK_CONNECT

117S00092
PACK_OPTION=VITAMINC
RX491
100
5% 1/20W TK 0201
1V2 S2
SOC_DOCK_CONNECT_UPC IN 89

VITAMIN-C:YES
RX492
10
5% 1/20W TK 0201
FROM VITAMIN C
GPIO 7, 1V2 S2
SOC_DOCK_CONNECT_VITAMINC 134

BOM_COST_GROUP=DEBUG

SYNC_MASTER=N2406* SYNC_DATE=10/06/2022

PAGE TITLE
DEBUG: VITAMIN-C

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VBAT

PPVBAT_AON — MAKE_BASE=TRUE → PPVBAT_AON 128
PPVBAT_AON → PPVBAT_AON 26 27

DCIN

73 PPDCIN_AON — MAKE_BASE=TRUE → PPDCIN_AON 128
82 PPDCIN_AON → PPDCIN_AON 59
31 PPDCIN_AON → PPDCIN_AON 26 27 28

PBUS

27 PPBUS_AON — MAKE_BASE=TRUE → PPBUS_AON 46 55 128

PPBUS_AON: 128, 59, 60, 60, 60, 41, 61, 61, 59, 61, 61, 124, 34, 52, 49, 59

ICEMAN VMAIN

133 33 PP3V8_AON — MAKE_BASE=TRUE → PP3V8_AON 128

PP3V8_AON: 60, 60, 62, 62, 62, 48, 115, 116, 116, 116, 117, 117, 117, 61 <---, 34 64, 63, 94 <---, 110, 63, 26, 130, 134, 130, 54, 80, 88, 94, 47, 51 135, 79, 48, 51 135, 50

PP5V_S2

54 PP5V_S2_HOLD — MIN_LINE_WIDTH=0.1500, MAKE_BASE=TRUE → PP5V_S2_HOLD 128 133

PP5V_S2_HOLD: 32, 47 48, 50 51, 28, 111, 124, 63, 68, 93, 120, 120, 134, 136, 34, 49, 52, 54, 27

94 PP5V_S2_HDMI — VOLTAGE=5V, MAKE_BASE=TRUE → PP5V_S2_HDMI 90 94

PP1V2 AWAKE

138 128 PP1V2_AWAKE — MAKE_BASE=TRUE → PP1V2_AWAKE 109 <=T724
PP1V2_AWAKE

PP1V2_AWAKE: 58, 97, 111, 115, 115 116, 116 117, 56, 97

PP1V2 S2

138 128 89 PP1V2_S2 — MAKE_BASE=TRUE → PP1V2_S2 28

PP1V2_S2: 30 31, 56 57 58, 77, 77, 85, 131, 99, 126, 134, 107 114, 119, 120, 48, 125, 93, 131, 67, 115, 14, 123, 89, 89

PP1V2_S2
PP1V2_S2
PP1V2_S2
79 78 76 75 73 72 71 PP1V2_S2
84 82 81 PP1V2_S2
94 PP1V2_S2
25 PP1V2_S2
PP1V2_S2
PP1V2_S2
47 PP1V2_S2
50 PP1V2_S2

1V8 S2 SYSTEM LOADS

138 128 PP1V8_S2 — MAKE_BASE=TRUE → PP1V8_S2 37

PP1V8_S2: 28, 77, 77, 75 76 79, 85, 58, 105, 109, 109, 119, 119, 67, 56 57, 87, 37, 107, 14, 99 133, 134, 25, 84

S2 SYSTEM LOADS

138 130 128 PP3V3_S2 — MAKE_BASE=TRUE → PP3V3_S2 97

PP3V3_S2: 78, 75 76 78 79, 120, 93, 77, 30, 134, 86, 84, 77, 77, 85

3V3 AON SYSTEM LOADS

138 130 128 PP3V3_AON — MAKE_BASE=TRUE → PP3V3_AON 121

PP3V3_AON: 113, 26, 134, 134, 134

PP5V_AON_P3V8AON

ICEMAN INTERNAL LDO

PP1V8_AON

138 128 PP1V8_AON — MAKE_BASE=TRUE → PP1V8_AON 28

PP1V8_AON: 113, 131, 35, 14, 114, 93 94, 123, 26, 123

PP1V8 AWAKE

138 PP1V8_AWAKE — MAKE_BASE=TRUE → PP1V8_AWAKE 115

PP1V8_AWAKE: 116 117, 58

PP1V2 LPMU LDO3 AWAKE SYSTEM LOADS

37 PP1V2_AWAKESW_BLC → PP1V2_AWAKESW_BLC — MAKE_BASE=TRUE 128
LPMU_LDO3
PP1V2_AWAKESW_BLC 112

PP1V8 LPMU SW0 S2 SYSTEM LOADS

37 PP1V8_S2SW_SNS → PP1V8_S2SW_SNS — MAKE_BASE=TRUE
LPMU_SW0
PP1V8_S2SW_SNS 59 60 61 62 63

DISPLAY POWER SEQUENCER OUTPUT

116 PPBCON_AWAKESW_BKLTCONN_VIN → PPBCON_AWAKESW_BKLTCONN_VIN — MAKE_BASE=TRUE
PPBCON_AWAKESW_BKLTCONN_VIN 63

110 PPMDB_AWAKESW_TCON → PPMDB_AWAKESW_TCON — MAKE_BASE=TRUE 128
PPMDB_AWAKESW_TCON 62

DEAD BATTERY SAK POWER

26 PP1V8_AON_LPMU → PP1V8_AON_LPMU — MAKE_BASE=TRUE 41 43

PAGE TITLE: POWER ALIASES 1

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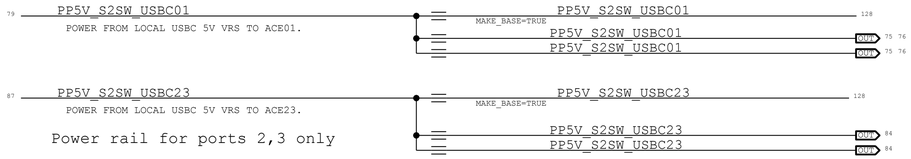
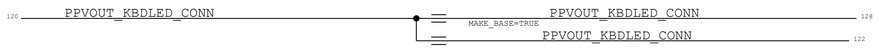
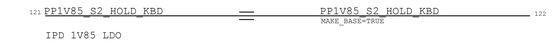
THIS PAGE WILL BE USED FOR SYSTEM / SUBSYSTEM ALIASES

USBC REQUIRED POWER ALIASES



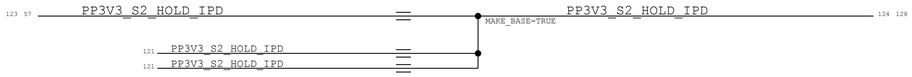
KEYBOARD BACKLIGHT



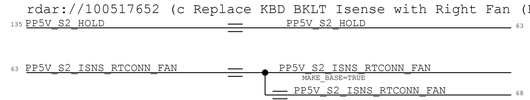


IPD: KEYBOARD / TRACKPAD

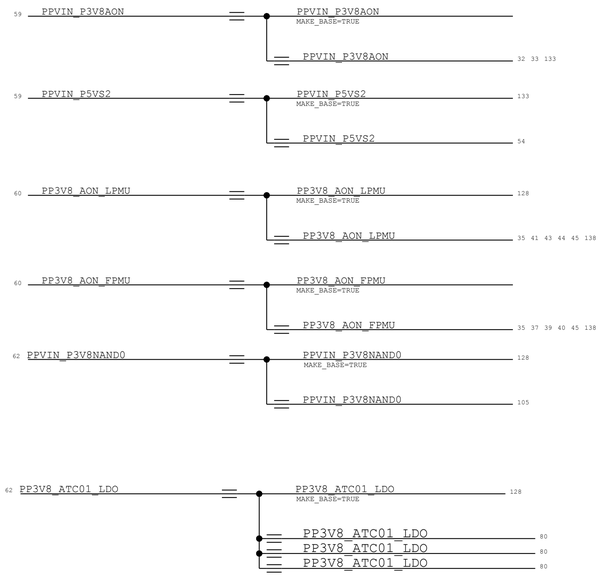
PP3V3_S2_IPD (LDO) ALIASES

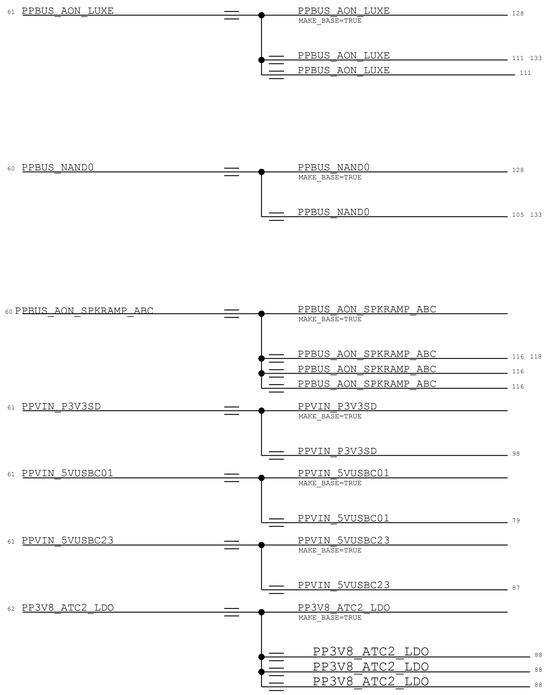


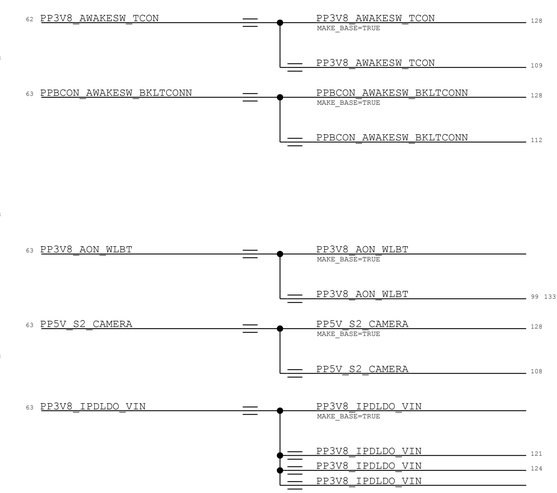
rdar://100517652 (c Replace KBD BKLT Isense with Right Fan (Fan1) 5V Isense)

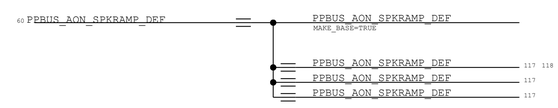


rdar://101884648 (c Replacing HDMI HS Isense (IDHC) with Mesa HS Isense (IIDR))









PAGE TITLE

POWER ALIASES 2

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TODO_DT: Update VOLTAGE proporties for H14

PCPU VR

64 48 PPVDD_PCPU_AWAKE_REGINT ═══ PPVDD_PCPU_AWAKE_REGINT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

64 49 PPVDD_PCPU_AWAKE_REGEXT5 ═══ PPVDD_PCPU_AWAKE_REGEXT5 46
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

64 53 PPVDD_PCPU_AWAKE ═══ PPVDD_PCPU_AWAKE 46 63 129
48 PPVDD_PCPU_AWAKE ═══
MAKE_BASE=TRUE
VOLTAGE=0.72V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
Spitfire Buck0 (PD#?)
═══ PPVDD_PCPU_AWAKE 15

64 48 PPVDD_PCPU_SRAM_AWAKE_REGINT ═══ PPVDD_PCPU_SRAM_AWAKE_REGINT
MAKE_BASE=TRUE
VOLTAGE=0.72V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

64 53 PPVDD_PCPU_SRAM_AWAKE ═══ PPVDD_PCPU_SRAM_AWAKE 46 63 129
48 PPVDD_PCPU_SRAM_AWAKE ═══
MAKE_BASE=TRUE
VOLTAGE=0.72V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
Spitfire Buck1 (PD#?)
═══ PPVDD_PCPU_SRAM_AWAKE 15

GPU VR

64 51 PPVDD_GPU_AWAKESW_REGINT ═══ PPVDD_GPU_AWAKESW_REGINT
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

64 52 PPVDD_GPU_AWAKESW_REGEXT5 ═══ PPVDD_GPU_AWAKESW_REGEXT5 46
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

64 52 PPVDD_GPU_AWAKESW_REGEXT6 ═══ PPVDD_GPU_AWAKESW_REGEXT6 46
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

64 53 PPVDD_GPU_AWAKESW ═══ PPVDD_GPU_AWAKESW 46 63 129
51 PPVDD_GPU_AWAKESW ═══
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
Spitfire Buck0 (PD#?)
═══ PPVDD_GPU_AWAKESW 15

PAGE TITLE
Power Aliases (3/5)

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PP1V2_S2 → PP1V2_S2 (41 43 138)
PPVDD_LOW_S2 → PPVDD_LOW_S2 (41 43 138)
LPMU LDO0
Vboot = 770mV for FuseRev>=4
800mV for FuseRev<4
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_LOW_S2 (16)
PPVDD_LOW_S2 (16)

PP3V8_AON_LPMU (41) → PP3V8_AON_LPMU (35 41 43 44 45 136 138)
PP3V3_S2 (41) → PP3V3_S2 (128 130 135)
LPMU LDO1
VOLTAGE=T.3V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
All Loads wired on other pages

PP3V8_AON_LPMU (41) → PP3V8_AON_LPMU (35 41 43 44 45 136 138)
NC_LPMU_LDO2 (41) → NC_LPMU_LDO2 MAKE_BASE=TRUE
LPMU LDO2 (Unused)

PP3V8_AON_LPMU (41) → PP3V8_AON_LPMU (35 41 43 44 45 136 138)
PP1V8_AON (41) → PP1V8_AON (128 135)
LPMU LDO3
Disables momentarily during CRASH
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
All Loads wired on other pages

PP3V8_AON_LPMU (41) → PP3V8_AON_LPMU (35 41 43 44 45 136 138)
PP3V3_AON (41) → PP3V3_AON (128 130 135)
LPMU LDO4
Disables momentarily during CRASH
VOLTAGE=T.3V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP3V3_AON (41)
PP3V3_AON (37)

GND (41) → GND (138 142)
NC_LPMU_LDO5 (41) → NC_LPMU_LDO5 MAKE_BASE=TRUE
LPMU LDO5 (Unused)

GND (41) → GND (138 142)
NC_LPMU_SW0 (41) → NC_LPMU_SW0 MAKE_BASE=TRUE
LPMU SW0 (Unused)

GND (41) → GND (138 142)
NC_LPMU_SW1 (41) → NC_LPMU_SW1 MAKE_BASE=TRUE
LPMU SW1 (Unused)

GND (41) → GND (138 142)
NC_LPMU_SW2 (41 36) → NC_LPMU_SW2 MAKE_BASE=TRUE
LPMU SW2 (Unused)

GND (37) → GND (138 142)
NC_FPMU_LDO0 (37) → NC_FPMU_LDO0 MAKE_BASE=TRUE
FPMU LDO0 (Unused)

PP3V8_AON_FPMU (37) → PP3V8_AON_FPMU (35 37 39 40 45 136 138)
PP1V8_AWAKE_SEPROM_LDO (37) → PP1V8_AWAKE_SEPROM_LDO
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_AWAKE_SEPROM_LDO (11)
FPMU LDO1

FPMU LDO2 (Project Specific)

FPMU LDO3 (Project Specific)

PP3V8_AON_FPMU (37 35) → PP3V8_AON_FPMU (35 37 39 40 45 136 138)
NC_FPMU_LDO4 (37 35) → NC_FPMU_LDO4 MAKE_BASE=TRUE (35)
FPMU LDO4 (Unused)

GND (37) → GND (138 142)
NC_FPMU_LDO5 (37) → NC_FPMU_LDO5 MAKE_BASE=TRUE
FPMU LDO5 (Unused)

Vboot note is based on actual boot voltages of latest OTP, based on SOC Tunables Spec SOC Setup Voltage Table
^ indicates 0V boot until PMGR/Volman enable

VOLTAGE property for SOC rails is based on the max of OTP and "Design-intended voltage" in SOC Tunables Spec SOC Setup Voltage Table

PPVDD_SOC_S1 (44 42 36) → PPVDD_SOC_S1 (128 130)
PPVDD_SOC_S1 (42) → PPVDD_SOC_S1
LPMU Buck0 (PD#0)
Vboot = 775mV
DVFM 665~944mV
VOLTAGE=T.944V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_SOC_S1 (16)

PPVDD_SRAM_S1 (133 44 42 36) → PPVDD_SRAM_S1
PPVDD_SRAM_S1 (42) → PPVDD_SRAM_S1
LPMU Buck1 (PD#1)
Vboot = 810mV for FuseRev>=4
850mV for FuseRev<4
VOLTAGE=T.85V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_SRAM_S1 (16)

PPVDD_ECPU_AWAKE (44 42 36) → PPVDD_ECPU_AWAKE
PPVDD_ECPU_AWAKE (42) → PPVDD_ECPU_AWAKE
LPMU Buck2 (PD#2)
Vboot = 725mV
DVFM 525~1100mV
VOLTAGE=T.06V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ECPU_AWAKE (15)

PP1V8_S2SW_VDD1 (44 42 36) → PP1V8_S2SW_VDD1 (128 130 133)
PP1V8_S2SW_VDD1 (42) → PP1V8_S2SW_VDD1
LPMU Buck3 (PD#3)
Vboot = 1.8V
Enabled in SLP_S2R and above
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2SW_VDD1 (17)

LPMU Buck4 (Unused)

LPMU Buck5 (Unused)

PPVDDQ1_S1 (44 42 36) → PPVDDQ1_S1
PPVDDQ1_S1 (42) → PPVDDQ1_S1
LPMU Buck6 (PD#6)
Vboot = 550mV
VOLTAGE=0.55V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDDQ1_S1 (5 18)

PPVDD_AMPH1_S2SW (44 42 36) → PPVDD_AMPH1_S2SW (128)
PPVDD_AMPH1_S2SW (42) → PPVDD_AMPH1_S2SW
LPMU Buck7 (PD#7)
Vboot = 1120mV
Enabled in SLP_S2R and above
VOLTAGE=T.12V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_AMPH1_S2SW (19)

PP1V2_S2 (44 43 36) → PP1V2_S2 (89 128 135)
PP1V2_S2 (43) → PP1V2_S2
LPMU Buck8 (PD#8)
Vboot = 1225mV
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_S2 (21 133)
PP1V2_S2 (5)
PP1V2_S2 (41 43 138)
PP1V2_S2 (37)

PPVDD_ECPU_SRAM_AWAKE (44 43 36) → PPVDD_ECPU_SRAM_AWAKE
PPVDD_ECPU_SRAM_AWAKE (43) → PPVDD_ECPU_SRAM_AWAKE
LPMU Buck9 (PD#9)
Vboot = 850mV
DVFM 770~1100mV
VOLTAGE=T.1V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_ECPU_SRAM_AWAKE (15)

FPMU SW0 (Project Specific)

PP1V8_S2 (37) → PP1V8_S2 (37 138)
PP1V8_AWAKE (37) → PP1V8_AWAKE (135)
FPMU SW1
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_AWAKE (11)

GND (37) → GND (138 142)
NC_FPMU_SW2 (37) → NC_FPMU_SW2 MAKE_BASE=TRUE
FPMU SW2 (Unused)

PCPUVR_SCRASH_L (129 35) MAKE_BASE=TRUE PCPUVR_SCRASH_L (47)
GPUVR_SCRASH_L (129 35) MAKE_BASE=TRUE GPUVR_SCRASH_L (50)
SOC_WDOG (43) MAKE_BASE=TRUE SOC_WDOG (10)
NC_PMU_CLK32K_CLVR_R (43 36) MAKE_BASE=TRUE NC_PMU_CLK32K_CLVR_R
NC_PMU_CLK32K_CLVR (35) MAKE_BASE=TRUE NC_PMU_CLK32K_CLVR
NC_CLVR_RESET_L (43) MAKE_BASE=TRUE NC_CLVR_RESET_L
NC_PVDD1_PWR_EN (43) MAKE_BASE=TRUE NC_PVDD1_PWR_EN
NC_LP5_IN_RESET_L (43) MAKE_BASE=TRUE NC_LP5_IN_RESET_L

PPVDD_DCS_S1 (40 38 36) → PPVDD_DCS_S1
PPVDD_DCS_S1 (39) → PPVDD_DCS_S1
FPMU Buck0 (PD#10)
Vboot = 700mV
DVFM 643~1020mV
VOLTAGE=T.02V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_DCS_S1 (16)

PPVDD_FABRIC_S1 (40 38 36) → PPVDD_FABRIC_S1 (129)
PPVDD_FABRIC_S1 (39) → PPVDD_FABRIC_S1
FPMU Buck1 (PD#11)
Vboot = 775mV
DVFM 672~968mV
VOLTAGE=T.968V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_FABRIC_S1 (19 20)

PPVDD_DISP_S1 (40 38 36) → PPVDD_DISP_S1 (128)
PPVDD_DISP_S1 (39) → PPVDD_DISP_S1
FPMU Buck2 (PD#12)
Vboot = 765mV
DVFM 651~965mV
VOLTAGE=T.965V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_DISP_S1 (16)

PP1V8_S2 (40 38 36) → PP1V8_S2 (128 135)
PP1V8_S2 (38) → PP1V8_S2
FPMU Buck3 (PD#13)
Vboot = 1.8V
VOLTAGE=T.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V8_S2 (41)
PP1V8_S2 (37 138)

PPVDDQ0_S1 (40 38 36) → PPVDDQ0_S1
PPVDDQ0_S1 (39) → PPVDDQ0_S1
FPMU Buck4 (PD#14)
Vboot = 550mV
VOLTAGE=1.55V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDDQ0_S1 (5 18)

PPVDD2H_S2SW (40 38 36) → PPVDD2H_S2SW (128)
PPVDD2H_S2SW (39) → PPVDD2H_S2SW
FPMU Buck5 (PD#15)
Vboot = 1050mV
DVFM 900~1100mV
Enabled in SLP_S2R and above
VOLTAGE=1.1V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD2H_S2SW (22)

PPVDD_CIO_S2SW (133 40 38 36) → PPVDD_CIO_S2SW
PPVDD_CIO_S2SW (39) → PPVDD_CIO_S2SW
FPMU Buck6 (PD#16)
Vboot = 850mV for FuseRev>=4
885mV for FuseRev<4
Enabled in SLP_DDR and above
Enabled in SLP_S2R if CIO device is attached
VOLTAGE=T.885V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_CIO_S2SW (19)

PPVDD_FIXED_S1 (40 38 36) → PPVDD_FIXED_S1
PPVDD_FIXED_S1 (39) → PPVDD_FIXED_S1
FPMU Buck7 (PD#17)
Vboot = 805mV for FuseRev>=4
840mV for FuseRev<=4
VOLTAGE=T.84V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_FIXED_S1 (20)

PP1V2_AWAKE (40 39 36) → PP1V2_AWAKE (128 135)
PP1V2_AWAKE (39) → PP1V2_AWAKE
FPMU Buck8 (PD#18)
Vboot = 1225mV
VOLTAGE=T.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PP1V2_AWAKE (21)
PP1V2_AWAKE (11)
PP1V2_AWAKE (11)
PP1V2_AWAKE (4 5 8 9)
PP1V2_AWAKE (43)

PPVDD_AMPH0_S2SW (40 39 36) → PPVDD_AMPH0_S2SW (128)
PPVDD_AMPH0_S2SW (39) → PPVDD_AMPH0_S2SW
FPMU Buck9 (PD#19)
Vboot = 1120mV
Enabled in SLP_S2R and above
VOLTAGE=T.12V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
PPVDD_AMPH0_S2SW (19)

PACK_OPTIONS TO INCLUDE IN NETLIST
LBUCK2:3PH
LBUCK5:N
LPMU_LDO0
FBUCK5:Y

PACK_OPTIONS TO INCLUDE IN NETLIST
SOC:S

Only req'd for project pages

PAGE TITLE
POWER ALIASES PMU (S)

Apple Inc.

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REVISION 4.0.0
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LPDPTX

MAKE_BASE=TRUE

LPDP_INT_DATA_C_P<0>	=	LPDP_INT_DATA_C_P<0>	7 109
LPDP_INT_DATA_C_N<0>	=	LPDP_INT_DATA_C_N<0>	7 109
LPDP_INT_DATA_C_P<1>	=	LPDP_INT_DATA_C_P<1>	7 109
LPDP_INT_DATA_C_N<1>	=	LPDP_INT_DATA_C_N<1>	7 109
LPDP_INT_DATA_C_P<2>	=	LPDP_INT_DATA_C_P<2>	7 109
LPDP_INT_DATA_C_N<2>	=	LPDP_INT_DATA_C_N<2>	7 109
LPDP_INT_DATA_C_P<3>	=	LPDP_INT_DATA_C_P<3>	7 109
LPDP_INT_DATA_C_N<3>	=	LPDP_INT_DATA_C_N<3>	7 109
LPDP_INT_AUX_C_P	=	LPDP_INT_AUX_C_P	7 109
LPDP_INT_AUX_C_N	=	LPDP_INT_AUX_C_N	7 109
141 LPDP_INT_HPD	=	LPDP_INT_HPD	7 109 126 141

MIPI

ENET

SD

8 PCIE_SD_UHS2_R2D_C_P	=	PCIE_SD_UHS2_R2D_C_P	95 MAKE_BASE=TRUE
8 PCIE_SD_UHS2_R2D_C_N	=	PCIE_SD_UHS2_R2D_C_N	95 MAKE_BASE=TRUE
8 PCIE_SD_UHS2_D2R_P	=	PCIE_SD_UHS2_D2R_P	95 MAKE_BASE=TRUE
8 PCIE_SD_UHS2_D2R_N	=	PCIE_SD_UHS2_D2R_N	95 MAKE_BASE=TRUE
8 PCIE_CLK100M_SD_UHS2_P	=	PCIE_CLK100M_SD_UHS2_P	95 MAKE_BASE=TRUE
8 PCIE_CLK100M_SD_UHS2_N	=	PCIE_CLK100M_SD_UHS2_N	95 MAKE_BASE=TRUE
8 SD_UHS2_RESET_L	=	SD_UHS2_RESET_L	97 MAKE_BASE=TRUE
8 SD_UHS2_CLKREQ_L	=	SD_UHS2_CLKREQ_L	97 MAKE_BASE=TRUE

USB3

LPDPRX

NAND

8 NC_PCIE_CLK100M_NAND0_1P	=	NC_PCIE_CLK100M_NAND0_1P	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND0_1N	=	NC_PCIE_CLK100M_NAND0_1N	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND0_3P	=	NC_PCIE_CLK100M_NAND0_3P	MAKE_BASE=TRUE
8 NC_PCIE_CLK100M_NAND0_3N	=	NC_PCIE_CLK100M_NAND0_3N	MAKE_BASE=TRUE

101 SWD_NAND0_S5E0_S5E1_SWCLK	=	SWD_NAND0_S5E0_S5E1_SWCLK	MAKE_BASE=TRUE
102 SWD_NAND0_S5E0_S5E1_SWCLK	=		
103 SWD_NAND0_S5E2_S5E3_SWCLK	=	SWD_NAND0_S5E2_S5E3_SWCLK	MAKE_BASE=TRUE
104 SWD_NAND0_S5E2_S5E3_SWCLK	=		
101 SWD_NAND0_S5E0_S5E1_SWDIO	=	SWD_NAND0_S5E0_S5E1_SWDIO	MAKE_BASE=TRUE
102 SWD_NAND0_S5E0_S5E1_SWDIO	=		
103 SWD_NAND0_S5E2_S5E3_SWDIO	=	SWD_NAND0_S5E2_S5E3_SWDIO	MAKE_BASE=TRUE
104 SWD_NAND0_S5E2_S5E3_SWDIO	=		

ATC3 - HDMI

9 DP_DP2HDMI_DATA_P<2>	=	DP_DP2HDMI_DATA_P<2>	
93 DP_DP2HDMI_DATA_P<2>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_N<2>	=	DP_DP2HDMI_DATA_N<2>	
93 DP_DP2HDMI_DATA_N<2>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_P<3>	=	DP_DP2HDMI_DATA_P<3>	
93 DP_DP2HDMI_DATA_P<3>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_N<3>	=	DP_DP2HDMI_DATA_N<3>	
93 DP_DP2HDMI_DATA_N<3>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_P<1>	=	DP_DP2HDMI_DATA_P<1>	
93 DP_DP2HDMI_DATA_P<1>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_N<1>	=	DP_DP2HDMI_DATA_N<1>	
93 DP_DP2HDMI_DATA_N<1>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_P<0>	=	DP_DP2HDMI_DATA_P<0>	
93 DP_DP2HDMI_DATA_P<0>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_DATA_N<0>	=	DP_DP2HDMI_DATA_N<0>	
93 DP_DP2HDMI_DATA_N<0>	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_AUX_P	=	DP_DP2HDMI_AUX_P	
93 DP_DP2HDMI_AUX_P	=	MAKE_BASE=TRUE	
9 DP_DP2HDMI_AUX_N	=	DP_DP2HDMI_AUX_N	
93 DP_DP2HDMI_AUX_N	=	MAKE_BASE=TRUE	

USBC

9 NC_USB_C0_HPD	=	NC_USB_C0_HPD	MAKE_BASE=TRUE
9 NC_USB_C1_HPD	=	NC_USB_C1_HPD	MAKE_BASE=TRUE
9 NC_USB_C2_HPD	=	NC_USB_C2_HPD	MAKE_BASE=TRUE

		MAKE_BASE=TRUE	
9 NC_EUSB_ATC3P	=	NC_EUSB_ATC3P	
		MAKE_BASE=TRUE	
9 NC_EUSB_ATC3N	=	NC_EUSB_ATC3N	

PAGE TITLE
SIGNAL ALIASES - 1 (HIGH SPEED)

Apple Inc.

DRAWING NUMBER 051-08242 | SIZE D
REVISION 4.0.0
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Internal signal aliases - Must be configured on project pages per notes below.

SOC, series caps | BBR A side | BBR B side | Connector

81 USBC_ATC2_R2D_C_P<1> = USBC_ATC2_R2D_C_P<1> 9 MAKE_BASE=TRUE
81 USBC_ATC2_R2D_C_N<1> = USBC_ATC2_R2D_C_N<1> 9 MAKE_BASE=TRUE
81 USBC_ATC2_R2D_C_P<2> = USBC_ATC2_R2D_C_P<2> 9 MAKE_BASE=TRUE
81 USBC_ATC2_R2D_C_N<2> = USBC_ATC2_R2D_C_N<2> 9 MAKE_BASE=TRUE
81 USBC_ATC2_D2R_P<1> = USBC_ATC2_D2R_P<1> 9 MAKE_BASE=TRUE
81 USBC_ATC2_D2R_N<1> = USBC_ATC2_D2R_N<1> 9 MAKE_BASE=TRUE
81 USBC_ATC2_D2R_P<2> = USBC_ATC2_D2R_P<2> 9 MAKE_BASE=TRUE
81 USBC_ATC2_D2R_N<2> = USBC_ATC2_D2R_N<2> 9 MAKE_BASE=TRUE

->

77 EUSB_DBG_P = EUSB_DBG_P MAKE_BASE=TRUE BI 9 127
77 EUSB_DBG_N = EUSB_DBG_N MAKE_BASE=TRUE BI 9 127

74 PMU_ACTIVE_READY
83 PMU_ACTIVE_READY
= PMU_ACTIVE_READY MAKE_BASE=TRUE BI 5 43 127 128 130

Caps and connector must be aliased to BBR signals.
BBR lanes 1 and 2 can be swapped, both pairs, both sides - all or nothing.
BBR inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

Added for t585_ref_usbc_1fka_3prt_ace3_951-15545_0.42.0

75 12 SWD_UPC_SWDIO0 = SWD_UPC_SWDIO0 73
75 12 SWD_UPC_SWCLK0 = SWD_UPC_SWCLK0 73

84 12 SWD_UPC_SWDIO2 = SWD_UPC_SWDIO2 82
84 12 SWD_UPC_SWCLK2 = SWD_UPC_SWCLK2 82

Internal signal aliases - Copied or debug circuitry added between.

89 77 USB2_ATC1_LS_P = USB2_ATC1_LS_P MAKE_BASE=TRUE
89 77 USB2_ATC1_LS_N = USB2_ATC1_LS_N MAKE_BASE=TRUE
89 85 USB2_ATC2_LS_P = USB2_ATC2_LS_P MAKE_BASE=TRUE
89 85 USB2_ATC2_LS_N = USB2_ATC2_LS_N MAKE_BASE=TRUE

127 9 EUSB_ATC0_P MAKE_BASE=TRUE = EUSB_ATC0_P BI 77
127 9 EUSB_ATC0_N MAKE_BASE=TRUE = EUSB_ATC0_N BI 77
127 9 EUSB_ATC1_P MAKE_BASE=TRUE = EUSB_ATC1_P BI 77
127 9 EUSB_ATC1_N MAKE_BASE=TRUE = EUSB_ATC1_N BI 77
127 9 EUSB_ATC2_P MAKE_BASE=TRUE = EUSB_ATC2_P BI 85
127 9 EUSB_ATC2_N MAKE_BASE=TRUE = EUSB_ATC2_N BI 85

IPD SWD ALIASES

123 SWD_NUB_IPD_SWDIO = SWD_NUB_IPD_SWDIO 12 MAKE_BASE=TRUE
123 SWD_NUB_IPD_SWCLK = SWD_NUB_IPD_SWCLK 12 MAKE_BASE=TRUE

PMU SYS ALIVE

128 110 105 87 43 PMU_SYS_ALIVE MAKE_BASE=TRUE
= PMU_SYS_ALIVE 68 79
= PMU_SYS_ALIVE 93

PAGE TITLE
SIGNAL ALIASES 2

Apple Inc.

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REF_SECDIS_SAK

108 FTCAM_ENABLE_1V8_OUT = FTCAM_ENABLE_1V8_OUT 107 128 MAKE_BASE=TRUE

CHGR_INT_L = CHGR_INT_L 10 28
MAKE_BASE=TRUE

HDMI

94 92 141 DPRX_INT_HPD = DPRX_INT_HPD 9
MAKE_BASE=TRUE

NC_HDMI_CECFET_EN = NC_HDMI_CECFET_EN 39
MAKE_BASE=TRUE

LPDPTX

109 7 139 126 LPDP_INT_HPD = LPDP_INT_HPD 139
MAKE_BASE=TRUE

NAND RESET

101 NAND0_RESET_L = NAND0_RESET_L 105 127
MAKE_BASE=TRUE
102 NAND0_RESET_L
103 NAND0_RESET_L
104 NAND0_RESET_L

P2 TP nets fix

129 77 TPT_MACAW0_DEBUG_SWDCLK = TPT_MACAW0_DEBUG_SWDCLK
MAKE_BASE=TRUE
129 77 TPT_MACAW0_DEBUG_SWDDAT = TPT_MACAW0_DEBUG_SWDDAT
MAKE_BASE=TRUE
129 77 TPT_MACAW1_DEBUG_SWDCLK = TPT_MACAW1_DEBUG_SWDCLK
MAKE_BASE=TRUE
129 77 TPT_MACAW1_DEBUG_SWDDAT = TPT_MACAW1_DEBUG_SWDDAT
MAKE_BASE=TRUE
129 85 TPT_MACAW2_DEBUG_SWDCLK = TPT_MACAW2_DEBUG_SWDCLK
MAKE_BASE=TRUE
129 85 TPT_MACAW2_DEBUG_SWDDAT = TPT_MACAW2_DEBUG_SWDDAT
MAKE_BASE=TRUE

10 TPT_AON_TST_CLKOUT = TPT_AON_TST_CLKOUT MAKE_BASE=TRUE

42 NC_LPMU_BUCK5_LX0 = NC_LPMU_BUCK5_LX0 MAKE_BASE=TRUE

PACK_OPTION=LBUCK5:N

SMC_I2C5

10 IN NC_I2C_SMC_SNS1_SCL = NC_I2C_SMC_SNS1_SCL
MAKE_BASE=TRUE
10 BI NC_I2C_SMC_SNS1_SDA = NC_I2C_SMC_SNS1_SDA
MAKE_BASE=TRUE

AP_I2C6

56 6 IN I2C_ATCRTMR_SCL
MAKE_BASE=TRUE
= I2C_ATCRTMR_SCL 71
= I2C_ATCRTMR_SCL 72
= I2C_ATCRTMR_SCL 81

56 6 BI I2C_ATCRTMR_SDA
MAKE_BASE=TRUE
= I2C_ATCRTMR_SDA 71
= I2C_ATCRTMR_SDA 72
= I2C_ATCRTMR_SDA 81

SPKARAMP ICC

117 116 SPKRAMP_ICC = SPKRAMP_ICC 127
MAKE_BASE=TRUE

CODEC

GND = GND
MAKE_BASE=TRUE

75 UPC_PMU_RESET_1V2 = UPC_PMU_RESET_1V2 43 129 131 134
MAKE_BASE=TRUE
76 UPC_PMU_RESET_1V2
84 UPC_PMU_RESET_1V2

78 PMU_UPC_FORCE_DFU = PMU_UPC_FORCE_DFU 35 131
MAKE_BASE=TRUE

75 73 INPUT_PWR_2LOW_L = INPUT_PWR_2LOW_L 26
MAKE_BASE=TRUE
76 INPUT_PWR_2LOW_L
84 82 INPUT_PWR_2LOW_L
30 INPUT_PWR_2LOW_L

Connecting UPC01 & UPC5 I2C1s Together

31 30 I2C_UPC01_3V3_SDA = I2C_UPC01_3V3_SDA 89 128
MAKE_BASE=TRUE
74 73 I2C_UPC01_3V3_SDA

31 30 I2C_UPC01_3V3_SCL = I2C_UPC01_3V3_SCL 89 128
MAKE_BASE=TRUE
74 73 I2C_UPC01_3V3_SCL

X2681 charger

28 P5VS2HOLD_PGOOD = P5VS2HOLD_PGOOD
MAKE_BASE=TRUE
54 P5VS2HOLD_PGOOD
129 34 P5VS2HOLD_PGOOD

X2681 ATCTMR0

12 SWD_NUB_ATCRTMR01_SWDIO = SWD_NUB_ATCRTMR01_SWDIO 71
MAKE_BASE=TRUE
= SWD_NUB_ATCRTMR01_SWDIO 72

12 SWD_NUB_ATCRTMR01_SWCLK = SWD_NUB_ATCRTMR01_SWCLK 71
MAKE_BASE=TRUE
= SWD_NUB_ATCRTMR01_SWCLK 72

12 SWD_NUB_ATCRTMR2_SWDIO = SWD_NUB_ATCRTMR2_SWDIO 81
MAKE_BASE=TRUE

12 SWD_NUB_ATCRTMR2_SWCLK = SWD_NUB_ATCRTMR2_SWCLK 81
MAKE_BASE=TRUE

TPT_VITC_RTMR_PWR_EN = TPT_VITC_RTMR_PWR_EN 134
MAKE_BASE=TRUE
NC_USBC0_3V3LDO_EN = NC_USBC0_3V3LDO_EN 134
MAKE_BASE=TRUE
TP_USB0_3V3_LDO_EN_VITC = TP_USB0_3V3_LDO_EN_VITC 134
MAKE_BASE=TRUE

128 127 5 SOC_FORCE_DFU = SOC_FORCE_DFU 78
MAKE_BASE=TRUE

X2681 SE//need check??@!!

25 NC_SE_SE_GPIO0 = NC_SE_SE_GPIO0
MAKE_BASE=TRUE
25 TP_SE_SE_GPIO1 = TP_SE_SE_GPIO1
MAKE_BASE=TRUE
25 NC_I2C_SE_SE_A_SCL = NC_I2C_SE_SE_A_SCL
MAKE_BASE=TRUE
25 NC_I2C_SE_SE_A_SDA = NC_I2C_SE_SE_A_SDA
MAKE_BASE=TRUE
25 NC_I2C_SE_SE_B_SCL = NC_I2C_SE_SE_B_SCL
MAKE_BASE=TRUE
25 NC_I2C_SE_SE_B_SDA = NC_I2C_SE_SE_B_SDA
MAKE_BASE=TRUE
25 TP_SE_SYS_GPIO0 = TP_SE_SYS_GPIO0
MAKE_BASE=TRUE
25 NC_SE_SYS_GPIO1 = NC_SE_SYS_GPIO1
MAKE_BASE=TRUE
25 NC_SE_SYS_GPIO2 = NC_SE_SYS_GPIO2
MAKE_BASE=TRUE
25 SE_IRQ_WAKE_R = SE_IRQ_WAKE_R 14
MAKE_BASE=TRUE
25 NC_I2C_SE_SYS_SCL = NC_I2C_SE_SYS_SCL
MAKE_BASE=TRUE
25 NC_I2C_SE_SYS_SDA = NC_I2C_SE_SYS_SDA
MAKE_BASE=TRUE
25 GND = GND
MAKE_BASE=TRUE

X2681 SECDIS AND LAS REF DESIGN

114 AMR1_OR_ND_1V8 = AMR1_OR_ND_1V8 141
MAKE_BASE=TRUE
114 AMR1_OR_ND_1V8 = AMR1_OR_ND_1V8 141
MAKE_BASE=TRUE
113 AMR1_OR_ND_1V8 = AMR1_OR_ND_1V8 141
MAKE_BASE=TRUE
113 AMR1_OR_ND_1V8 = AMR1_OR_ND_1V8 141
MAKE_BASE=TRUE

X2681 Charger enable

P5VS2HOLD_PWR_EN = P5VS2HOLD_PWR_EN 35 94 129
MAKE_BASE=TRUE
54 P5VS2HOLD_PWR_EN

X2681 UPC1/2 SWD moved to CSA170

X2681 HDMI DEBUG I2C

94 92 I2C_DP2HDMI_SCL = I2C_DP2HDMI_SCL 6 56
MAKE_BASE=TRUE
I2C_DP2HDMI_SCL
I2C_DP2HDMI_SCL

94 92 I2C_DP2HDMI_SDA = I2C_DP2HDMI_SDA 6 56
MAKE_BASE=TRUE
I2C_DP2HDMI_SDA
I2C_DP2HDMI_SDA

X2681 IMU

113 SPI_AOP_LAS_MISO_1V8 = SPI_AOP_LAS_MISO_1V8 14
MAKE_BASE=TRUE

43 NC_FAN_PWR_EN = NC_FAN_PWR_EN MAKE_BASE=TRUE

93 NC_TP_HDMI_SAK_RESETB_2 = NC_TP_HDMI_SAK_RESETB_2
MAKE_BASE=TRUE
DP2HDMI_RESET_R_L = DP2HDMI_RESET_R_L 92 93 94
MAKE_BASE=TRUE
HDMI_HPD_IN = HDMI_HPD_IN 90 92 93 94
MAKE_BASE=TRUE
DPRX_INT_HPD = DPRX_INT_HPD 92 94 141
MAKE_BASE=TRUE

DPRX_AUX_P = DPRX_AUX_P 92 93 94
MAKE_BASE=TRUE
DPRX_AUX_N = DPRX_AUX_N 92 93 94
MAKE_BASE=TRUE
HDMI_DDC_5V_SDA = HDMI_DDC_5V_SDA 90 92 94
MAKE_BASE=TRUE
HDMI_DDC_5V_SCL = HDMI_DDC_5V_SCL 90 92 94
MAKE_BASE=TRUE

NC_NAND0_OCARINA_WP_L = NC_NAND0_OCARINA_WP_L 105
MAKE_BASE=TRUE

110 PP1V8_AON_FPMU = PP1V8_AON_FPMU 35 37
MAKE_BASE=TRUE

78 75 NC_UPC0_AID0 = NC_UPC0_AID0
MAKE_BASE=TRUE

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ISP GPIO

AOP IO

10 NC_AOP_I2CM1_SCL	=	NC_AOP_I2CM1_SCL	MAKE_BASE=TRUE
10 NC_AOP_I2CM1_SDA	=	NC_AOP_I2CM1_SDA	MAKE_BASE=TRUE
10 NC_AOP_I2S0_MCK	=	NC_AOP_I2S0_MCK	MAKE_BASE=TRUE
10 NC_AOP_I2S0_LRCK	=	NC_AOP_I2S0_LRCK	MAKE_BASE=TRUE
10 NC_AOP_I2S0_DOUT	=	NC_AOP_I2S0_DOUT	MAKE_BASE=TRUE
10 NC_AOP_I2S0_DIN	=	NC_AOP_I2S0_DIN	MAKE_BASE=TRUE
10 NC_AOP_I2S0_BCLK	=	NC_AOP_I2S0_BCLK	MAKE_BASE=TRUE

SMC GPIO

10 SOC_DOMAIN_MGPIO_AOP1	=	SOC_DOMAIN_MGPIO_AOP1	142 MAKE_BASE=TRUE
10 NC_SMC_GPIO2	=	NC_SMC_GPIO2	MAKE_BASE=TRUE
10 NC_SMC_GPIO3	=	NC_SMC_GPIO3	MAKE_BASE=TRUE
10 NC_SMC_GPIO4	=	NC_SMC_GPIO4	MAKE_BASE=TRUE
10 NC_SMC_GPIO5	=	NC_SMC_GPIO5	MAKE_BASE=TRUE

SEP

MAKE_BASE=TRUE

6 SOC_DOMAIN_SGPIO_GRP1	=	SOC_DOMAIN_SGPIO_GRP1	142

NUB GPIO

MAKE_BASE=TRUE

10 SOC_DOMAIN_NGPIO_AOP1_0	=	SOC_DOMAIN_NGPIO_AOP1_0	142

6 NC_AP_UART3_R2D	=	NC_AP_UART3_R2D	MAKE_BASE=TRUE
6 NC_AP_UART3_D2R	=	NC_AP_UART3_D2R	MAKE_BASE=TRUE
6 NC_AP_UART3_R2D_RTS_L	=	NC_AP_UART3_R2D_RTS_L	MAKE_BASE=TRUE
6 NC_AP_UART3_D2R_CTS_L	=	NC_AP_UART3_D2R_CTS_L	MAKE_BASE=TRUE
6 NC_AP_UART4_D2R	=	NC_AP_UART4_D2R	MAKE_BASE=TRUE
6 NC_AP_UART4_R2D	=	NC_AP_UART4_R2D	MAKE_BASE=TRUE

NAND

8 SOC_DOMAIN_HGPIO_GRP0_0	=	SOC_DOMAIN_HGPIO_GRP0_0	MAKE_BASE=TRUE
8 SOC_DOMAIN_HGPIO_GRP0_1	=	SOC_DOMAIN_HGPIO_GRP0_1	MAKE_BASE=TRUE

NC SPN's

MAKE_BASE=TRUE

7 NC_DISP_TOUCH_BSYNC0	=	NC_DISP_TOUCH_BSYNC0
7 NC_DISP_TOUCH_BSYNC1	=	NC_DISP_TOUCH_BSYNC1
7 NC_DISP_TOUCH_EB	=	NC_DISP_TOUCH_EB

GND UNUSED PMU

138 GND	=	GND

ISP SPMI

MAKE_BASE=TRUE

Deprecated Debug

6 IPD_MTP_FUNC_1	=	IPD_MTP_FUNC_1	123 MAKE_BASE=TRUE

NC CIO ATC3 LSTX/RX

9 NC_CIO_ATC3_LSTX	=	NC_CIO_ATC3_LSTX	MAKE_BASE=TRUE
9 NC_CIO_ATC3_LSRX	=	NC_CIO_ATC3_LSRX	MAKE_BASE=TRUE

NC SPN's

6 NC_AP_I2S0_MCK	=	NC_AP_I2S0_MCK	MAKE_BASE=TRUE
6 NC_AP_I2S1_MCK	=	NC_AP_I2S1_MCK	MAKE_BASE=TRUE

6 SOC_DOMAIN_GPIO_GRP1_1	=	SOC_DOMAIN_GPIO_GRP1_1	142 MAKE_BASE=TRUE
6 NC_AP_SPI2_SSIN	=	NC_AP_SPI2_SSIN	MAKE_BASE=TRUE

7 NC_DISP_POL	=	NC_DISP_POL	MAKE_BASE=TRUE

SOC GPIO TPs BY DOMAIN

Nonused SOC pins pulled out by functional/power domains

142 SOC_DOMAIN_NGPIO_AOP1_0 1 (PP) PPZZ02
SM P2MM PLACE_SIDE=TOP

142 SOC_DOMAIN_GPIO_GRP1_1 1 (PP) PPZZ05
SM P2MM PLACE_SIDE=TOP

142 SOC_DOMAIN_HGPIO_GRP0_0 1 (PP) PPZZ08
SM P2MM PLACE_SIDE=TOP

142 SOC_DOMAIN_HGPIO_GRP0_1 1 (PP) PPZZ10
SM P2MM PLACE_SIDE=TOP

142 SOC_DOMAIN_MGPIO_AOP1 1 (PP) PPZZ11
SM P2MM PLACE_SIDE=TOP

142 SOC_DOMAIN_SGPIO_GRP1 1 (PP) PPZZ12
SM P2MM PLACE_SIDE=TOP

SOC PP Nets

NC SOC

6 NC_AP_UART1_R2D	=	NC_AP_UART1_R2D	MAKE_BASE=TRUE
6 NC_AP_UART1_D2R	=	NC_AP_UART1_D2R	MAKE_BASE=TRUE
6 NC_AP_UART1_R2D_RTS_L	=	NC_AP_UART1_R2D_RTS_L	MAKE_BASE=TRUE
6 NC_AP_UART1_D2R_CTS_L	=	NC_AP_UART1_D2R_CTS_L	MAKE_BASE=TRUE
6 NC_AP_UART5_R2D	=	NC_AP_UART5_R2D	MAKE_BASE=TRUE
6 NC_AP_SPI3_MOSI	=	NC_AP_SPI3_MOSI	MAKE_BASE=TRUE
6 NC_AP_SPI3_MISO	=	NC_AP_SPI3_MISO	MAKE_BASE=TRUE
6 NC_AP_SPI3_SCLK	=	NC_AP_SPI3_SCLK	MAKE_BASE=TRUE
6 NC_AP_SPI3_SSIN	=	NC_AP_SPI3_SSIN	MAKE_BASE=TRUE
6 NC_AP_SPI5_MOSI	=	NC_AP_SPI5_MOSI	MAKE_BASE=TRUE
6 NC_AP_SPI5_MISO	=	NC_AP_SPI5_MISO	MAKE_BASE=TRUE
6 NC_AP_SPI5_SCLK	=	NC_AP_SPI5_SCLK	MAKE_BASE=TRUE
6 NC_AP_SPI5_SSIN	=	NC_AP_SPI5_SSIN	MAKE_BASE=TRUE
6 NC_AP_SGPIO1	=	NC_AP_SGPIO1	MAKE_BASE=TRUE
6 NC_AP_SSPI0_MISO	=	NC_AP_SSPI0_MISO	MAKE_BASE=TRUE
6 NC_AP_SSPI0_SCLK	=	NC_AP_SSPI0_SCLK	MAKE_BASE=TRUE
7 NC_ISP_GPIO_1	=	NC_ISP_GPIO_1	MAKE_BASE=TRUE
7 NC_ISP_GPIO_2	=	NC_ISP_GPIO_2	MAKE_BASE=TRUE
7 NC_ISP_GPIO_3	=	NC_ISP_GPIO_3	MAKE_BASE=TRUE
6 NC_AP_GPIO2	=	NC_AP_GPIO2	MAKE_BASE=TRUE
6 NC_AP_GPIO6	=	NC_AP_GPIO6	MAKE_BASE=TRUE
6 NC_AP_GPIO11	=	NC_AP_GPIO11	MAKE_BASE=TRUE
6 NC_AP_GPIO12	=	NC_AP_GPIO12	MAKE_BASE=TRUE
6 NC_AP_GPIO18	=	NC_AP_GPIO18	MAKE_BASE=TRUE
6 NC_AP_GPIO19	=	NC_AP_GPIO19	MAKE_BASE=TRUE
6 NC_AP_GPIO20	=	NC_AP_GPIO20	MAKE_BASE=TRUE
6 NC_AP_GPIO23	=	NC_AP_GPIO23	MAKE_BASE=TRUE
6 NC_AP_GPIO24	=	NC_AP_GPIO24	MAKE_BASE=TRUE
6 NC_AP_GPIO25	=	NC_AP_GPIO25	MAKE_BASE=TRUE
6 NC_AP_GPIO26	=	NC_AP_GPIO26	MAKE_BASE=TRUE
6 NC_AP_GPIO27	=	NC_AP_GPIO27	MAKE_BASE=TRUE
6 NC_AP_GPIO28	=	NC_AP_GPIO28	MAKE_BASE=TRUE
6 NC_AP_GPIO30	=	NC_AP_GPIO30	MAKE_BASE=TRUE
6 NC_AP_GPIO31	=	NC_AP_GPIO31	MAKE_BASE=TRUE
6 NC_AP_GPIO32	=	NC_AP_GPIO32	MAKE_BASE=TRUE
6 NC_AP_GPIO33	=	NC_AP_GPIO33	MAKE_BASE=TRUE
10 NC_NUB_GPIO10	=	NC_NUB_GPIO10	MAKE_BASE=TRUE
10 NC_NUB_GPIO13	=	NC_NUB_GPIO13	MAKE_BASE=TRUE
10 NC_NUB_GPIO14	=	NC_NUB_GPIO14	MAKE_BASE=TRUE
10 NC_NUB_GPIO15	=	NC_NUB_GPIO15	MAKE_BASE=TRUE

NC SOC P2

7 NC_SENSOR0_CLK	=	NC_SENSOR0_CLK	MAKE_BASE=TRUE
6 NC_AP_GPIO5	=	NC_AP_GPIO5	MAKE_BASE=TRUE
10 NC_NUB_GPIO6	=	NC_NUB_GPIO6	MAKE_BASE=TRUE
10 NC_NUB_GPIO0	=	NC_NUB_GPIO0	MAKE_BASE=TRUE
7 NC_LPDPRX_AUX_D0P	=	NC_LPDPRX_AUX_D0P	MAKE_BASE=TRUE
7 NC_ISP_SPMI0_SCLK	=	NC_ISP_SPMI0_SCLK	MAKE_BASE=TRUE
7 NC_ISP_SPMI0_SDATA	=	NC_ISP_SPMI0_SDATA	MAKE_BASE=TRUE
129 6 TPT_AP_UART2_R2D_RTS_L	=	TPT_AP_UART2_R2D_RTS_L	MAKE_BASE=TRUE
129 6 TPT_AP_UART2_D2R_CTS_L	=	TPT_AP_UART2_D2R_CTS_L	MAKE_BASE=TRUE
129 6 TPT_AP_UART2_R2D	=	TPT_AP_UART2_R2D	MAKE_BASE=TRUE
129 6 TPT_AP_UART2_D2R	=	TPT_AP_UART2_D2R	MAKE_BASE=TRUE
6 NC_AP_I2S3_LRCK	=	NC_AP_I2S3_LRCK	MAKE_BASE=TRUE
6 NC_AP_I2S3_DOUT	=	NC_AP_I2S3_DOUT	MAKE_BASE=TRUE
6 NC_AP_I2S3_DIN	=	NC_AP_I2S3_DIN	MAKE_BASE=TRUE
6 NC_AP_I2S3_BCLK	=	NC_AP_I2S3_BCLK	MAKE_BASE=TRUE
6 NC_AP_I2S2_MCK	=	NC_AP_I2S2_MCK	MAKE_BASE=TRUE
6 NC_AP_GPIO36	=	NC_AP_GPIO36	MAKE_BASE=TRUE
6 NC_AP_GPIO35	=	NC_AP_GPIO35	MAKE_BASE=TRUE
6 NC_AP_GPIO22	=	NC_AP_GPIO22	MAKE_BASE=TRUE
10 NC_AOP_SCM_IO15	=	NC_AOP_SCM_IO15	MAKE_BASE=TRUE
10 NC_AOP_UART2_TXD	=	NC_AOP_UART2_TXD	MAKE_BASE=TRUE
10 NC_AOP_UART2_RXD	=	NC_AOP_UART2_RXD	MAKE_BASE=TRUE
6 NC_FPWM1	=	NC_FPWM1	MAKE_BASE=TRUE
6 NC_FPWM2	=	NC_FPWM2	MAKE_BASE=TRUE

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HDMI UART_R2D

92 6 UART_DP2HDMI_R2D — TP-P5 TPE500

VITAMIN C

134 77 ATCRTMR0_RESET_1V2_1V8_MCW_L = ATCRTMR0_RESET_1V2_1V8_MCW_L MAKE_BASE=TRUE
128 ATCRTMR0_RESET_1V2_1V8_MCW_L =

134 SOC_JTAG_TDO = SOC_JTAG_TDO MAKE_BASE=TRUE
127 10 SOC_JTAG_TDO =

134 SOC_JTAG_TDI = SOC_JTAG_TDI MAKE_BASE=TRUE
127 10 SOC_JTAG_TDI =

134 NC_DC_MUX_SEL = NC_DC_MUX_SEL MAKE_BASE=TRUE

I2C CKPLUS WAIVER

128 124 121 BI I2C_KBD_SCL
CKPLUS_WAIVE=I2C_PULLUP

128 124 121 BI I2C_KBD_SDA
CKPLUS_WAIVE=I2C_PULLUP

USB LEVEL SHIFTER

78 76 USB2_ATC1_DBG_LS_P = USB2_ATC1_DBG_LS_P 143
MAKE_BASE=TRUE

78 76 USB2_ATC1_DBG_LS_N = USB2_ATC1_DBG_LS_N 143
MAKE_BASE=TRUE

75 USB_DBG_LS_P = USB_DBG_LS_P 128 143
MAKE_BASE=TRUE

75 USB_DBG_LS_N = USB_DBG_LS_N 128 143
MAKE_BASE=TRUE

134 USB_DBG_LS_P = USB_DBG_LS_P 128 143
MAKE_BASE=TRUE

134 USB_DBG_LS_N = USB_DBG_LS_N 128 143
MAKE_BASE=TRUE

134 USB_DBG_LS_MUX_P = USB_DBG_LS_MUX_P
77 USB_DBG_LS_MUX_P = MAKE_BASE=TRUE

134 USB_DBG_LS_MUX_N = USB_DBG_LS_MUX_N
77 USB_DBG_LS_MUX_N = MAKE_BASE=TRUE

77 USB2_ATC0_LS_MUX_P = USB2_ATC0_LS_MUX_P
134 USB2_ATC0_LS_MUX_P = MAKE_BASE=TRUE

77 USB2_ATC0_LS_MUX_N = USB2_ATC0_LS_MUX_N
134 USB2_ATC0_LS_MUX_N = MAKE_BASE=TRUE

89 USB2_ATC0_LS_P = USB2_ATC0_LS_P 128
134 USB2_ATC0_LS_P = MAKE_BASE=TRUE

89 USB2_ATC0_LS_N = USB2_ATC0_LS_N 128
134 USB2_ATC0_LS_N = MAKE_BASE=TRUE

DUAL KIS ONLY aliases

TP0500 TP-P5 TP USB2_ATC1_DBG_LS_P MAKE_BASE=TRUE = USB2_ATC1_DBG_LS_P BI 77
TP0501 TP-P5 TP USB2_ATC1_DBG_LS_N MAKE_BASE=TRUE = USB2_ATC1_DBG_LS_N BI 77

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Signal Aliases - SGA/CGA Diffs

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8 7 6 5 4 3 2 1

SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup, shortest distance is used unless "1" is defined	EXAMPLE: 1,2,3,4,5,6,8,9,10, 2-10
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from hybrid table and stackup, shortest distance is used unless "1" defined	EXAMPLE: 1,"SDRAM_CLK_VIA", PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup, shortest distance is used unless "1," is defined	EXAMPLE: 2,4,6,8,10, ?

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17.2 RULES

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PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS ENABLED
	CLASS NAME	DIFF/SE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
	I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
T724->	SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*,HDMI*SCL,HDMI*SDA	Y
	SPMI	P	A_45_OHM_SE	*SPMI*	Y
	SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
	JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
	CLOCK_24M	P	A_45_OHM_SE	SOC_24M_O_R,NAND0_CLK24M*	Y
	SOC_XTAL_24M_IN	P	A_45_OHM_SE	SOC_XTAL24M_IN	Y
	SOC_XTAL_24M_OUT	P	A_45_OHM_SE	SOC_XTAL24M_OUT	Y
	CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
	TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*.TDM_SPKRAMP_A*,TDM_SPKRAMP_B*	Y
	TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*,TDM_SPKRAMP_D*,TDM_SPKRAMP_E*	Y
	TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
	SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
	UART	P	A_45_OHM_SE	UART_*	Y
	RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
	WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
	SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
	POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
	FAULT	P	A_45_OHM_SE	*FAULT*	Y
	DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
	FAN_CTRL	P	A_45_OHM_SE	SMC_FAN_*,FAN*PWM*,*FAN*TACH	Y
->	USBC_SOC_BSB0_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_D2R_C_1	Y
	USBC_SOC_BSB0_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_D2R_C_2	Y
	USBC_SOC_BSB0_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_R2D_1	Y
	USBC_SOC_BSB0_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_R2D_2	Y
	USBC_SOC_BSB0_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_AUX	Y
	USBC_SOC_BSB0_LSX	P	A_45_OHM_SE	CIO_ATC0_LS*	Y
	USBC_BSB0_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC0_D2R_CR_1	Y
	USBC_BSB0_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC0_D2R_CR_2	Y
	USBC_BSB0_CONN_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC0_R2D_C_1	Y
	USBC_BSB0_CONN_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC0_R2D_C_2	Y
	USBC_BSB0_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC0_AUXLSX	Y
	USBC_UPC0_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_USBC0_USB_TOP	Y
	USBC_UPC0_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_USBC0_USB_BOT	Y
	USBC_UPC0_CONN_CC	P	WIDTH_0P400	USBC0_CC*	Y
	USBC_UPC0_CONN_SBU	P	A_45_OHM_SE	USBC0_SBU*	Y
	USBC_SOC_RTMR0_USB2	P	A_85_OHM_DIFF	DP:DP_EUSB_ATC0	Y
	USBC_RTMR0_MUX_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC0_LS_MUX	Y
->	USBC_MUX_UPC0_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC0_LS	Y
	USBC_MUX_VITC_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC0_LS_VITAMINC	Y
	USBC_SOC_BSB1_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_D2R_C_1	Y
	USBC_SOC_BSB1_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_D2R_C_2	Y
	USBC_SOC_BSB1_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_R2D_1	Y
	USBC_SOC_BSB1_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_R2D_2	Y
	USBC_SOC_BSB1_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_AUX	Y
	USBC_SOC_BSB1_LSX	P	A_45_OHM_SE	CIO_ATC1_LS*	Y
	USBC_BSB1_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC1_D2R_CR_1	Y
	USBC_BSB1_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC1_D2R_CR_2	Y
	USBC_BSB1_CONN_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC1_R2D_C_1	Y
	USBC_BSB1_CONN_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC1_R2D_C_2	Y
	USBC_BSB1_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC1_AUXLSX	Y
	USBC_UPC1_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_USBC1_USB_TOP	Y
	USBC_UPC1_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_USBC1_USB_BOT	Y
	USBC_UPC1_CONN_CC	P	WIDTH_0P400	USBC1_CC*	Y
	USBC_UPC1_CONN_SBU	P	A_45_OHM_SE	USBC1_SBU*	Y
	USBC_SOC_RTMR1_USB2	P	A_85_OHM_DIFF	DP:DP_EUSB_ATC1	Y
	USBC_RTMR1_UPC1_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC1_LS	Y
	USBC_SOC_RTMR_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_EUSB_DBG	Y
	USBC_RTMR_MUX_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_USB_DBG_LS_MUX	Y
	USBC_MUX_UPC_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_USB_DBG_LS	Y
	USBC_MUX_VITC_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_USB_DBG_LS_VITAMINC	Y
	USBC_LSX	P	A_45_OHM_SE	*ATC*LS*X	Y
	MIPI_FTCAM_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_CLK,DP_MIPI_CLOCK_CONN	Y
	MIPI_FTCAM_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_DATA_0,DP_MIPI_DATA_CONN	Y
	MIPI_DFR_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_DFR_CLK_CONN_FILT	Y
	MIPI_DFR_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_DFR_DATA_CONN_FILT	Y
	PCIE_WIFI_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT_D2R_C	Y
	PCIE_WIFI_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT_R2D_C	Y
	PCIE_WIFI_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M_WLBT	Y
	PCIE_NAND0_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_D2R_C_0	Y
	PCIE_NAND0_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_R2D_C_0	Y
	PCIE_NAND0_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M_NAND0_0	Y
	PCIE_NAND1_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_D2R_C_1	Y
	PCIE_NAND1_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_R2D_C_1	Y
	PCIE_NAND1_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M_NAND0_1	Y
	PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
	PANEL_LPDP_DATA	P	A_85_OHM_DIFF	DP:DP_DP0,DP_DP1,DP_DP2,DP_DP3	Y
	PANEL_LPDP_AUX	P	A_85_OHM_DIFF	DP:DP_AUX	Y
	RCAL_PCIE	P	WIDTH_0P100	SOC_ST_PCIE_RCAL*,SOC_GP_PCIE_RCAL*	Y
	RCAL_CIO	P	WIDTH_0P100	SOC_ATCPHY0_RCAL*,SOC_ATCPHY1_RCAL*	Y
	RCAL_MIPI	P	WIDTH_0P100	*MIPI*REXT	Y
	RCAL_EUSB	P	WIDTH_0P100	SOC_ATC*_USB_RESREF,SOC_USBDBG_RESREF	Y
	BOARD_ID	P	A_45_OHM_SE	BOARD_ID*	Y
	BOARD_REV	P	A_45_OHM_SE	BOARD_REV*	Y
	WIRELESS_TIME_SYNC	P	A_45_OHM_SE	*TIME_SYNC*	Y
	KBD_PWM	P	A_45_OHM_SE	*KBD_BKLT_PWM*,BKLT_PWM_KEYB_3V3	Y
	HDMI_CLK_CONN	P	A_85_OHM_DIFF	DP:HDMI_CLK_CONN	Y
	HDMI_MADEA_CONN_DATA	P	A_85_OHM_DIFF	DP:HDMI_DATA*	Y
	SOC_MADEA_DATA	P	A_85_OHM_DIFF	DP:DPRX_DATA*	Y

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS ENABLED
	CLASS NAME	DIFF/SE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
	GROUND	P	DEFAULT	GND	Y
	ANALOG_GROUND	P	DEFAULT	*AGND*,GND_*	Y
	AUDIO_CONN_HEADPHONE_OUT	P	WIDTH_0P400	AUDIO_JACK_LEFT_OUT,AUDIO_JACK_RIGHT_OUT	Y
	AUDIO_CONN_HEADPHONE_OUT	P	WIDTH_0P400	AUD_CONN_LEFT_OUT,AUD_CONN_RIGHT_OUT	Y
	AUDIO_CONN_RETURN	P	WIDTH_0P500	AUDIO_JACK_GB_GND,AUDIO_JACK_CH_GND	Y
	AUDIO_CONN_RETURN	P	WIDTH_0P500	AUD_CONN_RING2,AUD_CONN_SLEEVE	Y
	AUDIO_CONN_SENSE	P	WIDTH_0P100	AUDIO_JACK_LEFT_SNS,AUDIO_JACK_RIGHT_SNS	Y
	AUDIO_CONN_SENSE	P	WIDTH_0P100	AUDIO_JACK_TIP_SNS,AUDIO_JACK_RING_SNS	Y
	AUDIO_CONN_SENSE	P	WIDTH_0P100	AUD_CONN_LEFT_SNS,AUD_CONN_RIGHT_SNS	Y
	AUDIO_CONN_SENSE	P	WIDTH_0P100	AUD_CONN_TIP_SENSE,AUD_CONN_RING_SENSE	Y
	SPEAKERAMP_OUTPUT	P	SPKRAMP_OUT_DIFF	DP:DP_SPKRAMP_*_OUT	Y
	SENSE_DIFF	P	SENSE_DIFF	DP:DP_CHGR_CS*,DP_ISNS_*,DP_*VSNS_XW,DP_*_VSEN_XW	Y
	SENSE_DIFF	P	SENSE_DIFF	DP:DP_SPMU_TDEV,DP_SPKRAMP_*_VSENSE	Y
	SENSE_DIFF	P	SENSE_DIFF	DP:DP_P3V8AON_ISEN*,DP_THMSNS*,DP_ISNS_*LCD	Y
	SENSE_DIFF	P	SENSE_DIFF	DP:DP_SOC_*_RCAL,DP_P3V8IDIF2_FB	Y
	SENSE_DIFF	P	SENSE_DIFF	DP:DP_P3V8AON_VSNS,DP_ATCRTMR*_THERM_D	Y
	RF_ANTENNA	P	WIDTH_0P100	RF_ANT_0,RF_ANT_1	Y
	PMU_BUCK_FB	P	VR_FEEDBACK	BUCK*_FB*	Y
	POWER	P	POWER	PP*	Y
T724->	USBC_SOC_BSB2_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC2_D2R_C_1	Y
	USBC_SOC_BSB2_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC2_D2R_C_2	Y
	USBC_SOC_BSB2_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC2_R2D_1	Y
	USBC_SOC_BSB2_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC2_R2D_2	Y
	USBC_SOC_BSB2_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC2_AUX	Y
	USBC_SOC_BSB2_LSX	P	A_45_OHM_SE	CIO_ATC2_LS*	Y
	USBC_BSB2_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC2_D2R_CR_1	Y
	USBC_BSB2_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC2_D2R_CR_2	Y
	USBC_BSB2_CONN_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC2_R2D_C_1	Y
	USBC_BSB2_CONN_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC2_R2D_C_2	Y
	USBC_BSB2_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC2_AUXLSX	Y
	USBC_UPC2_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_USBC2_USB_TOP	Y
	USBC_UPC2_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_USBC2_USB_BOT	Y
	USBC_UPC2_CONN_CC	P	WIDTH_0P400	USBC2_CC*	Y
	USBC_UPC2_CONN_SBU	P	A_45_OHM_SE	USBC2_SBU*	Y
	USBC_SOC_RTMR2_USB2	P	A_85_OHM_DIFF	DP:DP_EUSB_ATC2	Y
	USBC_RTMR2_MUX_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC2_LS_MUX	Y
	USBC_MUX_UPC2_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC2_LS	Y
	LOW_SPEED	P	A_45_OHM_SE	HDMI*RX,HDMI*TX	Y
	SW_NODE	P	DEFAULT	CHGR_BOOT*,*GATE*,PP*LX*,P*LX*NAND*,LUXE_LG*	Y
	SW_NODE	P	DEFAULT	*BST*,*DRVH*,DRVL*,P*SW*,*DRVL*	Y
	SW_NODE	P	DEFAULT	*PHASE*,*SNUB*,*BUCK*LX*	Y
	CLS_ATCRTMR_XTAL_IN	P	A_45_OHM_SE	ATCRTMR*XTAL*IN	Y
	CLS_ATCRTMR_XTAL_OUT	P	A_45_OHM_SE	ATCRTMR*XTAL*OUT	Y

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17.2 PHYSICAL CSETS

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
	CLASS NAME	NON-NAN	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
	I2C	S	A_DIELECTRIC_3X	=	Y
	SPI	S	A_DIELECTRIC_3X	=	Y
	SPMI	S	A_DIELECTRIC_3X	=	Y
	SWD	S	A_DIELECTRIC_3X	=	Y
	JTAG	S	A_DIELECTRIC_2X	=	Y
	CLOCK_24M	S	A_DIELECTRIC_8X	=	Y
	SOC_XTAL_24M_IN	S	A_DIELECTRIC_8X	=	Y
	SOC_XTAL_24M_OUT	S	A_DIELECTRIC_8X	=	Y
	CLOCK_32K	S	A_DIELECTRIC_8X	=	Y
	TDM_LEFT	S	A_DIELECTRIC_3X	=	Y
	TDM_RIGHT	S	A_DIELECTRIC_3X	=	Y
	TDM_CODEC	S	A_DIELECTRIC_3X	=	Y
	SPKR_ICC	S	A_DIELECTRIC_3X	=	Y
	UART	S	A_DIELECTRIC_2X	=	Y
	RESETS	S	A_DIELECTRIC_3X	=	Y
	WDOG	S	A_DIELECTRIC_3X	=	Y
	SOCHOT	S	A_DIELECTRIC_3X	=	Y
	POWER_BUTTON	S	A_DIELECTRIC_3X	=	Y
	FAULT	S	A_DIELECTRIC_3X	=	Y
	DMIC_PDM	S	A_DIELECTRIC_3X	=	Y
	FAN_CTRL	S	A_DIELECTRIC_2X	=	Y
T724->	USBC_SOC_BSB0_D2R_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB0_D2R_2	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB0_R2D_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB0_R2D_2	S	A_DIELECTRIC_7X	=	Y
	USBC_SOC_BSB0_AUX	S	A_DIELECTRIC_6X	=	Y
	USBC_SOC_BSB0_LSX	S	A_DIELECTRIC_6X	=	Y
T724->	USBC_BSB0_CONN_D2R_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB0_CONN_D2R_2	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB0_CONN_R2D_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB0_CONN_R2D_2	S	A_DIELECTRIC_7X	=	Y
	USBC_BSB0_CONN_AUXLSX	S	A_DIELECTRIC_6X	=	Y
	USBC_UPC0_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
	USBC_UPC0_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
	USBC_UPC0_CONN_CC	S	A_DIELECTRIC_2X	=	Y
	USBC_UPC0_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
	USBC_SOC_RTMR0_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_RTMR0_MUX_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_MUX_UPC0_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_MUX_VITC_USB2	S	A_DIELECTRIC_6X	=	Y
T724->	USBC_SOC_BSB1_D2R_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB1_D2R_2	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB1_R2D_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB1_R2D_2	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_SOC_BSB1_AUX	S	A_DIELECTRIC_6X	=	Y
T724->	USBC_SOC_BSB1_LSX	S	A_DIELECTRIC_6X	=	Y
T724->	USBC_BSB1_CONN_D2R_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB1_CONN_D2R_2	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB1_CONN_R2D_1	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB1_CONN_R2D_2	S	A_DIELECTRIC_7X	=	Y
T724->	USBC_BSB1_CONN_AUXLSX	S	A_DIELECTRIC_6X	=	Y
	USBC_UPC1_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
	USBC_UPC1_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
	USBC_UPC1_CONN_CC	S	A_DIELECTRIC_2X	=	Y
	USBC_UPC1_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
	USBC_SOC_RTMR1_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_RTMR1_UPC1_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_SOC_RTMR_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
	USBC_RTMR_MUX_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
	USBC_MUX_UPC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
	USBC_MUX_VITC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
	USBC_LSX	S	A_DIELECTRIC_6X	=	Y
	MIPI_FTCAM_CLK	S	A_DIELECTRIC_6X	=	Y
	MIPI_FTCAM_DATA	S	A_DIELECTRIC_6X	=	Y
	MIPI_DFR_CLK	S	A_DIELECTRIC_6X	=	Y
	MIPI_DFR_DATA	S	A_DIELECTRIC_6X	=	Y
	PCIE_WIFI_D2R	S	A_DIELECTRIC_7X	=	Y
	PCIE_WIFI_R2D	S	A_DIELECTRIC_7X	=	Y
	PCIE_WIFI_CLK	S	A_DIELECTRIC_7X	=	Y
	PCIE_NAND0_D2R	S	A_DIELECTRIC_7X	=	Y
	PCIE_NAND0_R2D	S	A_DIELECTRIC_7X	=	Y
	PCIE_NAND0_CLK	S	A_DIELECTRIC_7X	=	Y
	PCIE_NAND1_D2R	S	A_DIELECTRIC_7X	=	Y
	PCIE_NAND1_R2D	S	A_DIELECTRIC_7X	=	Y
	PCIE_NAND1_CLK	S	A_DIELECTRIC_7X	=	Y
	PCIE_CLKREQ	S	A_DIELECTRIC_2X	=	Y
T724->	PANEL_LPDP_DATA	S	A_DIELECTRIC_7X	=	Y
T724->	PANEL_LPDP_AUX	S	A_DIELECTRIC_6X	=	Y
	RCAL_PCIE	S	A_DIELECTRIC_2X	=	Y
	RCAL_CIO	S	A_DIELECTRIC_2X	=	Y
	RCAL_MIPI	S	A_DIELECTRIC_2X	=	Y
	RCAL_EUSB	S	A_DIELECTRIC_2X	=	Y
	BOARD_ID	S	A_DIELECTRIC_2X	=	Y
	BOARD_REV	S	A_DIELECTRIC_2X	=	Y
	WIRELESS_TIME_SYNC	S	A_DIELECTRIC_2X	=	Y
	KBD_PWM	S	A_DIELECTRIC_2X	=	Y
	GROUND	S	DEFAULT	=	Y
	ANALOG_GROUND	S	DEFAULT	=	Y
	AUDIO_CONN_HEADPHONE_OUT	S	A_DIELECTRIC_3X	=	Y
	AUDIO_CONN_RETURN	S	A_DIELECTRIC_2X	=	Y
	AUDIO_CONN_SENSE	S	A_DIELECTRIC_2X	=	Y
	SPEAKERAMP_OUTPUT	S	A_DIELECTRIC_2X	=	Y
	SENSE_DIFF	S	A_DIELECTRIC_2X	=	Y
	RF_ANTENNA	S	RF_ANTENNA	=	Y
	PMU_BUCK_FB	S	DEFAULT	=	Y
	POWER	S	DEFAULT	=	Y

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
	CLASS NAME	NON-NAN	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
T724->	USBC_SOC_BSB2_D2R_1	S	A_DIELECTRIC_7X	=	Y
	USBC_SOC_BSB2_D2R_2	S	A_DIELECTRIC_7X	=	Y
	USBC_SOC_BSB2_R2D_1	S	A_DIELECTRIC_7X	=	Y
	USBC_SOC_BSB2_R2D_2	S	A_DIELECTRIC_7X	=	Y
	USBC_SOC_BSB2_AUX	S	A_DIELECTRIC_6X	=	Y
	USBC_SOC_BSB2_LSX	S	A_DIELECTRIC_6X	=	Y
	USBC_BSB2_CONN_D2R_1	S	A_DIELECTRIC_7X	=	Y
	USBC_BSB2_CONN_D2R_2	S	A_DIELECTRIC_7X	=	Y
	USBC_BSB2_CONN_R2D_1	S	A_DIELECTRIC_7X	=	Y
	USBC_BSB2_CONN_R2D_2	S	A_DIELECTRIC_7X	=	Y
	USBC_BSB2_CONN_AUXLSX	S	A_DIELECTRIC_6X	=	Y
	USBC_UPC2_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
	USBC_UPC2_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
	USBC_UPC2_CONN_CC	S	A_DIELECTRIC_2X	=	Y
	USBC_UPC2_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
	USBC_SOC_RTMR2_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_RTMR2_MUX_USB2	S	A_DIELECTRIC_6X	=	Y
	USBC_MUX_UPC2_USB2	S	A_DIELECTRIC_6X	=	Y
T724 HDMI->	HDMI_CLK_CONN	S	A_DIELECTRIC_6X	=	Y
	HDMI_MADEA_CONN_DATA	S	A_DIELECTRIC_6X	=	Y
	SOC_MADEA_DATA	S	A_DIELECTRIC_6X	=	Y
	SW_NODE	S	A_DIELECTRIC_6X	=	Y

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17.2 SPACING CSETS, ISO

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	GROUND	DEFAULT
SPI	GROUND	DEFAULT
SPMI	GROUND	DEFAULT
SWD	GROUND	DEFAULT
JTAG	GROUND	DEFAULT
CLOCK_24M	GROUND	DEFAULT
CLOCK_32K	GROUND	DEFAULT
TDM_LEFT	GROUND	DEFAULT
TDM_RIGHT	GROUND	DEFAULT
TDM_CODEC	GROUND	DEFAULT
SPKR_ICC	GROUND	DEFAULT
UART	GROUND	DEFAULT
RESETS	GROUND	DEFAULT
WDOG	GROUND	DEFAULT
SOCHOT	GROUND	DEFAULT
POWER_BUTTON	GROUND	DEFAULT
FAULT	GROUND	DEFAULT
DMIC_PDM	GROUND	DEFAULT
FAN_CTRL	GROUND	DEFAULT
USBC_SOC_BSB0_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_AUX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_LSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_AUXLSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_TOP	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_BOT	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_CC	GROUND	DEFAULT
USBC_UPC0_CONN_SBU	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC0_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_AUX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_LSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_AUXLSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_TOP	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_BOT	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_CC	GROUND	DEFAULT
USBC_UPC1_CONN_SBU	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_DATA	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_DATA	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_D2R	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_R2D	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_D2R	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_R2D	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_D2R	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_R2D	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_CLKREQ	GROUND	DEFAULT
PANEL_LPDP_DATA	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PANEL_LPDP_AUX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
RCAL_PCIE	GROUND	DEFAULT
RCAL_CIO	GROUND	DEFAULT
RCAL_MIPI	GROUND	DEFAULT
BOARD_ID	GROUND	DEFAULT
BOARD_REV	GROUND	DEFAULT
WIRELESS_TIME_SYNC	GROUND	DEFAULT
KBD_PWM	GROUND	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	GROUND	DEFAULT
AUDIO_CONN_RETURN	GROUND	DEFAULT
AUDIO_CONN_SENSE	GROUND	DEFAULT
SPEAKERAMP_OUTPUT	GROUND	DEFAULT
SENSE_DIFF	GROUND	DEFAULT
SOC_XTAL_24M_IN	GROUND	DEFAULT
SOC_XTAL_24M_OUT	GROUND	DEFAULT
POWER	GROUND	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	POWER	DEFAULT
SPI	POWER	DEFAULT
SPMI	POWER	DEFAULT
SWD	POWER	DEFAULT
JTAG	POWER	DEFAULT
CLOCK_24M	POWER	DEFAULT
CLOCK_32K	POWER	DEFAULT
TDM_LEFT	POWER	DEFAULT
TDM_RIGHT	POWER	DEFAULT
TDM_CODEC	POWER	DEFAULT
SPKR_ICC	POWER	DEFAULT
UART	POWER	DEFAULT
RESETS	POWER	DEFAULT
WDOG	POWER	DEFAULT
SOCHOT	POWER	DEFAULT
POWER_BUTTON	POWER	DEFAULT
FAULT	POWER	DEFAULT
DMIC_PDM	POWER	DEFAULT
FAN_CTRL	POWER	DEFAULT
USBC_SOC_BSB0_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_AUX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_LSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_AUXLSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_TOP	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_BOT	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_CC	POWER	DEFAULT
USBC_UPC0_CONN_SBU	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC0_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_AUX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_LSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_AUXLSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_TOP	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_BOT	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_CC	POWER	DEFAULT
USBC_UPC1_CONN_SBU	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_DATA	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_DATA	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_D2R	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_R2D	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_D2R	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_R2D	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_D2R	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_R2D	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_CLKREQ	POWER	DEFAULT
PANEL_LPDP_DATA	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PANEL_LPDP_AUX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
RCAL_PCIE	POWER	DEFAULT
RCAL_CIO	POWER	DEFAULT
RCAL_MIPI	POWER	DEFAULT
BOARD_ID	POWER	DEFAULT
BOARD_REV	POWER	DEFAULT
WIRELESS_TIME_SYNC	POWER	DEFAULT
KBD_PWM	POWER	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	POWER	DEFAULT
AUDIO_CONN_RETURN	POWER	DEFAULT
AUDIO_CONN_SENSE	POWER	DEFAULT
SPEAKERAMP_OUTPUT	POWER	DEFAULT
SENSE_DIFF	POWER	DEFAULT
SOC_XTAL_24M_IN	POWER	DEFAULT
SOC_XTAL_24M_OUT	POWER	DEFAULT
POWER	POWER	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

	CLASS TO CLASS SPACING		
	CLASS NAME	CLASS NAME	CONSTRAINT SET
T724->	USBC_SOC_BSB0_D2R_1	USBC_SOC_BSB0_D2R_2	A_DIELECTRIC_5X
T724->	USBC_SOC_BSB0_R2D_1	USBC_SOC_BSB0_R2D_2	A_DIELECTRIC_5X
T724->	USBC_BSB0_CONN_D2R_1	USBC_BSB0_CONN_D2R_2	A_DIELECTRIC_5X
T724->	USBC_BSB0_CONN_R2D_1	USBC_BSB0_CONN_R2D_2	A_DIELECTRIC_5X
T724->	USBC_SOC_BSB1_D2R_1	USBC_SOC_BSB1_D2R_2	A_DIELECTRIC_5X
T724->	USBC_SOC_BSB1_R2D_1	USBC_SOC_BSB1_R2D_2	A_DIELECTRIC_5X
T724->	USBC_BSB1_CONN_D2R_1	USBC_BSB1_CONN_D2R_2	A_DIELECTRIC_5X
T724->	USBC_BSB1_CONN_R2D_1	USBC_BSB1_CONN_R2D_2	A_DIELECTRIC_5X
	PANEL_LPDP_DATA	PANEL_LPDP_DATA	A_DIELECTRIC_5X
	SOC_XTAL_24M_IN	SOC_XTAL_24M_OUT	A_DIELECTRIC_2X

PAGE TITLE
17.2 SPACING CSETS, CLASS-CLASS

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USBC page BOM

Select options as needed.

Multi-protocol Retimer(Lifuka)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	3	IC,RTMR,A0,USB-C RETIMER,FCCSP154	UF000,UF100,UG000	CRITICAL	ATCRTMR:A0
338S00773	3	IC,LIFUKA,B0,USB-C RETIMER,CSP154	UF000,UF100,UG000	CRITICAL	RT13:B0_MP
998-25504	3	IC,RTMR,B0,USB-C RETIMER,DEV,CSP154	UF000,UF100,UG000	CRITICAL	RT13:B0
998-27476	3	IC,LIFUKA,B1,USB-C RETIMER,DEV,CSP154	UF000,UF100,UG000	CRITICAL	RT13:B1_DEV
998-30147	3	IC,LIFUKA,B2,USB-C RETIMER,DEV,AXM,CSP154	UF000,UF100,UG000	CRITICAL	RT13:B2_DEV

ACE3

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S03133	3	IC,SN2012025,ACE3,A0,USB,PD	UF400,UF500,UG400	CRITICAL	USBCPC:ACE3_A0
353S03508	3	IC,SN2012025,ACE3,A1,USBPD,20HV	UF400,UF500,UG400	CRITICAL	USBCPC:ACE3_A1

U5500 APN 353S03508 in CSA55

EUSB level shifter-MACAW

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-26778	3	IC,MACAW,CYUSB2405,A2,CSP24	UF600,UF650,UG650	CRITICAL	MACAW:A2
338S00908	3	IC,MACAW,CYUSB2406,A3,CSP24	UF600,UF650,UG650	CRITICAL	MACAW:A3

Re-timer ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00574	3	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190,UG090	CRITICAL	ATCRTMR_ROM:WINBOND
335S00575	3	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190,UG090	CRITICAL	ATCRTMR_ROM:MACRONIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00575	335S00574	ALT_CMN	ALL	<RDAR://82686160>
335S00596	335S00574	ALT_CMN	ALL	<rdar://106960679>

335S00574 is approved per this slack
https://a1391194.slack.com/archives/G01S9AWHZT7/p1659569482647089

Programmble ACE ROMs NO LONGER NEEDED IN X2681 CURRENT BOM
ALWAYS USING BLANK PARTS//NOT FOR P1BU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00644	3	ROM,X2371	UF260,UG260,U5660	CRITICAL	ACE3_ROM_NOATC1ROM:BLANK
335S00644	4	ROM,X2371	UF250,UF260,UG260,U5660	CRITICAL	ACE3_ROM_YESATC1ROM:BLANK

UF250 removed per rdar://105021838 (EVTs: Switch to shared ROM for ATC0 and ATC1)

ACE BOM BLANK ALT parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00537	335S00644	ACE3_ROM_YESATC1ROM:BLANK	UF250,UF260,UG260,U5660	
335S00571	335S00644	ACE3_ROM_YESATC1ROM:BLANK	UF250,UF260,UG260,U5660	rdar:82361417
335S00537	335S00644	ACE3_ROM_NOATC1ROM:BLANK	UF260,UG260,U5660	
335S00571	335S00644	ACE3_ROM_NOATC1ROM:BLANK	UF260,UG260,U5660	rdar:82361417

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S03251	353S4037	ALT_CMN	ALL	<RDAR://95333221>
353S03294	353S4037	ALT_CMN	ALL	<RDAR://95333221>
353S00636	353S4037	ALT_CMN	ALL	<RDAR://95333221>

<--UF490 01/04/23

NAND PARTS

P2 update per Yash's box file in email of on 11/30/2022

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00551	4	NAND,BC5T,128GB,S5E,11.0,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:KX-512
335S00619	4	NAND,BC5T,128GB,S5E,11.0,512G,W,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-512
335S00552	4	NAND,BC5T,256GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-1TB_old
335S00581	4	NAND,3DV7T,256GB,S5E,XX.X,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-1TB
335S00652	4	NAND,BICS5,256GB,S5E,XX.X,512G,K,SLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-1TB_new
335S00553	4	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-2TB_old
335S00583	4	NAND,3DV7T,512GB,S5E,17.0,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-2TB
335S00653	4	NAND,BICS5,512GB,S5E,XX.X,512G,K,SLGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-2TB_new
335S00643	4	NAND,BC5T,1TB,S5E,XX.X,512G,K,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-4TB
335S00610	4	NAND,3DV7T,1TB,S5E,17.0,512G,H,ULGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-4TB

NAND SOCKET stale removed 09/13/2022

06/03/2022

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SOC-DEV/SOCKET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-13908	1	PCBA,LONGMEN,X2681	U0600	CRITICAL	SOC:SOCKET

SOC-B0

Binning
Bin 1: 6PCPU,18FSTP (Low Power) - non-harvested parts
Bin 2: 6PCPU,18FSTP (High Power) - harvested/downbinned
Bin 2: SYS CONFIG-5PCPU,14FSTP
Bin 5: 5-6PCPU,16-18 FSTP (GFX Harv, PCPU Harv) - harvested/downbinned
Bin 5: SYS CONFIG-5PCPU,14FSTP

rdar://110924968 (DVT2s Set Lobos B1 APNs as primary, add B0 APNs as alts)

BIN1

998-32451	1	SOC,LOBOS SOC,LOBOS B1+36G,1A,BIN1,LP,AX,M,B2647	U0600	CRITICAL	SOC:6C_18FSTP_36G

B1 36G MICRON BIN1

Bin1 =6C, 18FSTP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-32452	998-32451	ANY	ALL	B1 36G BIN1 HYNIX	B1 Bin1 HYNIX ALT
998-31193	998-32451	ANY	ALL	B0 36G BIN1 HYNIX	B0 Bin1 HYNIX ALT
998-31191	998-32451	ANY	ALL	B0 36G BIN1 MICRON	B0 Bin1 MICRON ALT

998-32449	1	SOC,LOBOS SOC,LOBOS B1+18G,1A,BIN1,LP,AX,M,B2647	U0600	CRITICAL	SOC:6C_18FSTP_18G

B1 18G MICRON BIN1

Bin1 =6C, 18FSTP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-32450	998-32449	ANY	ALL	B1 18G BIN1 HYNIX	B1 Bin1 HYNIX ALT
998-31192	998-32449	ANY	ALL	B0 18G BIN1 HYNIX	B0 Bin1 HYNIX ALT
998-31190	998-32449	ANY	ALL	B0 18G BIN1 HYNIX	B0 Bin1 MICRON ALT

BIN5

Bin5 =5C, 14FSTP

998-32459	1	SOC,LOBOS SOC,LOBOS B1+36G,1A,BIN5,AX,M,B2647	U0600	CRITICAL	SOC:5C_14FSTP_36G

B1 36G MICRON BIN5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-31207	998-32459	ANY	ALL	B0 36G BIN5 MICRON	B0 BIN5 MICRON ALT
998-31209	998-32459	ANY	ALL	B0 36G BIN5 HYNIX	B0 BIN5 HYNIX ALT
998-31195	998-32459	ANY	ALL	B0 36G BIN2 MICRON	B0 BIN2 MICRON ALT
998-31197	998-32459	ANY	ALL	B0 36G BIN2 HYNIX	B0 BIN2 HYNIX ALT
998-31191	998-32459	ANY	ALL	B0 36G BIN1 MICRON	B0 BIN1 MICRON ALT
998-31193	998-32459	ANY	ALL	B0 36G BIN1 HYNIX	B0 BIN1 HYNIX ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-32460	998-32459	ANY	ALL	B1 36G BIN5 HYNIX	B1 BIN5 HYNIX ALT
998-32455	998-32459	ANY	ALL	B1 36G BIN2 MICRON	B1 BIN2 MICRON ALT
998-32456	998-32459	ANY	ALL	B1 36G BIN2 HYNIX	B1 BIN2 HYNIX ALT
998-32451	998-32459	ANY	ALL	B1 36G BIN1 MICRON	B1 BIN1 MICRON ALT
998-32452	998-32459	ANY	ALL	B1 36G BIN1 HYNIX	B1 BIN1 HYNIX ALT

BIN5

Bin5 =5C, 14FSTP

998-32457	1	SOC,LOBOS SOC,LOBOS B1+18G,1A,BIN5,AX,M,B2647	U0600	CRITICAL	SOC:5C_14FSTP_18G

B1 18G MICRON BIN5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-31206	998-32457	ANY	ALL	B0 18G BIN5 MICRON	B0 BIN5 MICRON ALT
998-31208	998-32457	ANY	ALL	B0 18G BIN5 HYNIX	B0 BIN5 HYNIX ALT
998-31194	998-32457	ANY	ALL	B0 18G BIN2 MICRON	B0 BIN2 MICRON ALT
998-31196	998-32457	ANY	ALL	B0 18G BIN2 HYNIX	B0 BIN2 HYNIX ALT
998-31190	998-32457	ANY	ALL	B0 18G BIN1 MICRON	B0 BIN1 MICRON ALT
998-31192	998-32457	ANY	ALL	B0 18G BIN1 HYNIX	B0 BIN1 HYNIX ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-32458	998-32457	ANY	ALL	B1 18G BIN5 HYNIX	B1 BIN5 HYNIX ALT
998-32453	998-32457	ANY	ALL	B1 18G BIN2 MICRON	B1 BIN2 MICRON ALT
998-32454	998-32457	ANY	ALL	B1 18G BIN2 HYNIX	B1 BIN2 HYNIX ALT
998-32449	998-32457	ANY	ALL	B1 18G BIN1 MICRON	B1 BIN1 MICRON ALT
998-32450	998-32457	ANY	ALL	B1 18G BIN1 HYNIX	B1 BIN1 HYNIX ALT

SPI IPD CS L SERIES SOURCE TERMINATION RESISTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S00073	2	RES,TK,0 OHM,1A MAX,1/20W,0201	RT36B,RT352	IPD_SPI_CS_R:0_OHM
117S00113	2	RES,TK,20 OHM,5%,1/20W,0201	RT36B,RT352	IPD_SPI_CS_R:20_OHM
117S00122	2	RES,TK,33 OHM,5%,1/20W,0201	RT36B,RT352	IPD_SPI_CS_R:33_OHM

BOMOPTION=TPAD_SOC_PULLUP:<30K/47K>

USE BOM_OPTION TO SELECT BETWEEN 30K OR 47K PULL-UPS THAT TIE TO SOC PINS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S00521	4	RES,TK,30K OHM,1%,1/20W,0201	RT350,RT363,RT341,RT371	TPAD_SOC_PULLUP:30K
117S00129	4	RES,TK,47K OHM,5%,1/20W,0201	RT350,RT363,RT341,RT371	TPAD_SOC_PULLUP:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RT333	UT330BOMYES

U1910

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00574	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4x4MM,SON8	U1910	CRITICAL	

JUNO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00939	1	IC,EOS SN300V,B20,DEV,Y50,WLCSP79	U5000	CRITICAL	EOS:B20_DEV
338S00941	1	IC,JUNO,SE310S,A0,DEV,10C,WLCSP42	U5000	CRITICAL	JUNO:A0_DEV
338S00956	1	IC,JUNO,SE310S,A0,PROD,1PB,WLCSP42	U5000	CRITICAL	JUNO:A0_POR

338S01013	338S00956	ALT_CMN	ALL	<rdar://110035277>

HDMI COBRA

CSA170

OCARINA 0/1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN400	CRITICAL	OCARINA0:A0_OTPBC

BLACK

GREY

SD CARD CONNECTOR BOM OPTIONS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-00196	1	CONN,RCPT,BLK,SD,X1982	JK600	CRITICAL	

TAWANG BOM OPTIONS

rdar://103327171

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S03375	6	IC,TAWANG,SPKR AMP,CLASS-D,B0,CSP30	UR600,UR630,UR640,UR700,UR730,UR760	CRITICAL	

PBUS CAPS not call C5210

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COMMON BOM GROUPS

BOM GROUP	BOM OPTIONS
X2681_COMMON	SCH,PCB,COMMON,ALT_CMN,ALTERNATE:INSTANCE,X2681_COMMON1,X2681_COMMON2,X2681_BLC,X2681_JUNO,X2681_FAN,X2681_HDMI,X2681_IMU,X2681_PROGPARTS,X2681_PWR,X2681_SOC,X2681_TPAD,X2681_USBC
X2681_COMMON1	BOARD_ID,BOARD_REV:0100,BOOTCFG1,BOOTCFG2
X2681_COMMON2	REFSECDIS_SOC_PU:30K,RF_CONN,STFNR
X2681_PROGPARTS	ACE3_ROM_YESATC1ROM:BLANK,ATCRTMR_ROM:WINBOND,HDMI_ROM:512
X2681_BATT	ACEFWDB:POR
X2681_BLC	BLC_BEN_IC:V4,BLC_5V_SERIES:10_OHM,BLC_5V_CAP:4P7_UF
X2681_FAN	
X2681_HDMI	COBRA-A1_CGF2,COBRAPART:0,DATA_FILT,HDMI_CL_FILT:YES,HDMI_CEC_FET:NO,LDO_HDMI:5V,HDMICONN:PORTABLES_14_BTN2
X2681_IMU	REFIMU_IC:BMI286,REFIMU_RE400:30K
X2681_JUNO	JUNO:A0_POR
X2681_SOC	DEV_DFU:TADFU,SE_IRQ,SEPROM_1V8:SYS
X2681_TPAD	IPD_SPI_CS_R:20_OHM,TPAD_SOC_PULLUP:30K
X2681_USBC	ACE3:20V,ATC0_ROM_ONLY:NO,MACAW:A3,RT13:B2_DEV,SYS_BOOT_PWR:DISABLED,STRAP2_LS:NO,USBCPC:ACE3_A1
X2681_PWR	P5VUSB_DSCHG,X2681_BATT,X2681_CHAPEL,X2681_ICEMAN_HP,X2681_MANDOLA,X2681_SPLITFIRE
X2681_CHAPEL	CHAPEL_PORTABLES,SOC:S
X2681_ICEMAN_HP	P3V8AON_IC:A2_BOM2_R0C1,P3V8AON_LPM,P3V8ILIM:BOM2_5V
X2681_MANDOLA	3V8_DLY:YES,MANDOLA_IC:3A,MANDOLA_R_C
X2681_SPLITFIRE	
X2681_PVT	LFKA_TEST_MODE:NO,USBC_DUAL_DFU:NO,USBC_DUAL_KIS:NO,VITAMIN-C:NO

DEV BOM GROUPS

BOM GROUP	BOM OPTIONS
X2681_DEVEL:ENG	ALTERNATE:INSTANCE,ALT_CMN,BATT_DBG,DBG_BTN,DBG_LED,DEV_IPD,HDMI_DEBUG_CONN:YES,SNSRES_DEV,USBC_DBG,LFKA_TEST_MODE:YES,USBC_DUAL_DFU:YES,USBC_DUAL_KIS:YES,VITAMIN-C:YES

BOARD REV BOM

PD resistors

	BOM GROUP	BOM OPTIONS	
	BOARD_REV:1111		
	BOARD_REV:1110	BOARDREV0	
	BOARD_REV:1101	BOARDREV1	
1010	BOARD_REV:0101	BOARDREV3,BOARDREV1	
1011	BOARD_REV:0100	BOARDREV3,BOARDREV1,BOARDREV0	DVT2s build rev4 board
1100	BOARD_REV:0011	BOARDREV3,BOARDREV2	EVTs build rev3 board
1101	BOARD_REV:0010	BOARDREV3,BOARDREV2,BOARDREV0	P2s build rev2 board
1110	BOARD_REV:0001	BOARDREV3,BOARDREV2,BOARDREV1	P1s build rev1 board
1111	BOARD_REV:0000	BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0	P1BUs build rev1 board

BOARD ID

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARDID2

For X2461 use BOARD_ID[7:0] = 00000100
rdar://95401385 (X2461 MLB Set board ID to "00000100")

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00478	COMMON BOM,MLB-S,X2681	X2681_COMMON
985-01983	DEV BOM,MLB-S,X2681	X2681_DEVEL:ENG
985-02118	DEV BOM (SPECIAL CONFIG),MLB-C,X2681	X2681_PVT

Variable BOM Groups/Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00478	1	COMMON BOM,MLB-S,X2681	BASE	CRITICAL	BASE_BOM
985-01983	1	DEV BOM,MLB-S,X2681	DEVEL	CRITICAL	DEVEL_BOM

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
SSD:NOS5E	LND_4_BOM,OCARINA0:A0_OTPBC
SSD:512GB_KX	LND_4_BOM,NAND:KX-512,OCARINA0:A0_OTPBC
SSD:512GB_WD	LND_4_BOM,NAND:WD-512,OCARINA0:A0_OTPBC
SSD:1TB_HY	LND_4_BOM,NAND:HY-1TB,OCARINA0:A0_OTPBC
SSD:1TB_KX_old	LND_4_BOM,NAND:TS-1TB_old,OCARINA0:A0_OTPBC
SSD:1TB_KX_new	LND_4_BOM,NAND:TS-1TB_new,OCARINA0:A0_OTPBC
SSD:2TB_HY	LND_4_BOM,NAND:HY-2TB,OCARINA0:A0_OTPBC
SSD:2TB_KX_old	LND_4_BOM,NAND:TS-2TB_old,OCARINA0:A0_OTPBC
SSD:2TB_KX_new	LND_4_BOM,NAND:TS-2TB_new,OCARINA0:A0_OTPBC
SSD:4TB_HY	LND_4_BOM,NAND:HY-4TB,OCARINA0:A0_OTPBC
SSD:4TB_KX	LND_4_BOM,NAND:TS-4TB,OCARINA0:A0_OTPBC

SSD 685 BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00535	COMMON BOM,SSD_2_LAND,MLB-C,X2681	ALT_CMN,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L2
685-00536	COMMON BOM,SSD_4_LAND,MLB-C,X2681	ALT_CMN,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L4

SSD Variable BOM Groups/Development

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00535	1	SSD PARTS,SSD_2_LAND,MLB-C,X2681	SSD	CRITICAL	LND_2_BOM
685-00536	1	SSD PARTS,SSD_4_LAND,MLB-C,X2681	SSD	CRITICAL	LND_4_BOM

SSD Support BOM Groups

BOM GROUP	Host BOM	BOM OPTIONS
SSD_SUPPORT:L1-L2	2L Support BOM	SSD_2L
SSD_SUPPORT:L1-L4	4L Support BOM	SSD_2L,SSD_4L,SSD_BRANCH_2L

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BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS
939-14735	PCBA,MLB-C,DCDC-1,SOC SOCKET,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:SOCKET,SSD:NOSSE
939-14736	PCBA,MLB-C,DCDC-2,NO SOC SOCKET,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SSD:NOSSE

BOM VARIANT TABLES-DCDC

5C,14FSTPFSTP,18G

639-17902	MLB_S,5C,14FSTP,18G,512G_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:512GB_KX
639-18407	MLB_S,5C,14FSTP,18G,512G_WD,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:512GB_WD
639-18213	MLB_S,5C,14FSTP,18G,1TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:1TB_HY
639-18214	MLB_S,5C,14FSTP,18G,1TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:1TB_KX_old
639-19452	MLB_S,5C,14FSTP,18G,1TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:1TB_KX_new
639-18219	MLB_S,5C,14FSTP,18G,2TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:2TB_HY
639-18220	MLB_S,5C,14FSTP,18G,2TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:2TB_KX_old
639-19456	MLB_S,5C,14FSTP,18G,2TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:2TB_KX_new
639-18409	MLB_S,5C,14FSTP,18G,4TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:4TB_HY
639-18223	MLB_S,5C,14FSTP,18G,4TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_18G,SSD:4TB_KX
639-18212	MLB_S,5C,14FSTP,36G,512G_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:512GB_KX
639-18408	MLB_S,5C,14FSTP,36G,512G_WD,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:512GB_WD
639-18216	MLB_S,5C,14FSTP,36G,1TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:1TB_HY
639-18217	MLB_S,5C,14FSTP,36G,1TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:1TB_KX_old
639-19454	MLB_S,5C,14FSTP,36G,1TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:1TB_KX_new
639-18221	MLB_S,5C,14FSTP,36G,2TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:2TB_HY
639-18222	MLB_S,5C,14FSTP,36G,2TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:2TB_KX_old
639-19458	MLB_S,5C,14FSTP,36G,2TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:2TB_KX_new
639-18410	MLB_S,5C,14FSTP,36G,4TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:4TB_HY
639-18225	MLB_S,5C,14FSTP,36G,4TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:5C_14FSTP_36G,SSD:4TB_KX

6C,18FSTPFSTP

639-18228	MLB_S,6C,18FSTP,18G,512G_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:512GB_KX
639-18411	MLB_S,6C,18FSTP,18G,512G_WD,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:512GB_WD
639-18230	MLB_S,6C,18FSTP,18G,1TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:1TB_HY
639-18231	MLB_S,6C,18FSTP,18G,1TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:1TB_KX_old
639-19453	MLB_S,6C,18FSTP,18G,1TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:1TB_KX_new
639-18236	MLB_S,6C,18FSTP,18G,2TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:2TB_HY
639-18237	MLB_S,6C,18FSTP,18G,2TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:2TB_KX_old
639-19457	MLB_S,6C,18FSTP,18G,2TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:2TB_KX_new
639-18413	MLB_S,6C,18FSTP,18G,4TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:4TB_HY
639-18240	MLB_S,6C,18FSTP,18G,4TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_18G,SSD:4TB_KX
639-18244	MLB_S,6C,18FSTP,36G,512G_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:512GB_KX
639-18412	MLB_S,6C,18FSTP,36G,512G_WD,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:512GB_WD
639-18233	MLB_S,6C,18FSTP,36G,1TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:1TB_HY
639-18234	MLB_S,6C,18FSTP,36G,1TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:1TB_KX_old
639-19455	MLB_S,6C,18FSTP,36G,1TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:1TB_KX_new
639-18238	MLB_S,6C,18FSTP,36G,2TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:2TB_HY
639-18239	MLB_S,6C,18FSTP,36G,2TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:2TB_KX_old
639-19459	MLB_S,6C,18FSTP,36G,2TB_KX_new,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:2TB_KX_new
639-18414	MLB_S,6C,18FSTP,36G,4TB_HY,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:4TB_HY
639-18242	MLB_S,6C,18FSTP,36G,4TB_KX,X2681	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C_18FSTP_36G,SSD:4TB_KX

SYNC_MASTER=X2681_* SYNC_DATE=09/30/2022

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BOM VARIANT TABLES

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BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS

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BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS

BOM VARIANT TABLES-P1,P2

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SYSTEM EE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1080	376S0820	ALT_CMN	ALL	<RDAR://57125638>	
107S0276	107S00020	ALT_CMN	ALL	<RDAR://57126636>	
311S00176	311S00153	ALT_CMN	ALL	<RDAR://57133089>	
353S02030	353S01993	ALT_CMN	ALL	<RDAR://57133661>	
138S00284	138S00136	ALT_CMN	ALL	<RDAR://57134599>	
138S0852	138S0818	ALT_CMN	ALL	<RDAR://57137990>	
138S0750	138S00097	ALT_CMN	ALL	<RDAR://57138474>	
152S00864	152S00851	ALT_CMN	ALL	<RDAR://57159654>	
138S00181	138S0835	ALT_CMN	ALL	<RDAR://57161300>	
138S00291	138S0835	ALT_CMN	ALL	<RDAR://57161300>	
311S00392	311S00129	ALT_CMN	ALL	<RDAR://106781111>	<-UT360 03/17/23
311S00060	311S0273	ALT_CMN	ALL	<RDAR://57172430>	
353S00878	353S00599	ALT_CMN	ALL	<RDAR://57173083>	
371S00220	371S00181	ALT_CMN	ALL	<RDAR://57196734>	
377S0155	377S0184	ALT_CMN	ALL	<RDAR://57230484>	
353S00852	353S4262	ALT_CMN	ALL	<RDAR://57244062>	
155S00648	155S00647	ALT_CMN	ALL	<RDAR://62952600>	
311S00267	311S00244	ALT_CMN	ALL	<RDAR://63954135>	<-UD010 etc 06/08/20
311S00277	311S00276	ALT_CMN	ALL	<RDAR://63847960>	<-UF720 etc 06/09/20
311S00268	311S00246	ALT_CMN	ALL	<RDAR://64048104>	<-U2240 etc 06/10/20
740S00081	740S00053	ALT_CMN	ALL	<RDAR://64196298>	<-FS601 etc 06/23/20
138S00049	138S0831	ALT_CMN	ALL	<RDAR://65054474>	<-CD511 etc 07/21/20
376S00292	376S1140	ALT_CMN	ALL	<RDAR://64911019>	<-QW700 07/21/20
377S00165	377S00031	ALT_CMN	ALL	<RDAR://64912351>	<-DZF664 etc 07/21/20
371S00085	371S00190	ALT_CMN	ALL	<RDAR://64913950>	<-D5401 etc 07/21/20
128S00058	128S00098	ALT_CMN	ALL	<RDAR://65152442>	<-CKB03 etc 07/22/20
128S00105	128S00098	ALT_CMN	ALL	<RDAR://65152442>	<-CKB03 etc 07/22/20
132S00176	132S0640	ALT_CMN	ALL	<RDAR://65054857>	<-CS222 etc 08/25/20
138S00104	138S0978	ALT_CMN	ALL	<RDAR://65054612>	<-CT623 etc 08/25/20
155S00097	155S0664	ALT_CMN	ALL	<RDAR://102911599>	<-FLT600 etc 08/25/20
311S00300	311S0671	ALT_CMN	ALL	<RDAR://65005395>	<-UA600 etc 08/25/20
128S00119	128S00016	ALT_CMN	ALL	<RDAR://81123919>	<-CPB30-CPB33 07/27/21
152S01787	152S00285	ALT_CMN	ALL	<RDAR://98832166>	<-LP800 09/27/20
107S00041	107S00039	ALT_CMN	ALL	<RDAR://64239446>	<-R9450 etc 09/29/20
107S00365	107S00373	ALT_CMN	ALL	<RDAR://64240698>	<-R5800 09/29/20
197S0588	197S0591	ALT_CMN	ALL	<RDAR://65008394>	<-Y0600 09/29/20
197S0590	197S0591	ALT_CMN	ALL	<RDAR://65008394>	<-Y0600 09/29/20
376S00036	376S00328	ALT_CMN	ALL	<RDAR://95800222>	<-Q5820 07/19/22
107S00443	107S00005	ALT_CMN	ALL	<RDAR://98860549>	<-RD591 08/19/22
128S00069	128S00094	ALT_CMN	ALL	<RDAR://98083158>	<-CS890 etc 08/22/22
128S00131	128S00094	ALT_CMN	ALL	<RDAR://98083158>	<-CS890 etc 08/22/22
376S00605	376S00489	ALT_CMN	ALL	<RDAR://99007701>	<-U5230 etc 08/22/22
353S02789	353S3021	ALT_CMN	ALL	<RDAR://98080817>	<-U6030 08/30/22
107S00492	107S00234	ALT_CMN	ALL	<RDAR://98082467>	<-RD691etc 09/01/22
376S00618	376S00544	ALT_CMN	ALL	<RDAR://101229139>	<-Q5178etc 10/11/22
376S00516	376S00544	ALT_CMN	ALL	<RDAR://101229139>	<-Q5178etc 10/17/22
371S00370	371S00062	ALT_CMN	ALL	<RDAR://101818762>	<-D5340etc 12/07/22
353S02175	353S00882	ALT_CMN	ALL	<RDAR://1017777653>	<-UH901 12/07/22
518S00311	518S0818	ALT_CMN	ALL	<RDAR://102913554>	<-JE500 etc 12/07/22
107S00057	107S00100	ALT_CMN	ALL	<RDAR://103036991>	<-RD761 12/08/22
107S00440	107S00062	ALT_CMN	ALL	<RDAR://103037200>	<-RD964 etc 12/08/22
107S0150	107S00460	ALT_CMN	ALL	<RDAR://103037486>	<-RE100 etc 12/16/22
107S00298	107S00460	ALT_CMN	ALL	<RDAR://103037486>	<-RE100 etc 12/16/22
107S00474	107S00017	ALT_CMN	ALL	<RDAR://103037883>	<-RD863 12/29/22
311S0460	311S0449	ALT_CMN	ALL	<RDAR://102833457>	<-U5340 etc 12/09/22
311S00405	311S0665	ALT_CMN	ALL	<RDAR://99158863>	<-UT101 etc 12/09/22
353S02624	353S01595	ALT_CMN	ALL	<RDAR://1018184l3>	<-U6040 12/16/22
377S00210	377S00172	ALT_CMN	ALL	<RDAR://101782110>	<-D5402 12/20/22
376S00466	376S00463	ALT_CMN	ALL	<RDAR://101782379>	<-Q0520 12/20/22
377S00186	377S00060	ALT_CMN	ALL	<RDAR://101782315>	<-DZE766 etc 12/20/22
138S00124	138S00123	ALT_CMN	ALL	<RDAR://101827436>	<-CF406 etc 12/20/22
377S00201	377S00240	ALT_CMN	ALL	<RDAR://97047667>	<-D5403 12/20/22
155S00867	155S0644	ALT_CMN	ALL	<RDAR://1029111061>	<-L3507 12/22/22
155S00885	155S00188	ALT_CMN	ALL	<RDAR://101364618>	<-FLE400 etc 12/20/22

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
107S00150	107S0208	ALT_CMN	ALL	<RDAR://64240900>	<-RE100 etc 09/30/20
377S00166	377S00160	ALT_CMN	ALL	<RDAR://64047267>	<-DZF660 etc 09/30/20
138S00343	138S00329	ALT_CMN	ALL	<RDAR://64426303>	<-C3502 etc 09/30/20
138S00330	138S00081	ALT_CMN	ALL	<RDAR://64425937>	<-C3175 etc 10/02/20
152S00182	152S00703	ALT_CMN	ALL	<RDAR://64456067>	<-LC260 10/02/20
107S00325	107S00232	ALT_CMN	ALL	<RDAR://64241500>	<-R5260 10/02/20
152S01410	152S01300	ALT_CMN	ALL	<RDAR://66866291>	<-LS820 etc 10/02/20
152S00785	152S00477	ALT_CMN	ALL	<RDAR://69846686>	<-LX810 10/02/20
371S00220	371S00307	ALT_CMN	ALL	<RDAR://69512996>	<-D5270 10/02/20
371S0602	371S00245	ALT_CMN	ALL	<RDAR://69900494>	<-D9400 10/02/20
740S0118	740S00028	ALT_CMN	ALL	<RDAR://61296520>	<-FS200 etc 10/02/20
138S0746	138S0705	ALT_CMN	ALL	<RDAR://65194305>	<-CG811 etc 10/02/20
138S0786	138S0705	ALT_CMN	ALL	<RDAR://65194305>	<-CG811 etc 10/02/20
311S0341	311S0536	ALT_CMN	ALL	<RDAR://64195790>	<-UH802 10/09/20
353S02407	353S02212	ALT_CMN	ALL	<RDAR://63861789>	<-UT620 10/09/20
311S00310	311S00306	ALT_CMN	ALL	<RDAR://69815717>	<-UF840 etc 10/14/20
152S00434	152S1829	ALT_CMN	ALL	<RDAR://69844024>	<-LT601 10/14/20
152S00199	152S00413	ALT_CMN	ALL	<RDAR://64480169>	<-LS230 10/14/20
152S01218	152S00413	ALT_CMN	ALL	<RDAR://64480169>	<-LS230 10/14/20
152S01037	152S00887	ALT_CMN	ALL	<RDAR://65153548>	<-L7801 etc 10/14/20
152S01070	152S00887	ALT_CMN	ALL	<RDAR://65153548>	<-L7801 etc 10/14/20
335S00500	335S00494	ALT_CMN	ALL	<RDAR://68784220>	<-U2010 11/17/20
353S02635	353S02395	ALT_CMN	ALL	<RDAR://69166162>	<-UF015 etc 11/18/20
353S01792	353S3901	ALT_CMN	ALL	<RDAR://68820723>	<-U6041 01/05/21
107S0255	107S0240	ALT_CMN	ALL	<RDAR://71994260>	<-RD590 01/05/21
371S00322	371S00047	ALT_CMN	ALL	<RDAR://70069054>	<-DH612 etc 01/05/21
311S00322	311S00321	ALT_CMN	ALL	<RDAR://83225248>	<-UT340 etc 09/17/21
107S00491	107S00061	ALT_CMN	ALL	<RDAR://82693585>	<-RD702 etc 09/24/21
138S00416	138S00328	ALT_CMN	ALL	<RDAR://82683097>	<-C2300 etc 09/24/21
353S03084	353S02407	ALT_CMN	ALL	<RDAR://93197792>	<-UT620 05/12/22
353S02897	353S1429	ALT_CMN	ALL	<RDAR://97641038>	<-U8150 etc 08/01/22
353S02402	353S1429	ALT_CMN	ALL	<RDAR://97641038>	<-U8150 etc 08/01/22
377S00223	377S00040	ALT_CMN	ALL	<RDAR://98409160>	<-U5150 09/01/22
138S00148	138S00149	ALT_CMN	ALL	<RDAR://98081681>	<-CF030 etc 09/01/22
138S00151	138S00149	ALT_CMN	ALL	<RDAR://98081681>	<-CF030 etc 09/01/22
138S00150	138S00149	ALT_CMN	ALL	<RDAR://98081681>	<-CF030 etc 09/01/22
377S00196	377S00185	ALT_CMN	ALL	<RDAR://91816792>	<-DZE600 etc 09/01/22
311S00405	311S0665	ALT_CMN	ALL	<RDAR://99158863>	<-UT101 etc 09/01/22
138S00450	138S0831	ALT_CMN	ALL	<RDAR://97804865>	<-CT618 etc 09/01/22
353S02434	353S3332	ALT_CMN	ALL	<RDAR://98078261>	<-U7490 09/02/22
376S00631	376S0636	ALT_CMN	ALL	<RDAR://98409928>	<-QW501 09/02/22
376S00292	376S00294	ALT_CMN	ALL	<RDAR://101778232>	<-Q8700 12/09/22
376S00633	376S00294	ALT_CMN	ALL	<RDAR://101778232>	<-Q8700 12/09/22
376S00378	376S00324	ALT_CMN	ALL	<RDAR://1024438911>	<-Q5170 12/09/22
376S00383	376S00324	ALT_CMN	ALL	<RDAR://1024438911>	<-Q5170 12/09/22
155S00309	155S0831	ALT_CMN	ALL	<RDAR://1028886213>	<-FLM500 01/04/23
155S0830	155S0316	ALT_CMN	ALL	<RDAR://1028886155>	<-LX500 01/04/23
371S00325	371S00085	ALT_CMN	ALL	<RDAR://101778613>	<-DF400 etc 01/04/23

DISCHARGE FET ALT8 rdar://98349451

376S00647	376S00078	ALT_CMN	ALL	<RDAR://98349451>	<-QF910 etc 09/02/22
376S00634	376S00078	ALT_CMN	ALL	<RDAR://98349451>	<-QF910 etc 09/02/22
376S00588	376S00078	ALT_CMN	ALL	<RDAR://98349451>	<-QF910 etc 09/02/22
376S00647	376S00074	ALT_CMN	ALL	<RDAR://98349451>	<-QC280 etc 09/02/22
376S00634	376S00074	ALT_CMN	ALL	<RDAR://98349451>	<-QC280 etc 09/02/22
376S00078	376S00074	ALT_CMN	ALL	<RDAR://98349451>	<-QC280 etc 09/02/22
376S00588	376S00074	ALT_CMN	ALL	<RDAR://98349451>	<-QC280 etc 09/02/22
376S00332	376S00074	ALT_CMN	ALL	<RDAR://98349451>	<-QC280 etc 09/02/22
376S00647	376S00588	ALT_CMN	ALL	<RDAR://98349451>	<-QH900 etc 09/02/22
376S00634	376S00588	ALT_CMN	ALL	<RDAR://98349451>	<-QH900 etc 09/02/22
376S00557	376S00282	ALT_CMN	ALL	<RDAR://103541578>	<-QS155 12/29/22

DCDC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S0863	138S0853	ALT_CMN	ALL	<RDAR://56380033>	
152S00963	152S00885	ALT_CMN	ALL	<RDAR://56380033>	
138S00047	138S00073	ALT_CMN	ALL	<RDAR://56380033>	
107S00373	107S00365	ALT_CMN	ALL	<RDAR://56380033>	
128S00026	128S00011	ALT_CMN	ALL	<RDAR://56380033>	
128S00087	128S00011	ALT_CMN	ALL	<RDAR://56380033>	
128S00031	128S00011	ALT_CMN	ALL	<RDAR://56380033>	
128S00039	128S00038	ALT_CMN	ALL	<RDAR://56380033>	<-C etc 06/23/20
128S0364	128S0264	ALT_CMN	ALL	<RDAR://56380033>	
152S00383	152S00680	ALT_CMN	ALL	<RDAR://56380033>	
376S00303	376S00012	ALT_CMN	ALL	<RDAR://56380033>	
376S00227	376S00203	ALT_CMN	ALL	<RDAR://56380033>	
376S00228	376S1179	ALT_CMN	ALL	<RDAR://56380033>	
138S0789	138S0941	ALT_CMN	ALL	<RDAR://56380033>	
138S00332	138S00328	ALT_CMN	ALL	<RDAR://57328643>	
152S00343	152S00839	ALT_CMN	ALL	<RDAR://57238826>	
152S01090	152S01085	ALT_CMN	ALL	<RDAR://57230783>	
376S00321	376S00397	ALT_CMN	ALL	<RDAR://>	<-Q5801 etc 11/18/21
107S00015	107S00011	ALT_CMN	ALL	<RDAR://68783358>	<-RC503 etc 11/18/21
107S00493	107S00056	ALT_CMN	ALL	<RDAR://98860242>	<-R5820 08/22/22
128S00106	128S00107	ALT_CMN	ALL	<RDAR://95642408>	<-C5250 etc 08/01/22
128S00110	128S00107	ALT_CMN	ALL	<RDAR://95642408>	<-C5250 etc 08/01/22
376S00036	376S00328	ALT_CMN	ALL	<RDAR://95800171>	<-Q5820 etc 08/02/22
376S00627	376S00328	ALT_CMN	ALL	<RDAR://95800171>	<-Q5820 etc 08/02/22
128S00132	128S00011	ALT_CMN	ALL	<RDAR://100435028>	<-C5201 etc 10/06/22
132S00412	132S00195	ALT_CMN	ALL	<RDAR://101823767>	<-C7774 etc 12/09/22
138S00396	138S00392	ALT_CMN	ALL	<RDAR://102387306>	<-C2350 etc 12/09/22
138S00437	138S00392	ALT_CMN	ALL	<RDAR://102387306>	<-C2350 etc 12/09/22
138S00458	138S00392	ALT_CMN	ALL	<RDAR://102387306>	<-C2350 etc 12/09/22
131S00691	131S00365	ALT_CMN	ALL	<RDAR://101827871>	<-C5373 12/09/22
138S00385	138S00377	ALT_CMN	ALL	<RDAR://1013157291>	<-C9430 etc 12/20/22
138S00457	138S00377	ALT_CMN	ALL	<RDAR://1013157291>	<-C9430 etc 12/20/22

rdar://99660774 (X2681 BOM ALT APNs update P1BU)

376S00614	376S0761	ALT_CMN	ALL	<RDAR://99660774>	<-Q5265 09/07/22
376S00600	376S0761	ALT_CMN	ALL	<RDAR://99660774>	<-Q5265 09/07/22
152S00199	152S01218	ALT_CMN	ALL	<RDAR://99660774>	<-LS230 09/07/22
107S00475	107S00044	ALT_CMN	ALL	<RDAR://99660774>	<-R5220 09/07/22
107S00076	107S00044	ALT_CMN	ALL	<RDAR://64238973>	<-R5220 etc 09/07/22
152S01789	152S00265	ALT_CMN	ALL	<RDAR://98418505>	<-LS800 09/07/22
371S00385	371S0602	ALT_CMN	ALL	<RDAR://98805110>	<-D9500 etc 08/22/22
152S01431	152S01413	ALT_CMN	ALL	<RDAR://99660774>	<-L9410 09/07/22
998-26284	152S01651	ALT_CMN	ALL	<RDAR://99660774>	<-L9401 09/07/22
152S00343	152S01325	ALT_CMN	ALL	<RDAR://99660774>	<-L7830 etc 09/08/22
152S01780	152S00238	ALT_CMN	ALL	<RDAR://99660774>	<-LN480 09/07/22
152S00991	152S00984	ALT_CMN	ALL	<RDAR://99660774>	<-LF900 etc 09/07/22
152S01788	152S00182	ALT_CMN	ALL	<RDAR://99660774>	<-LC260 09/07/22
152S01789	152S00265	ALT_CMN	ALL	<RDAR://99660774>	<-LS800,LP800 09/07/22
152S01752	152S01692	ALT_CMN	ALL	<RDAR://99660774>	<-L9500 etc 09/09/22
152S01809	152S01512	ALT_CMN	ALL	<RDAR://99660774>	<-L9400 etc 10/06/22
152S01835	152S01826	ALT_CMN	ALL	<RDAR://102884306>	<-L9401 etc 12/14/22
152S01824	152S01826	ALT_CMN	ALL	<RDAR://102884306>	<-L9401 etc 12/14/22
152S01836	152S01268	ALT_CMN	ALL	<RDAR://1030769751>	<-L7801 etc 12/22/22
152S01837	152S01268	ALT_CMN	ALL	<RDAR://1030769751>	<-L7801 etc 12/22/22
152S01838	152S01268	ALT_CMN	ALL	<RDAR://1030769751>	<-L7801 etc 12/22/22
138S00460	138S00035	ALT_CMN	ALL	<RDAR://98805110>	<-C7778 12/20/22
138S00397	138S00035	ALT_CMN	ALL	<RDAR://99660774>	<-C7778 etc 09/08/22

X2681 SPECIAL

107S00494	107S00058	ALT_CMN	ALL	<RDAR://1030378111>	<-RD862 12/09/22
107S0251	107S0249	ALT_CMN	ALL	<RDAR://1030379711>	<-RD965 12/29/22

SSD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S01023	152S00384	ALT_CMN	ALL	<RDAR://64459385>	<-LN420 etc 07/21/20
138S00097	138S0750	ALT_CMN	ALL	<RDAR://65198749>	<-CN403 etc 09/29/20
152S01780	152S00238	ALT_CMN	ALL	<RDAR://98416933>	<-LN480 etc 08/30/22
152S01024	152S00386	ALT_CMN	ALL	<RDAR://69894838>	<-LN421 etc 10/02/20 <-LG800 etc 10/02/20
132S00064	132S0409	ALT_CMN	ALL	<RDAR://69816599>	<-CN402 etc 10/02/20
138S00139	138S00138	ALT_CMN	ALL	<RDAR://64426113>	<-CN045 etc 10/02/20
138S00164	138S00138	ALT_CMN	ALL	<RDAR://64426113>	<-CN045 etc 10/02/20
138S00280	138S00138	ALT_CMN	ALL	<RDAR://64426113>	<-CN045 etc 10/02/20
138S00229	138S00107	ALT_CMN	ALL	<RDAR://108500107>	<-CN010 etc 12/07/22
107S00297	107S00344	ALT_CMN	ALL	<RDAR://103037358>	<-RN402 etc 01/04/23

BLC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S00812	152S1701	ALT_CMN	ALL	<RDAR://55465318>	
371S00217	371S00079	ALT_CMN	ALL	<RDAR://55465318>	
371S00435	371S00079	ALT_CMN	ALL	<rdar://107274512>	<-DT000 04/19/23
138S00087	138S1086	ALT_CMN	ALL	<RDAR://55465318>	
138S00482	138S1086	ALT_CMN	ALL	<RDAR://103316741>	<-CT050 etc 12/15/22
376S00021	376S00263	ALT_CMN	ALL	<RDAR://72627423>	<-Q9800 etc 01/05/20
376S00328	376S00263	ALT_CMN	ALL	<RDAR://103534029>	<-Q9800 etc 12/20/22

new 01/05/2023

155S00737	155S0921	ALT_CMN	ALL	<RDAR://102885520>	<-FLM712 01/05/23
155S00754	155S00098	ALT_CMN	ALL	<RDAR://102886500>	<-FLM710 etc 01/05/23
311S00279	311S00285	ALT_CMN	ALL	<RDAR://101781346>	<-UH801 etc 01/09/23
197S00371	197S00375	ALT_CMN	ALL	<RDAR://101780769>	<-YH700 01/05/23
197S00374	197S00375	ALT_CMN	ALL	<RDAR://101780769>	<-YH700 01/05/23
353S03028	353S01211	ALT_CMN	ALL	<RDAR://101714817>	<-UH502 01/05/23
131S00213	131S0556	ALT_CMN	ALL	<RDAR://101823304>	<-CH910 01/12/23
377S0077	377S0183	ALT_CMN	ALL	<RDAR://101819719>	<-DZH505 01/12/23
138S00022	138S00020	ALT_CMN	ALL	<RDAR://101827649>	<-CH722 etc 01/12/23
138S0734	138S0838	ALT_CMN	ALL	<RDAR://101825609>	<-CH775 01/12/23
138S00167	138S00237	ALT_CMN	ALL	<RDAR://101825378>	<-CH917 etc 01/12/23
138S0772	138S00013	ALT_CMN	ALL	<RDAR://103040015>	<-CH914 01/12/23
116S00014	116S00044	ALT_CMN	ALL	<RDAR://103038044>	<-RH780 etc 01/12/23
311S00269	311S00234	ALT_CMN	ALL	<RDAR://101781138>	<-UH700 01/12/23

new 03/14/2023 (EVT)

152S01836	152S01837	ALT_CMN	ALL	<RDAR://104334933>	<-L9411 03/14/23
152S01838	152S01837	ALT_CMN	ALL	<RDAR://104334933>	<-L9411 03/14/23
152S01461	152S01283	ALT_CMN	ALL	<rdar://108168179>	<-LL7800 etc 04/18/23
155S0660	155S0513	ALT_CMN	ALL	<rdar://107446684>	<-LR500 etc 04/19/23
138S1103	138S0719	ALT_CMN	ALL	<rdar://108281556>	<-CR510 04/19/23
107S00547	107S00478	ALT_CMN	ALL	<rdar://108011027>	<-RF911 etc 04/19/23
335S00603	335S0915	ALT_CMN	ALL	<rdar://107015500>	<-UH701 etc 04/19/23
138S00489	138S00488	ALT_CMN	ALL	<rdar://107156112>	<-CF420 etc 04/19/23
353S02787	353S01211	ALT_CMN	ALL	<rdar://104895648>	<-UH502 04/19/23
197S00318	197S00323	ALT_CMN	ALL	<rdar://108323962>	<-Q9355 04/20/23
197S00391	197S00323	ALT_CMN	ALL	<rdar://108323962>	<-Q9355 04/20/23

new 03/14/2023 (EVT)

155S0387	155S0694	ALT_CMN	ALL	<rdar://102885693>	<-LL501 etc 05/30/23
118S00827	117S00097	ALT_CMN	ALL	<rdar://108718018>	<-RR760 etc 05/30/23

PAGE TITLE

BOM ALTERNATES

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PACK OPTIONS

REF_SOC_H15S

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA10	LPDP_RX
CSA12	SDCARD

REF_CHARGER_MANDOLA_MP

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA52	PP_LX_BOT
CSA52	CHGR_PH_SNB
CSA53	3V8_DELAY:YES
	5V_DELAY:NO

REF_MAGSAFE_ACE3

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA55	USBC_DBG:IN
	UPC5_STRAP3:RPD

REF_VR_ICEMAN_HP

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA57	3V8_AON_I2C-DEV
CSA58	3V8_AON_RG402
	3V8_AON_RPH1_ORIG
	3V8_AON_RPH2_MIRR
	3V8_AON_RPH3_MIRR
CSA60	P3V8ILIM_MUX:Y
	3V8_AON_PBUS-18V

REF_PMU_CHAPEL_H15

PACK_OPTIONS TO INCLUDE IN NETLIST
SOC:S
FBUCK5:Y

REF_VR_SPITFIRE_EKARA_H15S

PACK_OPTIONS TO INCLUDE IN NETLIST

ipd / trackpad

	PACK_OPTIONS TO INCLUDE IN NETLIST
	IPD_RESETS_LS:PASS_THRU
	IPD_MCU_INT_WAKE_LS:X2SON_THK
CSA253	IPD_TOUCH_CLK_SRC:MLB
CSA253	IPD_PACK_MTP_FUNC1_FLEX:PULLDOWN

SPF_27UF STUFFING

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA128	SPF_27UF

REF_VR_5V_SN621371

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA122	5V_S2_PBUS-18V

REF_IMU_SOVEREIGN

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA144	REFIMU_TP:P5MM
CSA144	REFIMU_VDD:LCFILT
CSA144	REFIMU_TEST:YES

PACK_OPTIONS TO INCLUDE IN NETLIST
VDD1_DIRECT

PACK_OPTIONS TO INCLUDE IN NETLIST
ATC_VR_PG-RES

SPITFIRE/EKARA

PACK_OPTIONS TO INCLUDE IN NETLIST
L:2M4M
POLY_PBUS:18V

REF_USBC_LKFA_3PRT_ACE3

PACK_OPTIONS TO INCLUDE IN NETLIST
KEEP_SMALL_ARKANOID_CONN
ATC_BOUNDARYSCAN:YES
USBC_LAPTOP
PKGS:SMALL_PITCH
ACE2_SS_CAP
UPC1_ROM:YES
UPC1_UART_DEBUG
UPC1_UART_PD:NO
ATC01_VR_MLCC-REGULAR
ATC2_VR_MLCC-REGULAR
ATC_VR_DSCHG-EN-R:NO
ATC_RTMR_ROM:XSON
UPC_STRAP1_PD:NO
USBC_GATE_PACKAGE:SOT
LDCM:ENABLED
SOC_FORCE_DFU:YES
SOC_FORCE_DFU_YES:SOT
UPC2_STRAP4:NC
CHIP_ID_0X2

REF_USBC_VR_LT8642_1

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA158	5VUSBC01_THICKSTNCL
CSA158	5VUSBC01_PBUS-18V
CSA158	5VUSBC01_AND:PP

REF_USBC_VR_TPS62180

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA168	5VUSBC23_PBUS-18V

REF_HDMI_COBRA

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA175	HDMICONN:PORTABLES_14
CSA177	HDMI14UF:NORM
CSA178	HDMI2SOC:ATC3
CSA177	HDMICH744:THICK
	HDMI_DEBUG_CONN:YES

REF_SDCARD

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA198	SD_VR_3V3:THICKSTNCL

REF_WIRELESS_WILLAMETTE

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA201	3X_ANTENNA
CSA201	SUNWAY
	WLBT_TP_0P4

REF_STORAGE_S5E

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA224,CSA229	2V5_NAND_PBUS-B12-18V

REF_SPKRAMP_SN012776

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA246	SPKRAMP_A
CSA246	SPKRAMP_B
CSA246	SPKRAMP_C
CSA246	SPKRAMP_ICC_GB
CSA247	SPKRAMP_D
CSA247	SPKRAMP_E
CSA247	SPKRAMP_F

AUDIO CONN

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA248	

TOUCH ID

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA256	PKGS:TD_LARGER_PITCH

REF_DEBUG_DEBUG

	PACK_OPTIONS TO INCLUDE IN NETLIST
CSA294	VITAMINC

Pin Delay

pin delay file is imported by APPLEX
pin delay table has to be removed as it cuased fatal errors in cPlus

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Apple Inc.

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